University of Toronto

Term Test 1

Date - Feb 11, 2009

Duration: 7:15pm - 9pm

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)
2. Single handwritten aid sheet allowed.
3. Only tests written in pen will be considered for a re-mark.
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T F CMOS microchips typically consist of both PMOS and NMOS transistors

T F The "C" in CMOS stands for Complete

T F A 2-input NOR gate is designed to have the same worst-case rise and fall times. The best-case fall time is smaller than the best-case rise time in this gate.

T F The Body effect causes the threshold of an NMOS transistor to decrease when the V_{SB} is decreased.

T F A chain of identical minimum sized inverters can achieve an overall delay smaller than that of a single minimum sized inverter assuming both drive the same load capacitance.

T F A chain of three inverters has a total delay equal to the sum of delays of its individual inverters in the same chain.

T F Two NMOS transistors in series with their gates both tied to V_{DD} can pull the source of the bottom transitor up to but not exceeding $V_{DD} - 2V_{tn}$.

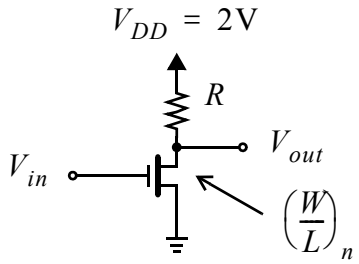
T F For the same driving capability, a two-input NAND gate has a smaller layout than a two-input NOR gate.

T F The capacitance of a reversed biased junction increases as the reverse bias voltage is increased.

T F Velocity saturation is more common in modern technologies as a result of the very thin gate oxide.

Last Name: _____

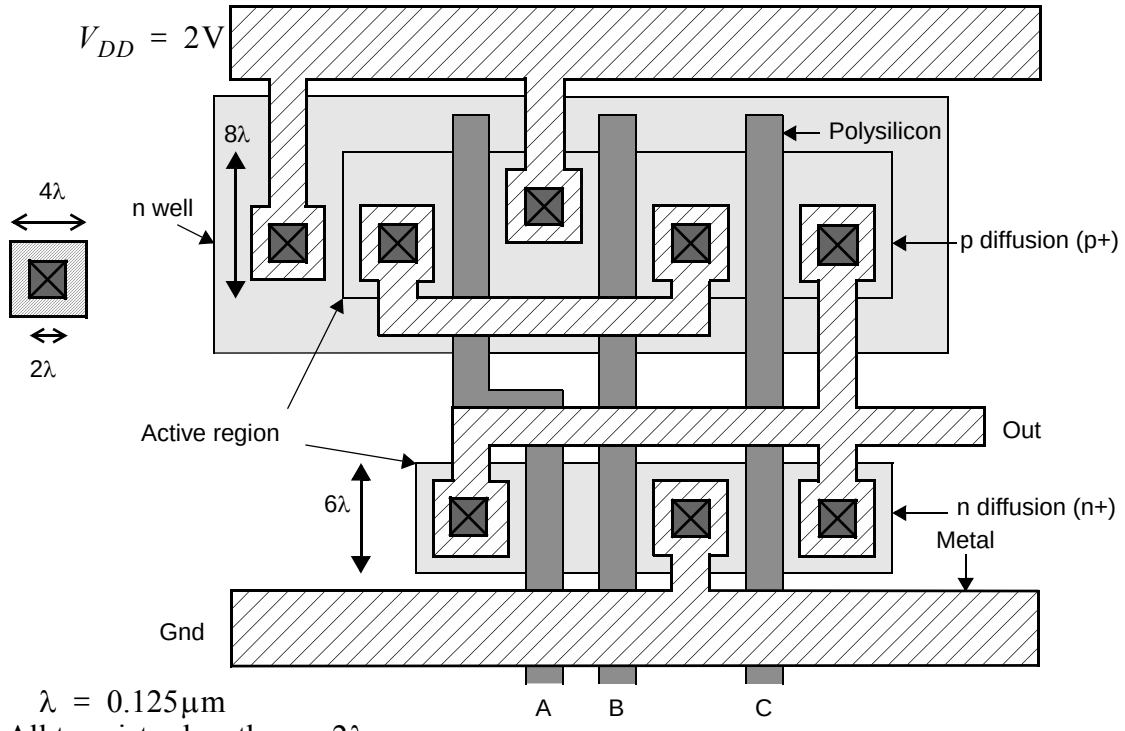
[6] Question 2:



R =
$\left(\frac{W}{L}\right)_n$ =

Consider the RTL inverter shown above. Using the transistor values on the last page, find values for R and $\left(\frac{W}{L}\right)_n$ such that the logic low output value, $V_{OL} = 0.2\text{V}$ and the average power dissipated by the inverter, $P_{\text{diss}} = 1\text{mW}$ when the output has an equal probability of being either high or low. Ignore any capacitance in this question.

[6] Question 3:



λ = 0.125μm

All transistor lengths are 2λ

a) Find the input capacitance of the input C (include overlap capacitance but no Miller effect)

C_{in_C} =

Question 1 (continued)

b) Identify on the layout above the drain of the PMOS connected to the output and find the output capacitance due to this drain when the output equals 2V.

C_{dp} =

c) Repeat b) for the case where the output equals 0V.

C_{dp} =

Last Name: _____

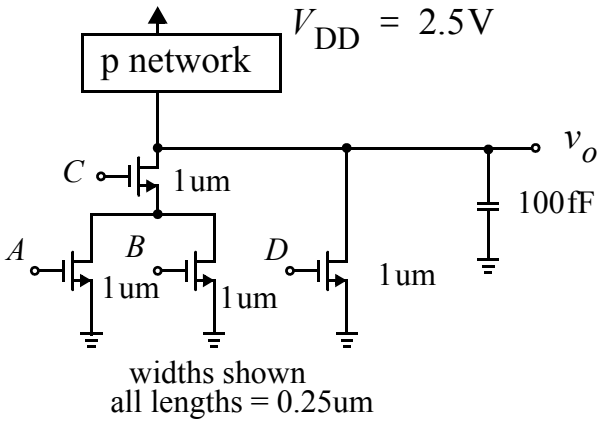
[6] Question 4: Consider a CMOS inverter with $V_{DD} = 2\text{V}$, $\left(\frac{W}{L}\right)_n = 4$, $\left(\frac{W}{L}\right)_p = 8$ and the output capacitance equal to 100fF.

a) Find t_{df} using the RC delay estimation.

$t_{df} =$

b) For a step input voltage (with zero rise time) from 0 to V_{DD}, sketch the **current**, I_{Dn}, through the NMOS transistor vs **time**. Label the points on your sketch where the transistor is in cutoff, active and/or triode and show the current and time values at the transitions of the different regions.

[6] Question 5: For the n portion of a complex CMOS gate shown below, find the slowest case, t_{df_slow} and fastest case, t_{df_fast} corresponding to different input patterns.



t_{df_slow} =

t_{df_fast} =

(blank sheet for scratch calculations)

Last Name: _____

ECE334F Digital Electronics Parameter Sheet

Physical Constants;

$\phi_T = kT/q = 26\text{mV}$ (at 300K); $k = 1.38 \times 10^{-23}$ J/K; $T = 300$ K (at $27°C$); $q = 1.6 \times 10^{-19}$ C;

$\varepsilon_o = 8.854 \times 10^{-12} F/\text{m}$; $k_{ox} = 3.9$; $\phi_s = 2|\phi_F| = 0.6V$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9\text{V}$

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	(see below)
PMOS	-0.4	0.4	30	0.1	6	0.3	2	(see below)

V_{T0} is the threshold voltage with zero bulk-source voltage.

γ is used to account for non-zero bulk-source voltage.

μC_{ox} is the transistor current gain parameter.

λ is to account for the transistor finite output impedance (channel length modulation).

C_{ox} is the gate capacitance per unit area.

C_o is the gate overlap capacitance per unit length.

C_j is the drain/source junction capacitance per unit area.

C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters **except under the gate**.

$C_{jsw} = 0.3\ fF/\mu m$ for both NMOS and PMOS

C_{jswg} is the drain/sourc junction capacitance per unit length under the gate.

$C_{jswg} = 0.15\ fF/\mu m$ for both NMOS and PMOS