University of Toronto

Term Test 2

Date - Mar 18, 2009

Duration: 7:15pm - 9pm

ECE334 — Digital Electronics

Lecturer - D. Johns

ANSWER QUESTIONS ON THESE SHEETS **USING BACKS IF NECESSARY**

1. Assume the parameters on the parameter sheet (last page) unless otherwise stated (mosfets are from a 0.25um CMOS technology)
2. Single handwritten aid sheet allowed.
3. Only tests written in pen will be considered for a re-mark.
4. Grading indicated by [ ]. Attempt all questions since a blank answer will certainly get 0.

Question	Mark
1	
2	
3	
4	
5	
Total	

Last Name: _____

First Name: _____

Student #: _____

(max grade = 29)

[5] Question 1: Answer the True [T] or False [F] questions below by **circling** the correct answer. Each correct answer is worth 0.5 marks.

T F In a 45nm CMOS process, the subthreshold leakage current can be a significant portion of the overall power dissipation of a digital chip.

T F The overall power dissipation of a digital chip consists of both static and dynamic power.

T F The dynamic power of a digital chip is due to the energy being dissipated across capacitors in the chip.

T F N-type silicon is made by doping pure silicon with Boron

T F Photoresist is a material that is applied to the glass masks during CMOS processing.

T F CMOS gates are made out of polysilicon so they will not melt during annealing.

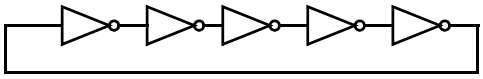
T F A self-aligned process means that the different masks are self-aligned with each other.

T F A via is a connection between adjacent levels of metal.

T F A register is made out of two latches where the latches are clocked on opposite phases.

T F A CMOS schmitt trigger is often used at the outputs of a digital chip to reduce noise.

[6] Question 2:



$V_{DD} = 2.5V$

all lengths = 0.25um

$f_1 =$

$f_2 =$

Consider the 5 state "ring oscillator" shown above. The oscillation frequency is given by $f = 1/(2Nt_d)$ where N is the number of inverters and t_d is the delay through a single inverter. Use the CMOS parameters on the last page and only account for gate capacitance.

a) Find f_1 assuming $W_n = 1\mu m$ and $W_p = 2\mu m$ for each inverter.

b) Find f_2 assuming $W_n = 4\mu m$ and $W_p = 8\mu m$ for each inverter.

[6] Question 3: Consider an aluminum wire that is $2\mu m$ above the substrate, is $0.7\mu m$ in height and has a width of w. Recall:

$$C = \varepsilon_{ox} l\left[\frac{w}{h} + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right] \qquad R = \left(\frac{\rho}{t}\right)\left(\frac{l}{w}\right)$$

Resistivity of Aluminum is $2.8\ \mu\Omega \bullet cm$

a) For the case of $w = 0.4\mu m$, find $R_{\square}$ (Ω/square) and C_l ($fF/\mu m$).

$R_{\square} =$

$C_l =$

b) Repeat a) but for $w = 1.2\mu m$.

$R_{\square} =$

$C_l =$

c) Compare the capacitance increase in parts a) and b) and explain what phenomenon causes such a small capacitance increase although the width increased by a factor of three.

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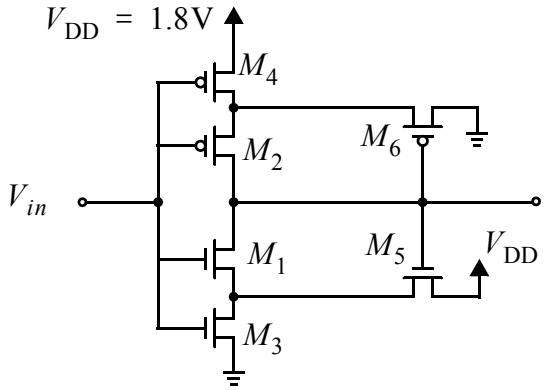
[6] Question 4: Consider the Schmitt trigger shown below where it is desired to have thresholds at 1.0V and 1.2V..



$\mu_n C_{ox} = 200\mu\text{A/V}^2$ All lengths = $0.2\mu\text{m}$

$\mu_p C_{ox} = 50\mu\text{A/V}^2$ $W_1 = W_3 = 1\mu\text{m}$

$V_{tn} = -V_{tp} = 0.25\text{V}$ $W_2 = W_4 = 2\mu\text{m}$

a) Find the width of either M_5 or M_6 such that the Schmitt trigger has one threshold at 1.2V (only one of these 2 transistors sets this threshold). Ignore body effect.

b) If the body effect is taken into account, would the thresholds move further apart, move closer together, both move up, both move down or stay the same? Explain.

[6] Question 5: Consider a bank of CMOS registers where $T_{\text{setup}} = 300ps$, $T_{\text{hold}} = 200ps$, $T_{ccq} = 100ps$ and $T_{pcq} = 250ps$. Also assume an average gate delay equals $T_{\text{gate}} = 50ps$.

a) If it is desired to run a system clock at 800MHz, how many gate delays can be in the logic between registers?

b) If an internal delay of 50ps is inserted into every register right at the clock input, what is the new T_{setup}, T_{hold}, T_{ccq}, T_{pcq}?

c) If an internal delay of 50ps is inserted into every register right at the "D" input, what is then new T_{setup}, T_{hold}, T_{ccq}, T_{pcq}?

(blank sheet for scratch calculations)

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ECE334F Digital Electronics Parameter Sheet

Physical Constants;

$\phi_T = kT/q = 26\text{mV}$ (at 300K); $k = 1.38 \times 10^{-23}$ J/K; $T = 300$ K (at $27°C$); $q = 1.6 \times 10^{-19}$ C;

$\varepsilon_o = 8.854 \times 10^{-12} F/\text{m}$; $k_{ox} = 3.9$; $\phi_s = 2|\phi_F| = 0.6V$

MOS Transistor; CMOS basic parameters. Channel length = $0.25\mu m$, $m_j = 0.5$, $\phi_o = 0.9\text{V}$

	V_{T0} (V)	γ $(V^{0.5})$	μC_{ox} $(\mu A/V^2)$	λ (V^{-1})	C_{ox} $(fF/\mu m^2)$	C_o $(fF/\mu m)$	C_j $(fF/\mu m^2)$	C_{jsw} $(fF/\mu m)$
NMOS	0.4	0.4	120	0.06	6	0.3	2	(see below)
PMOS	-0.4	0.4	30	0.1	6	0.3	2	(see below)

V_{T0} is the threshold voltage with zero bulk-source voltage.

γ is used to account for non-zero bulk-source voltage.

μC_{ox} is the transistor current gain parameter.

λ is to account for the transistor finite output impedance (channel length modulation).

C_{ox} is the gate capacitance per unit area.

C_o is the gate overlap capacitance per unit length.

C_j is the drain/source junction capacitance per unit area.

C_{jsw} is the drain/source junction capacitance per unit length to account for drain/source perimeter capacitance. Assume this value is the same for all perimeters **except under the gate**.

$C_{jsw} = 0.3\ fF/\mu m$ for both NMOS and PMOS

C_{jswg} is the drain/sourc junction capacitance per unit length under the gate.

$C_{jswg} = 0.15\ fF/\mu m$ for both NMOS and PMOS