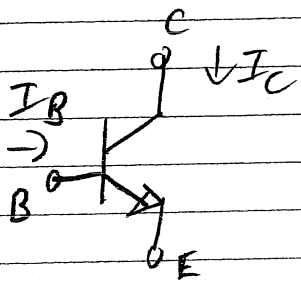


USE OF COMPOUND DEVICES

BJT

CURRENT GAIN

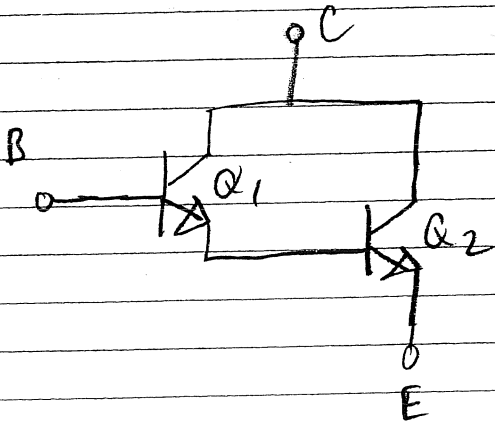
$$\beta = \frac{I_C}{I_B}$$



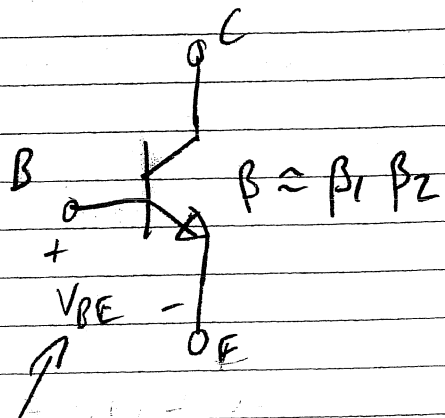
(ACTIVE REGION)

TO INCREASE CURRENT GAIN

USE A DARLINGTON CONFIGURATION



(\Rightarrow)



$$V_{BE} = V_{BE1} + V_{BE2}$$

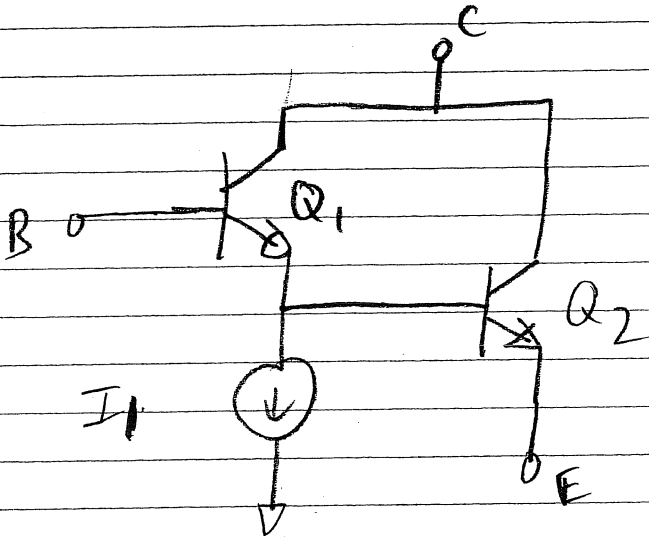
IF USED AS SHOWN ABOVE Q1 BIASED WITH ONLY I_{B2} (MAY BE TOO SMALL A BIAS CURRENT)

So

USUALLY ADD BIAS CURRENT TO

$Q_1 \Rightarrow$ ALSO HELPS TURN OFF Q_2

IF Q_1 TURNED OFF



FOR PNP \Rightarrow OFTEN USE NPN TOGETHER

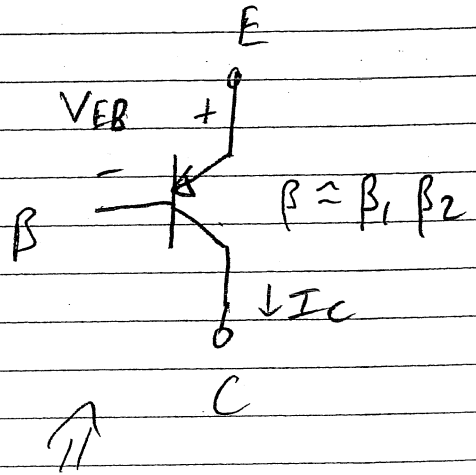
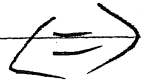
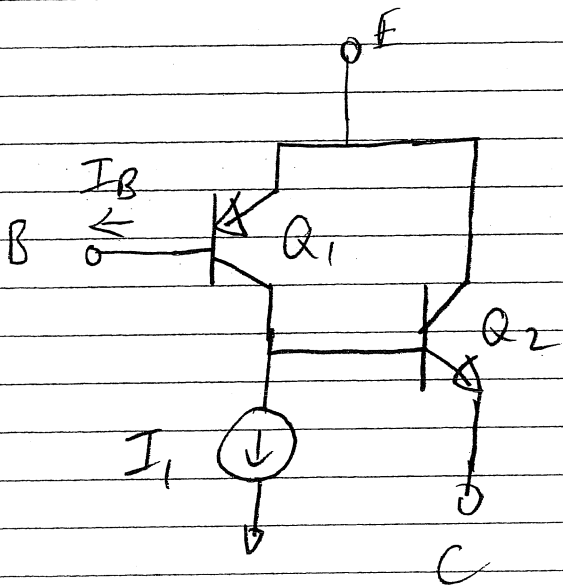
WITH PNP TO IMPROVE

PNP

(NPN USUALLY HAVE BETTER
 PERFORMANCE THAN PNP)
 (HIGHER β & HIGHER f_t)

ESPECIALLY IF PNP BUILT AS LATERAL DEVICE RATHER THAN VERTICAL DEVICE

CA3



$$I_C \approx \beta_N I_{SP}$$

WHERE I_{SP} IS SCALE CURRENT OF PNP Q_1

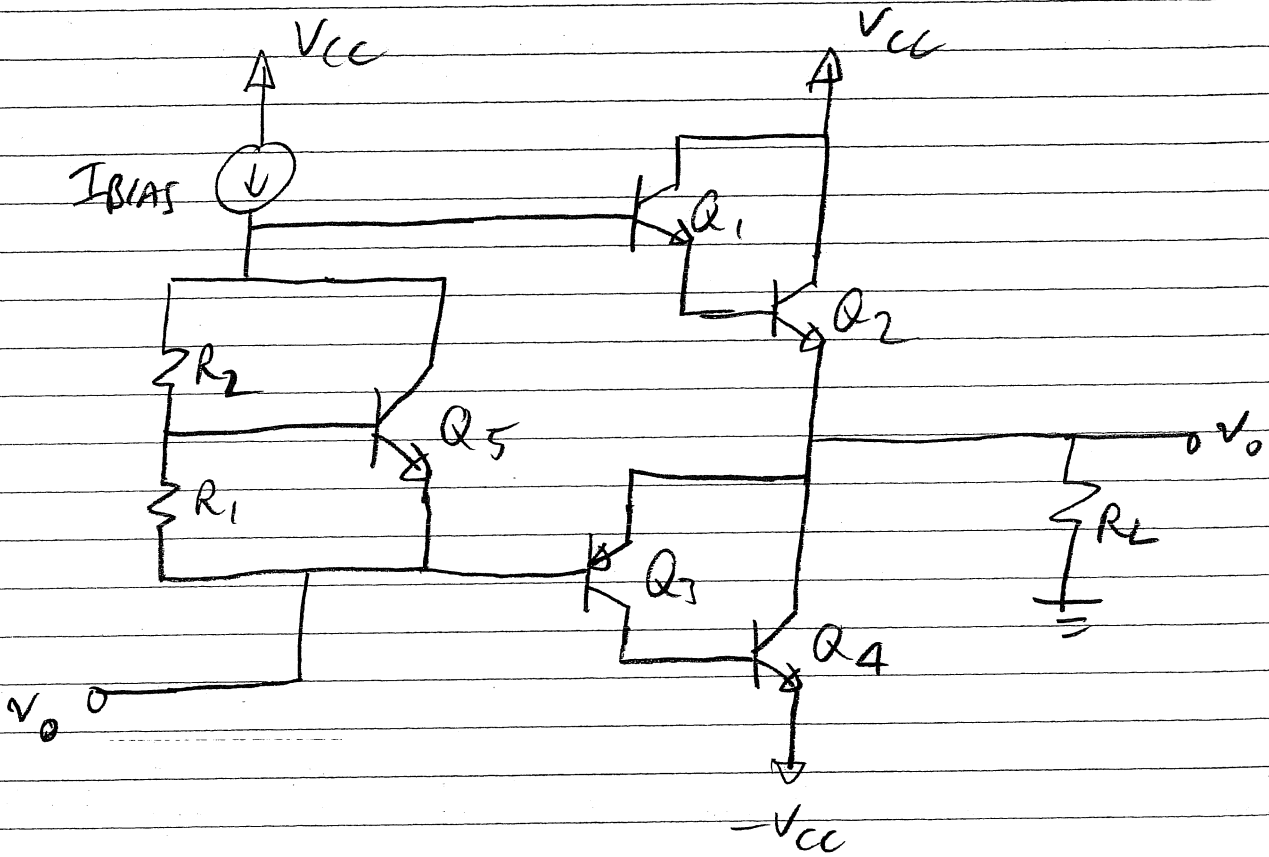
$$I_C \approx \beta_N I_{SP} e^{\frac{V_{EB}}{V_T}}$$

USE

NOTE THERE IS A FEEDBACK LOOP AROUND Q_1 & Q_2 HERE SO STABILITY MUST BE CONSIDERED

(CD4)

USE IN AN OUTPUT STAGE



$$\text{MIN } v_o \Rightarrow v_{o-\text{min}} + V_{BE3}$$

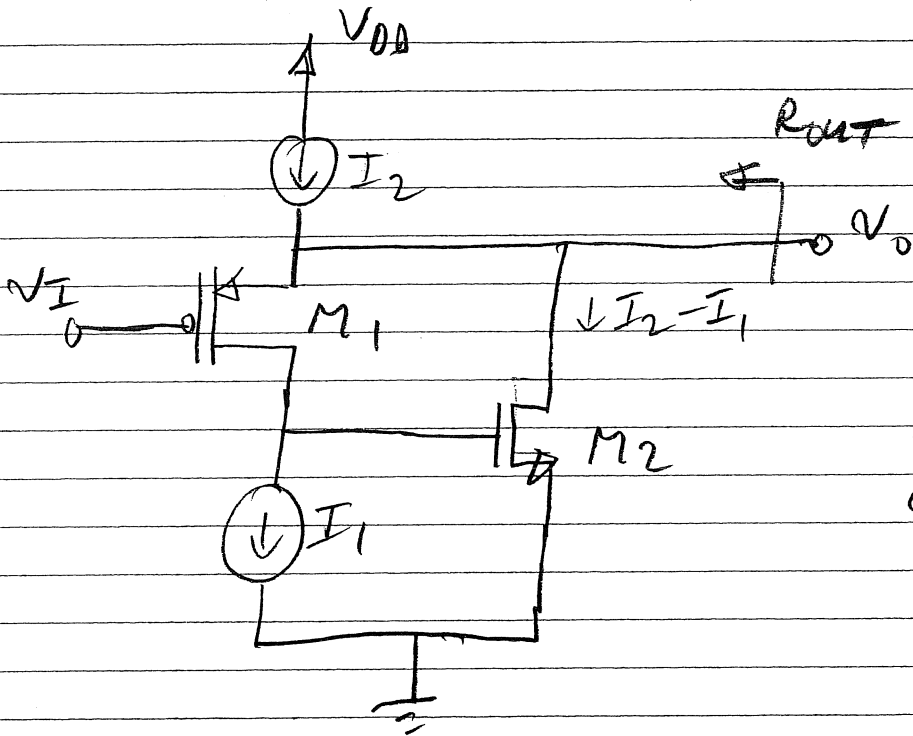
(SIMILAR TO PNP ALONE)

$$\text{MAX } v_o \Rightarrow V_{CC} - V_{BIAS} - V_{BE1} - V_{BE2}$$

(EXTRA V_{BE} DROP)

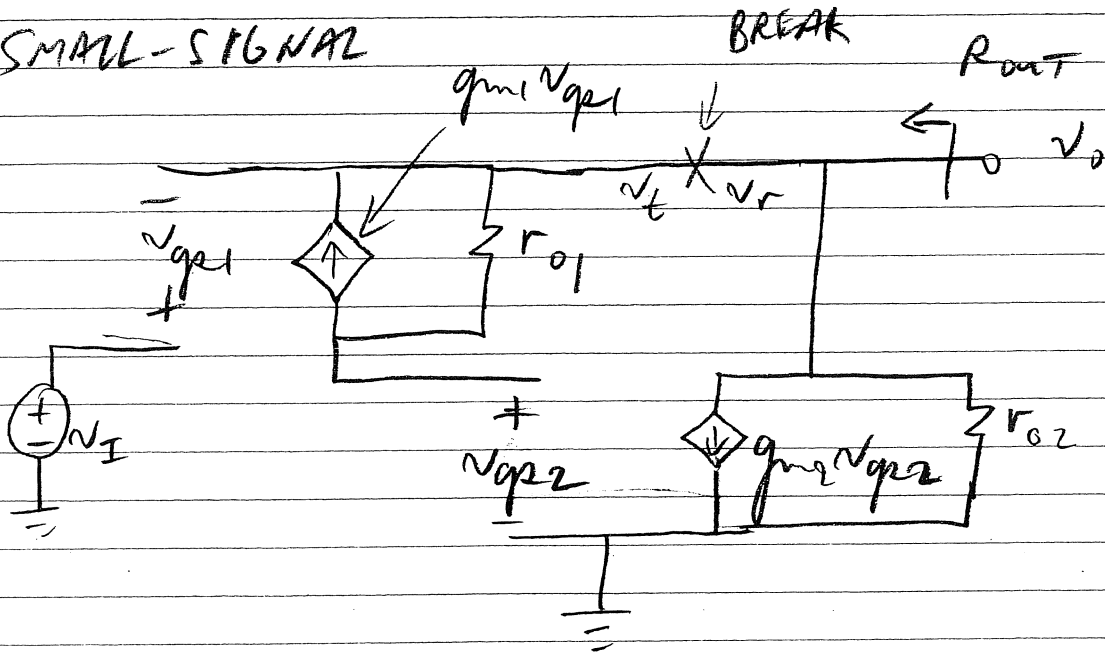
CMOS

SUPER SOURCE FOLLOWER



PMOS
 NMOS
 COMBINATION

SMALL-SIGNAL



CD6

IMPEDANCE SEEN TO LEFT OF BREAK $\rightarrow \infty$

$$\frac{v_{gs2}}{v_t} = (1 + g_{m1} r_{o1}) \approx g_{m1} r_{o1}$$

$$\frac{v_r}{v_{gs2}} = -g_{m2} r_{o2}$$

$$L \equiv -\frac{v_r}{v_t} \approx g_{m1} g_{m2} r_{o1} r_{o2}$$

$$R_{p0} = r_{o2}$$

$$L_s = 0$$

$$R_{out} = R_{p0} \left[\frac{1 + L_s}{1 + L_o} \right]$$

$$L_o = L$$

$$R_{out} = \frac{r_{o2}}{g_{m1} g_{m2} r_{o1} r_{o2}} = \frac{1}{\underline{\underline{g_{m2} (g_{m1} r_{o1})}}}$$

$$R_{out} \ll \frac{1}{g_{m2}}$$