7.3 Find the intrinsic gain of an NMOS transistor fabricated in a process for which $k_n' = 200\ \mu A/V^2$ and $V_A' = 20\ V\ \mu m$. The transistor has a 0.5-μm channel length and is operated at $V_{OV} = 0.25$ V. If a 2-mA/V transconductance is required, what must I_D and W be?

7.4 An NMOS transistor fabricated in a certain process is found to have an intrinsic gain of 80 V/V when operated at an I_D of 100 μA. Find the intrinsic gain for $I_D = 25\ \mu A$ and $I_D = 400\ \mu A$. For each of these currents, find the factor by which g_m changes from its value at $I_D = 100\ \mu A$.

D 7.5 Consider an NMOS transistor fabricated in a 0.18-μm technology for which $k_n' = 387\ \mu A/V^2$ and $V_A' = 5$ V/μm. It is required to obtain an intrinsic gain of 25 V/V and a g_m of 1 mA/V. find the required values of L, W/L, and the bias current I. Assume L=0.3um

D 7.9 Using a CMOS technology for which $k_n' = 200\ \mu A/V^2$ and $V_A' = 20$ V/μm, design a current-source-loaded CS amplifier for operation at $I = 50\ \mu A$ with $V_{OV} = 0.2$ V. The amplifier is to have an open-circuit voltage gain of −100 V/V. Assume that the current-source load is ideal. Specify L and W/L.

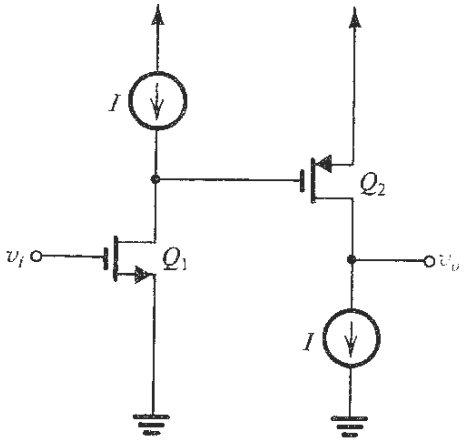

Figure P7.12

7.12 Figure P7.12 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2, find an expression for the overall voltage gain in terms of g_m and r_o of Q_1 and Q_2.

***7.13** The NMOS transistor in the circuit of Fig. P7.13 has $V_t = 0.5$ V, $k_n' W/L = 2$ mA/V², and $V_A = 20$ V.

(a) Neglecting the dc current in the feedback network and the effect of r_o, find V_{GS}. Then find the dc current in the feedback network and V_{DS}. Verify that you were justified in neglecting the current in the feedback network when you found V_{GS}.

(b) Find the small-signal voltage gain, v_o/v_i. What is the peak of the largest output sinewave signal that is possible while the NMOS transistor remains in saturation? What is the corresponding input signal?

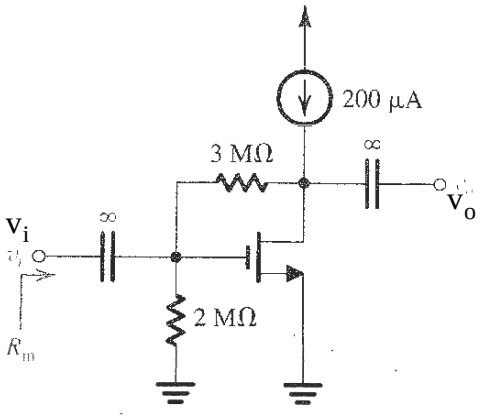

Figure P7.13