**D 11.15** Design the quiescent current of a class AB BJT output stage so that the incremental voltage gain for $v_i$ in the vicinity of the origin is in excess of 0.98 V/V for loads larger than 100 Ω. Assume that the BJTs have $V_{BE}$ of 0.7 V at a current of 100 mA and determine the value of $V_{BB}$ required.

***11.18** A class AB output stage, resembling that in Fig. 11.11 but utilizing a single supply of +10 V and biased at $V_i = 6$ V, is capacitively coupled to a 100-Ω load. For transistors for which $|V_{BE}| = 0.7$ V at 1 mA and for a bias voltage $V_{BB} = 1.4$ V, what quiescent current results? For a step change in output from 0 to −1 V, what input step is required? Assuming transistor saturation voltages of zero, find the largest possible positive-going and negative-going steps at the output.

**D 11.19** Consider the diode-biased class AB circuit of Fig. 11.14. For $I_{BIAS} = 100$ μA, find the relative size ($n$) that should be used for the output devices (in comparison to the biasing devices) to ensure that an output resistance of 10 Ω or less is obtained in the quiescent state. Neglect the resistance of the biasing diodes.

**D *11.20** A class AB output stage using a two-diode bias network as shown in Fig. 11.14 utilizes diodes having the same junction area as the output transistors. For $V_{CC} = 10$ V, $I_{BIAS} = 0.5$ mA, $R_L = 100$ Ω, $\beta_N = 50$, and $|V_{CEsat}| = 0$ V, what is the quiescent current? What are the largest possible positive and negative output signal levels? To achieve a positive peak output level equal to the negative peak level, what value of $\beta_N$ is needed if $I_{BIAS}$ is not changed? What value of $I_{BIAS}$ is needed if $\beta_N$ is held at 50? For this value, what does $I_Q$ become?

**11.23** A $V_{BE}$ multiplier is designed with equal resistances for nominal operation at a terminal current of 1 mA, with half the current flowing in the bias network. The initial design is based on $\beta = \infty$ and $V_{BE} = 0.7$ V at 1 mA.

(a) Find the required resistor values and the terminal voltage.
(b) Find the terminal voltage that results when the terminal current increases to 2 mA. Assume $\beta = \infty$.
(c) Repeat (b) for the case the terminal current becomes 10 mA.

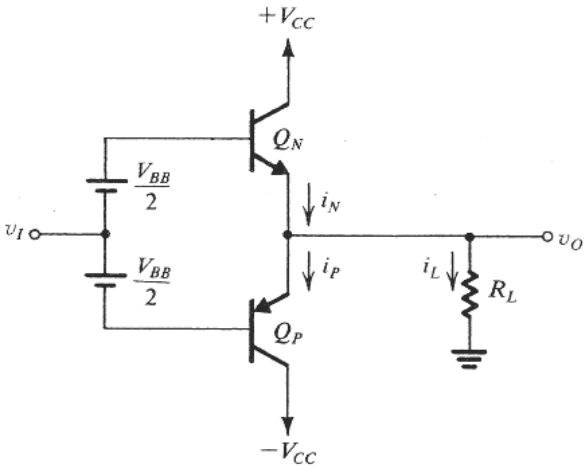


Fig. 11.11

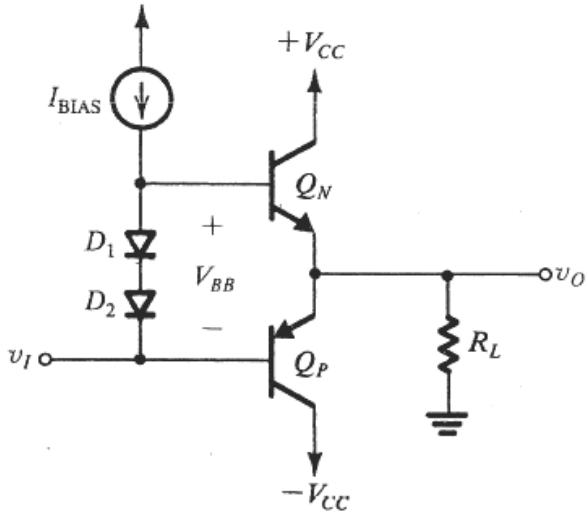


Fig. 11.14

**D 11.25** (a) For the circuit in Fig. 11.17 in which $Q_1$ and $Q_2$ are matched, and $Q_N$ and $Q_P$ are matched, show that the small-signal voltage gain at the quiescent condition is given by

$$\frac{v_o}{v_i} = \frac{R_L}{R_L + (2/g_m)}$$

where $g_m$ is the transconductance of each of $Q_N$ and $Q_P$ and where channel-length modulation is neglected.

(b) For the case $I_{BIAS} = 0.1$ mA, $R_L = 1$ kΩ, $k_n = k_p = nk_1 = nk_2$, where $k = \mu C_{ox}(W/L)$, and $k_1 = 20$ mA/V$^2$, find the ratio $n$ that results in an incremental gain of 0.98. Also find the quiescent current $I_Q$.

**D 11.26** Design the circuit of Fig. 11.17 to operate at $I_{Q_2} = 1$ mA with $I_{BIAS} = 0.1$ mA. Let $\mu_n C_{ox} = 250$ μA/V$^2$, $\mu_p C_{ox} = 100$ μA/V$^2$, $V_{tn} = -V_{tp} = 0.45$ V, and $V_{DD} = V_{SS} = 2.5$ V. Design so that $Q_1$ and $Q_2$ are matched and $Q_N$ and $Q_P$ are matched, and that in the quiescent state each operates at an overdrive voltage of 0.2 V.

(a) Specify the $W/L$ ratio for each of the four transistors.
(b) In the quiescent state with $v_O = 0$, what must $v_I$ be?
(c) If $Q_N$ is required to supply a maximum load current of 10 mA, find the maximum allowable output voltage. Assume that the transistor supplying $I_{BIAS}$ needs a minimum of 0.2 V to operate properly.

**D 11.29** It is required to design the circuit of Fig. 11.19 to drive a load resistance of 50 Ω while exhibiting an output resistance, around the quiescent point, of 2.5 Ω. Operate $Q_N$ and $Q_P$ at $I_Q = 1.5$ mA and $|V_{OV}| = 0.15$ V. The technology utilized is specified to have $k_n' = 250$ μA/V$^2$, $k_p' = 100$ μA/V$^2$, $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = V_{SS} = 2.5$ V.

(a) Specify $(W/L)$ for each of $Q_N$ and $Q_P$.
(b) Specify the required value of $\mu$.
(c) What is the expected error in the stage gain?
(d) In the quiescent state, what dc voltage must appear at the output of each of the error amplifiers?
(e) At what value of positive $v_O$ will $Q_P$ be supplying all the load current? Repeat for negative $v_O$ and $Q_N$ supplying all the load current.
(f) What is the linear range of $v_O$?

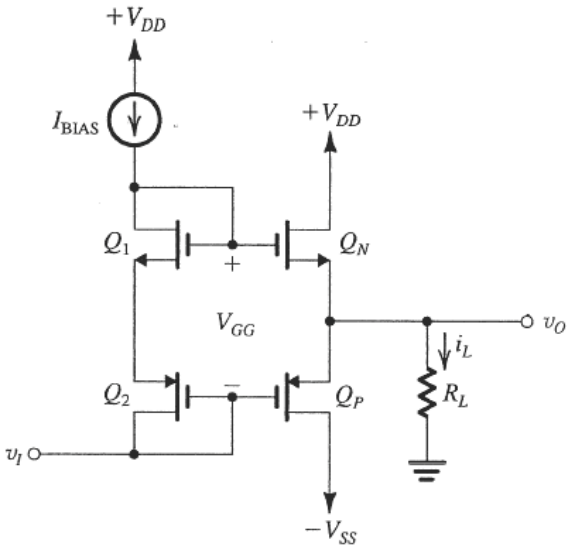


Fig. 11.17

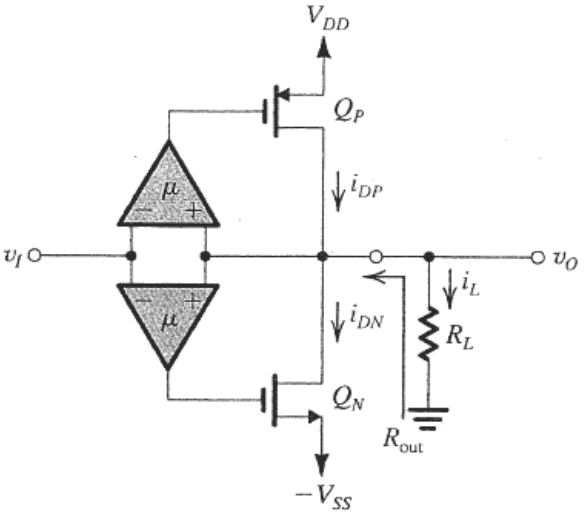


Fig. 11.19