Switched-Capacitor Circuits

Basic Building Blocks

Opamps

- Ideal opamps usually assumed.
- Important non-idealities
  - dc gain: sets the accuracy of charge transfer, hence, transfer-function accuracy.
  - unity-gain freq, phase margin & slew-rate: sets the max clocking frequency. A general rule is that unity-gain freq should be 5 times (or more) higher than the clock-freq.
  - dc offset: Can create dc offset at output. Circuit techniques to combat this which also reduce 1/f noise.
Basic Building Blocks

Double-Poly Capacitors

- Substantial parasitics with large bottom plate capacitance (20 percent of $C_1$)
- Also, metal-metal capacitors are used but have even larger parasitic capacitances.

Switches

- Mosfet switches are good switches.
  - off-resistance near $G\Omega$ range
  - on-resistance in 100$\Omega$ to 5k$\Omega$ range (depends on transistor sizing)
- However, have non-linear parasitic capacitances.
Basic Building Blocks

Non-Overlapping Clocks

- Non-overlapping clocks — both clocks are never on at same time
- Needed to ensure charge is not inadvertently lost.
- Integer values occur at end of \( \phi_1 \).
- End of \( \phi_2 \) is 1/2 off integer value.

Switched-Capacitor Resistor Equivalent

- Charged to \( V_1 \) and then \( V_2 \) during each clk period.
- \( \Delta Q = C_1(V_1 - V_2) \) every clock period
- \( Q_x = C_x V_x \) (1)
- \( C_1 \) charged to \( V_1 \) and then \( V_2 \) during each clk period.
- \( \Delta Q_1 = C_1(V_1 - V_2) \) (2)
- Find equivalent average current
  \[ I_{avg} = \frac{C_1(V_1 - V_2)}{T} \] (3)
  where \( T \) is the clk period.
Switched-Capacitor Resistor Equivalent

- For equivalent resistor circuit

\[ I_{eq} = \frac{V_1 - V_2}{R_{eq}} \]  \hspace{1cm} (4)

- Equating two, we have

\[ R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \]  \hspace{1cm} (5)

- This equivalence is useful when looking at low-freq portion of a SC-circuit.
- For higher frequencies, discrete-time analysis is used.

Resistor Equivalence Example

- What is the equivalent resistance of a 5pF capacitance sampled at a clock frequency of 100kHz.
- Using (5), we have

\[ R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^3)} = 2M\Omega \]

- Note that a very large equivalent resistance of 2M\Omega can be realized.
- Requires only 2 transistors, a clock and a relatively small capacitance.
- In a typical CMOS process, such a large resistor would normally require a huge amount of silicon area.
Parasitic-Sensitive Integrator

- Start by looking at an integrator which IS affected by parasitic capacitances
- Want to find output voltage at end of $\phi_1$ in relation to input sampled at end of $\phi_1$.

\[
v_i(n) = v_{ci}(nT) \quad v_o(n) = v_{co}(nT)
\]

\[
v_{ci}(t) \quad v_{cx}(t) \quad v_{co}(t)
\]

\[
v_{c2}(nT)
\]

\[
\begin{align*}
\phi_1 & \\
\phi_2 & \\
C_2 & \\
C_1 & \\
\end{align*}
\]

Parasitic-Sensitive Integrator

- At end of $\phi_2$
  \[
  C_2v_{co}(nT - T/2) = C_2v_{co}(nT - T) - C_1v_{ci}(nT - T)
  \]
  \[\text{(6)}\]
- But would like to know the output at end of $\phi_1$
  \[
  C_2v_{co}(nT) = C_2v_{co}(nT - T/2)
  \]
  \[\text{(7)}\]
- Leading to
  \[
  C_2v_{co}(nT) = C_2v_{co}(nT - T) - C_1v_{ci}(nT - T)
  \]
  \[\text{(8)}\]
Parasitic-Sensitive Integrator

• Modify above to write

\[ v_o(n) = v_o(n - 1) - \frac{C_1}{C_2} v_i(n - 1) \]  \hspace{1cm} (9)

and taking z-transform and re-arranging, leads to

\[ H(z) = \frac{V_o(z)}{V_i(z)} = -\left( \frac{C_1}{C_2} \right) \frac{1}{z - 1} \]  \hspace{1cm} (10)

• Note that gain-coefficient is determined by a ratio of two capacitance values.
• Ratios of capacitors can be set VERY accurately on an integrated circuit (within 0.1 percent)
• Leads to very accurate transfer-functions.

Typical Waveforms
Low Frequency Behavior

- Equation (10) can be re-written as

\[ H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{z^{1/2} - z^{-1/2}} \]  \hspace{1cm} (11)

- To find freq response, recall

\[ z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \]  \hspace{1cm} (12)
\[ z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right) \]  \hspace{1cm} (13)
\[ z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right) \]  \hspace{1cm} (14)

\[ H(e^{j\omega T}) = -\left(\frac{C_1}{C_2}\right)\frac{\cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)}{j2\sin\left(\frac{\omega T}{2}\right)} \]  \hspace{1cm} (15)

Low Frequency Behavior

- Above is exact but when \( \omega T \ll 1 \) (i.e., at low freq)

\[ H(e^{j\omega T}) \approx -\left(\frac{C_1}{C_2}\right)\frac{1}{j\omega T} \]  \hspace{1cm} (16)

- Thus, the transfer function is same as a continuous-time integrator having a gain constant of

\[ K_I \approx \frac{C_1}{C_2 T} \]  \hspace{1cm} (17)

which is a function of the integrator capacitor ratio and clock frequency only.
Parasitic Capacitance Effects

Accounting for parasitic capacitances, we have

\[ H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right) \frac{1}{z - 1} \]  \hspace{1cm} (18)

Thus, gain coefficient is not well controlled and partially non-linear (due to \( C_{p1} \) being non-linear).

Parasitic-Insensitive Integrators

By using 2 extra switches, integrator can be made insensitive to parasitic capacitances

— more accurate transfer-functions
— better linearity (since non-linear capacitances unimportant)
Parasitic-Insensitive Integrators

- Same analysis as before except that $C_1$ is switched in polarity before discharging into $C_2$.

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right) \frac{1}{z-1}$$  \hspace{1cm} (19)

- A positive integrator (rather than negative as before)

- $C_{p3}$ has little effect since it is connected to virtual gnd
- $C_{p4}$ has little effect since it is driven by output
- $C_{p2}$ has little effect since it is either connected to virtual gnd or physical gnd.
Parasitic-Insensitive Integrators

- $C_{p1}$ is continuously being charged to $v_i(n)$ and discharged to ground.

- $\phi_1$ on — the fact that $C_{p1}$ is also charged to $v_i(n-1)$ does not affect $C_1$ charge.

- $\phi_2$ on — $C_{p1}$ is discharged through the $\phi_2$ switch attached to its node and does not affect the charge accumulating on $C_2$.

- While the parasitic capacitances may slow down settling time behavior, they do not affect the discrete-time difference equation

\[
C_{p1}v_i(n) = C_1v_o(n-1) \quad \text{(20)}
\]

Parasitic-Insensitive Inverting Integrator

\[
C_2v_{co}(nT-T/2) = C_2v_{co}(nT-T) \quad \text{(20)}
\]
\[
C_2v_{co}(nT) = C_2v_{co}(nT-T/2) - C_1v_{ci}(nT) \quad \text{(21)}
\]

- Present output depends on present input (delay-free)

\[
H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2} \frac{z}{z-1} \quad \text{(22)}
\]

- Delay-free integrator has negative gain while delaying integrator has positive gain.
Signal-Flow-Graph Analysis

Vin(z) \rightarrow C_1 \rightarrow V_1(z)

V_2(z) \rightarrow C_2 \rightarrow V_2(z)

V_3(z) \rightarrow C_3 \rightarrow V_3(z)

V_1(z) \rightarrow -C_1(1 - z^{-1})

V_2(z) \rightarrow C_2z^{-1}

V_3(z) \rightarrow -C_3

\frac{1}{C_A} \frac{1}{1 - z^{-1}} \rightarrow V_o(z)

First-Order Filter

- Start with an active-RC structure and replace resistors with SC equivalents.
- Analyze using discrete-time analysis.
First-Order Filter

\[ V_i(z) \quad \begin{array}{c} \phi_1 \\ C_2 \end{array} \quad \begin{array}{c} \phi_1 \\ \phi_2 \end{array} \quad C_3 \quad \phi_1 \]

\[ V_o(z) \quad \begin{array}{c} \phi_1 \\ \phi_2 \end{array} \quad \begin{array}{c} \phi_1 \\ \phi_2 \end{array} \quad \begin{array}{c} \phi_1 \\ C_A \end{array} \]

\[ V_i(z) \]

\[ \begin{array}{c} -C_2 \\ -C_1(1 - z^{-1}) \end{array} \]

\[ \begin{array}{c} 1 \\ C_A \\ \frac{1}{1 - z^{-1}} \end{array} \]

\[ V_o(z) \]

\[ C_A(1 - z^{-1})V_o(z) = -C_3V_o(z) - C_2V_i(z) - C_1(1 - z^{-1})V_i(z) \quad (23) \]

\[ H(z) \equiv \frac{V_o(z)}{V_i(z)} = \frac{\left( \frac{C_1}{C_A} \right)(1 - z^{-1}) + \left( \frac{C_2}{C_A} \right)}{1 - z^{-1} + \frac{C_3}{C_A}} \quad (24) \]

\[ = \frac{\left( \frac{C_1 + C_2}{C_A} \right)z - \frac{C_1}{C_A}}{\left( 1 + \frac{C_3}{C_A} \right)z - 1} \]
First-Order Filter

• The pole of (24) is found by equating the denominator to zero

\[ z_p = \frac{C_A}{C_A + C_3} \]  \hspace{1cm} (25)

• For positive capacitance values, this pole is restricted to the real axis between 0 and 1 — circuit is always stable.

• The zero of (24) is found to be given by

\[ z_z = \frac{C_1}{C_1 + C_2} \]  \hspace{1cm} (26)

• Also restricted to real axis between 0 and 1.

First-Order Filter

The dc gain is found by setting \( z = 1 \) which results in

\[ H(1) = \frac{-C_2}{C_3} \]  \hspace{1cm} (27)

• Note that in a fully-differential implementation, effective negative capacitances for \( C_1, C_2 \) and \( C_3 \) can be achieved by simply interchanging the input wires.

• In this way, a zero at \( z = -1 \) could be realized by setting

\[ C_1 = -0.5C_2 \]  \hspace{1cm} (28)
First-Order Example

• Find the capacitance values needed for a first-order SC-circuit such that its 3dB point is at 10kHz when a clock frequency of 100kHz is used.
• It is also desired that the filter have zero gain at 50kHz (i.e. \( z = -1 \)) and the dc gain be unity.
• Assume \( C_A = 10pF \).

Solution

• Making use of the bilinear transform \( p = (z - 1)/(z + 1) \) the zero at \(-1\) is mapped to \( \Omega = \infty \).
• The frequency warping maps the -3dB frequency of 10kHz (or \( 0.2\pi \) rad/sample) to

\[
\Omega = \tan \left( \frac{0.2\pi}{2} \right) = 0.3249 \quad (29)
\]

• in the continuous-time domain leading to the continuous-time pole, \( p_p \), required being

\[
p_p = -0.3249 \quad (30)
\]

• This pole is mapped back to \( z_p \) given by

\[
z_p = \frac{1 + p_p}{1 - p_p} = 0.5095 \quad (31)
\]

• Therefore, \( H(z) \) is given by

\[
H(z) = \frac{k(z + 1)}{z - 0.5095} \quad (32)
\]
First-Order Example

- where $k$ is determined by setting the dc gain to one (i.e. $H(1) = 1$) resulting

$$H(z) = \frac{0.24525(z + 1)}{z - 0.5095} \quad (33)$$

- or equivalently,

$$H(z) = \frac{0.4814z + 0.4814}{1.9627z - 1} \quad (34)$$

- Equating these coefficients with those of (24) (and assuming $C_A = 10pF$) results in

$$C_1 = 4.814pF \quad (35)$$
$$C_2 = -9.628pF \quad (36)$$
$$C_3 = 9.628pF \quad (37)$$

Switch Sharing

- Share switches that are always connected to the same potentials.
Fully-Differential Filters

- Most modern SC filters are fully-differential
- Difference between two voltages represents signal (also balanced around a common-mode voltage).
- Common-mode noise is rejected.
- Even order distortion terms cancel

\[ v_{p1} = k_1 v_1 + k_2 v_1^2 + k_3 v_1^3 + k_4 v_1^4 + \ldots \]
\[ v_{\text{diff}} = 2k_1 v_1 + 2k_3 v_1^3 + 2k_5 v_1^5 + \ldots \]
\[ v_{n1} = -k_1 v_1 + k_2 v_1^2 - k_3 v_1^3 + k_4 v_1^4 + \ldots \]
Fully-Differential Filters

• Negative continuous-time input — equivalent to a negative $C_1$

\[ V_i(z) \]
\[ - \]
\[ + \]
\[ C_1 \]
\[ \phi_1 \]
\[ \phi_2 \]
\[ C_2 \]
\[ \phi_1 \]
\[ \phi_2 \]
\[ C_3 \]
\[ \phi_1 \]
\[ \phi_2 \]
\[ C_4 \]
\[ \phi_1 \]
\[ \phi_2 \]

\[ V_o(z) \]
\[ + \]
\[ - \]

• Note that fully-differential version is essentially two copies of single-ended version, however ... area penalty not twice.

• Only one opamp needed (though common-mode circuit also needed)

• Input and output signal swings have been doubled so that same dynamic range can be achieved with half capacitor sizes (from $kT/C$ analysis)

• Switches can be reduced in size since small caps used.

• However, there is more wiring in fully-differ version but better noise and distortion performance.
Low-Q Biquad Filter

\[ H_a(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{k_2 s^2 + k_1 s + k_0}{s^2 + (\frac{\omega_o}{Q}) s + \omega_o^2} \] (38)

\[ \frac{1}{\omega_o} \]

\[ C_A = 1 \quad V_c(s) \]

\[ -\frac{1}{\omega_o} \]

\[ C_B = 1 \]

\[ \frac{Q}{\omega_o} \]

\[ \frac{1}{k_1} \]

\[ k_2 \]

\[ V_{out}(s) \]

\[ V_{in}(s) \]

\[ \omega_o / k_o \]

\[ 1 / k_1 \]

\[ k_2 \]

\[ \omega_o \]

\[ \frac{1}{\omega_o} \]

\[ C_1 \]

\[ K_1 C_1 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ K_2 C_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ K_3 C_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ V_{out}(z) \]

\[ V_{in}(z) \]

\[ K_1 C_1 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]

\[ \phi_1 \]

\[ \phi_2 \]
Low-Q Biquad Filter Design

\[ H(z) = \frac{V_o(z)}{V_i(z)} = \frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1} \]  \hspace{1cm} (39)

• we can equate the individual coefficients of “z” in (39) and (40), resulting in:

\[ K_3 = a_0 \]  \hspace{1cm} (41)
\[ K_2 = a_2 - a_0 \]  \hspace{1cm} (42)
\[ K_1K_5 = a_0 + a_1 + a_2 \]  \hspace{1cm} (43)
\[ K_6 = b_2 - 1 \]  \hspace{1cm} (44)
\[ K_4K_5 = b_1 + b_2 + 1 \]  \hspace{1cm} (45)

• A degree of freedom is available here in setting internal \( V_i(z) \) output
Low-Q Biquad Filter Design

- Can do proper dynamic range scaling
- Or let the time-constants of 2 integrators be equal by
  \[ K_4 = K_5 = \sqrt{b_1 + b_2 + 1} \]  
  \[ (46) \]

Low-Q Biquad Capacitance Ratio

- Comparing resistor circuit to SC circuit, we have
  \[ K_4 \approx K_5 \approx \omega_o T \]  
  \[ (47) \]
  \[ K_6 \approx \frac{\omega_o T}{Q} \]  
  \[ (48) \]
- However, the sampling-rate, \(1/T\), is typically much larger than the approximated pole-frequency, \(\omega_o\),
  \[ \omega_o T \ll 1 \]  
  \[ (49) \]

Low-Q Biquad Capacitance Ratio

- Thus, the largest capacitors determining pole positions are the integrating capacitors, \(C_1\) and \(C_2\).
- If \(Q < 1\), the smallest capacitors are \(K_4C_1\) and \(K_5C_2\) resulting in an approximate capacitance spread of \(1/(\omega_o T)\).
- If \(Q > 1\), then from (48) the smallest capacitor would be \(K_6C_2\) resulting in an approximate capacitance spread of \(Q/(\omega_o T)\) — can be quite large for \(Q > 1\).
High-Q Biquad Filter

- Use a high-Q biquad filter circuit when $Q \gg 1$
- Q-damping done with a cap around both integrators
- Active-RC prototype filter

\[
\begin{align*}
\frac{1}{\omega_o} & = \frac{1}{Q} \\
C_1 & = 1 \\
C_2 & = 1 \\
\end{align*}
\]

\[
\begin{align*}
V_{in}(s) & \quad \omega_o/k_o \\
k_1/\omega_o & \quad -1/\omega_o \\
k_2 & \quad V_{out}(s)
\end{align*}
\]

High-Q Biquad Filter

- Q-damping now performed by $K_6 C_1$
High-Q Biquad Filter

- Input $K_1 C_1$: major path for lowpass
- Input $K_2 C_1$: major path for band-pass filters
- Input $K_3 C_2$: major path for high-pass filters
- General transfer-function is:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \frac{-K_3 z^2 + (K_1 K_5 + K_2 K_5 - 2 K_3)z + (K_3 - K_2 K_5)}{z^2 + (K_4 K_5 + K_5 K_6 - 2)z + (1 - K_5 K_6)}$$ (50)

- If matched to the following general form

$$H(z) = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$ (51)

High-Q Biquad Filter

$$K_1 K_5 = a_0 + a_1 + a_2$$ (52)
$$K_2 K_5 = a_2 - a_0$$ (53)
$$K_3 = a_2$$ (54)
$$K_4 K_5 = 1 + b_0 + b_1$$ (55)
$$K_5 K_6 = 1 - b_0$$ (56)

- And, as in lowpass case, can set

$$K_4 = K_5 = \sqrt{1 + b_0 + b_1}$$ (57)

- As before, $K_4$ and $K_5$ approx $\omega_o T \ll 1$ but $K_6 \approx 1/Q$
Charge Injection

- To reduce charge injection (thereby improving distortion), turn off certain switches first.

\[ V_1(z) \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3 \rightarrow Q_4 \rightarrow \phi_1 \rightarrow \phi_2 \rightarrow V_o(z) \]

- Advance \( \phi_{1a} \) and \( \phi_{2a} \) so that only their charge injection affect circuit (result is a dc offset)

\[ Q_{CH} = -WLC_{ox}V_{eff} = -WLC_{ox}(V_{GS} - V_t) \] (58)

- Charge related to \( V_{GS} \) and \( V_t \) and \( V_t \) related to substrate-source voltage.

- Source of \( Q_3 \) and \( Q_4 \) remains at 0 volts — amount of charge injected by \( Q_3, Q_4 \) is not signal dependent and can be considered as a dc offset.
Charge Injection Example

• Estimate dc offset due to channel-charge injection when $C_1 = 0$ and $C_2 = C_A = 10C_3 = 10pF$.

• Assume switches $Q_3, Q_4$ have $V_{th} = 0.8V$, $W = 30\mu m$, $L = 0.8\mu m$, $C_{ox} = 1.9 \times 10^{-3} \text{ pF/}\mu \text{m}^2$, and power supplies are $\pm 2.5V$.

• Channel-charge of $Q_3, Q_4$ (when on) is

$$Q_{CH3} = Q_{CH4} = -(30)(0.8)(0.0019)(2.5 - 0.8)$$

$$= -77.5 \times 10^{-3} \text{ pC}$$

• dc feedback keeps virtual opamp input at zero volts.

Charge Injection Example

• Charge transfer into $C_3$ given by

$$Q_{C3} = -C_3v_{out}$$

(60)

• We estimate half channel-charges of $Q_3, Q_4$ are injected to the virtual ground leading to

$$\frac{1}{2}(Q_{CH3} + Q_{CH4}) = Q_{C3}$$

(61)

which leads to

$$v_{out} = \frac{77.5 \times 10^{-3} \text{ pC}}{1pF} = 78 \text{ mV}$$

(62)

• dc offset affected by the capacitor sizes, switch sizes and power supply voltage.