### A/D Converter Basics

\[ V_{in} \rightarrow \text{A/D} \rightarrow B_{out} \]

\[ V_{ref} \]

\[ V_{ref}(b_12^{-1} + b_22^{-2} + \ldots + b_N2^{-N}) = V_{in} \pm x \]

where \( \left( -\frac{1}{2}V_{LSB} < x < \frac{1}{2}V_{LSB} \right) \)  

- **Range of valid input values** produce the **same output signal** — quantization error.

\[ B_{out} \]

\[ \frac{V_{LSB}}{V_{ref}} = \frac{1}{4} = 1\text{ LSB} \]
### Analog to Digital Converters

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### Integrating Converters

- Low offset and gain errors for low-speed applications
- Small amount of circuitry
- Conversion speed is $2^{N+1} \times 1/T_{\text{clk}}$

(Vin is held constant during conversion.)

$T_{\text{clk}} = \frac{1}{f_{\text{clk}}}$
Integrating Converters

- Count at end of $T_2$ is digital output
- Does not depend on RC time-constant

- Notches the input frequencies which are multiples of $1/T_1$
Successive-Approximation Converters

- Makes use of binary search algorithm
- Requires N steps for N-bit converter
- Successively "tunes" a signal until within 1 LSB of input
- Medium speed
- Moderate accuracy

DAC Based Successive-Approximation

- Adjust $V_{D/A}$ until within 1 LSB of $V_{in}$
- Start with MSB and continue until LSB found
- D/A mainly determines overall accuracy
- Input S/H required
Charge Redistribution A/D

1. Sample mode

\[ V_x = 0 \]

\[ V_{in} = V_{ref} \]

2. Hold mode

\[ V_x = -V_{in} \]

\[ V_{in} = \frac{V_{ref}}{2} \]

3. Bit cycling

\[ V_x = -V_{in} + \frac{V_{ref}}{2} \]

- Combines S/H, D/A converter, and difference circuit
- **Sample mode**: Caps charged to \( V_{in} \), compar reset.
- **Hold mode**: Caps switched to gnd so \( V_x = -V_{in} \)
- **Bit cycling**: Cap switched to \( V_{ref} \). If \( V_x < 0 \) cap left connected to \( V_{ref} \) and bit=1. Otherwise, cap back to gnd and bit=0. Repeat \( N \) times
- **Cap bottom plates** connected to \( V_{ref} \) side to minimize parasitic capacitance at \( V_x \). Parasitic cap does not cause conversion errors but it attenuates \( V_x \).
Algorithmic (or Cyclic) A/D Converter

- Operates similar to successive-approx converter
- Successive-approx halves ref voltage each cycle
- Algorithmic doubles error each cycle (leaving ref voltage unchanged)

Signed input

Flowchart:
1. Start
2. Sample $V = V_{in}$, $i = 1$
3. If $V > 0$
   - $b_i = 1$
   - $V \rightarrow 2(V - \frac{V_{ref}}{4})$
   - $i \rightarrow i + 1$
   - Go to step 4.
4. If $i > N$
   - Stop
5. If $V < 0$
   - $b_i = 0$
   - $V \rightarrow 2(V + \frac{V_{ref}}{4})$
   - $i \rightarrow i + 1$
   - Go to step 4.

Ratio-Independent Algorithmic Converter

- Small amount of circuitry — reuse cyclically in time
- Requires a high-precision multiply by 2 gain stage

Diagram:
- $V_{in}$ to S/H
- Gain amp X2
- Cmp
- Shift register
- Out
- $V_{ref}/4$
- $-V_{ref}/4$
**Ratio-Independent Algorithmic Converter**

1. Sample remainder and cancel input-offset voltage.
2. Transfer charge $Q_1$ from $C_1$ to $C_2$.
3. Sample input signal with $C_1$ again after storing charge $Q_1$ on $C_2$.
4. Combine $Q_1$ and $Q_2$ on $C_1$, and connect $C_1$ to output.

- Does not rely on cap matching
- Sample input twice using $C_1$; hold first charge in $C_2$ and re-combine with first charge on $C_1$

**Flash (or Parallel) Converters**

- High-speed
- Large size and power hungry
- $2^N$ comparators
- Speed bottleneck usually large cap load at input
- Thermometer code out of comps
- Nands used for simpler decoding and/or bubble error correction
- Use comp offset cancellation
Issues in Designing Flash A/D Converters

- **Input Capacitive Loading** — use interpolating arch.
- **Resistor-String Bowing** — Due to $I_{in}$ of bipolar comps — force center tap (or more) to be correct.
- **Signal and/or Clock Delay** — Small arrival diff in clock or input cause errors. (250MHz 8-bit A/D needs 5ps matching for 1LSB) — route clock and $V_{in}$ together with the delays matched [Gendai, 1991]. Match capacitive loads
- **Substrate and Power-Supply Noise** — $V_{ref} = 2$ V and 8-bit, 7.8 mV of noise causes 1 LSB error — shield clocks and use on-chip supply cap bypass
- **Flashback** — Glitch at input due to going from track to latch mode — use preamps in comparators and match input impedances

Flash Converters — Bubble Errors

- Thermometer code should be 1111110000
- Bubble error (noise, metastability) — 1111110100
- Usually occurs near transition point but can cause **gross errors** depending on encoder
(2N–1) to N encoder

N digital outputs

Two-Step A/D Converters

• High-speed, medium accuracy (but 1 sample latency)
• Less area and power than flash
• Only 32 comparators in above 8-bit two-step
• Gain amp likely sets speed limit
• Without digital error correction, many blocks need at least 8-bit accuracy
Digital Error Correction

- Relaxes requirements on input A/D
- Requires a 5-bit 2nd stage since $V_q$ increased

Interpolating A/D Converters

- Use input amps to amplify input around reference voltages
- Latch thresholds less critical
- Less cap on input (faster than flash)
- Match delays to latches
- Often combined with folding architecture
Interpolating Converters

![Graph showing interpolating converters with voltages V1, V2, V2a, and V2b.]

V_in (Volts) vs. Vin (Volts)

Latch threshold

Pipelined A/D Converters

![Diagram of a pipelined A/D converter with N-bit shift register and DAPRX digital approximators.]

Vin – N-bit shift register

1-bit DAPRX

Analog pipeline (DAPRX - digital approximator)

S/H

Cmp

Vin – Vref/4

Vref/4

V_in
Time-Interleaved A/D Converters [Black, 80]

- Use parallel A/Ds and multiplex them
- Tone occurs at $f_s/N$ for $N$ converters if mismatched
- Input S/H critical, others not — perhaps different tech for input S/H