

# Continuous-Time Filters



## Motivation

### Switched-capacitor filters

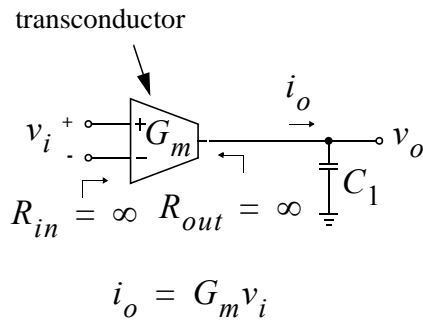
- + Accurate transfer-functions
- + High linearity, good noise performance
- Limited in speed
- Requires anti-aliasing filters

### Continuous-time filters

- Moderate transfer-function accuracy (requires tuning circuitry)
- Moderate linearity
- + High-speed
- + Good noise performance



## G<sub>m</sub>-C Integrators



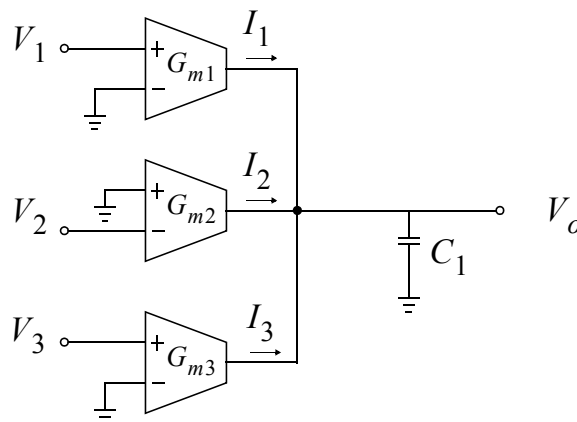
$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \equiv \left(\frac{\omega_{ti}}{s}\right) V_i$$

$$\omega_{ti} = \frac{G_m}{C_1}$$

- Use a transconductor to build an integrator
- Output current is linearly related to input voltage
- Output impedance is ideally infinite
- Note — an OTA (operational transconductance amplifier) has a high  $G_m$  value but not usually linear.



## Multiple-Input G<sub>m</sub>-C Integrator



$$V_o = \frac{1}{sC_1} (G_{m1}V_1 - G_{m2}V_2 + G_{m3}V_3)$$



## Example

- What  $G_m$  is needed for an integrator having a unity-gain frequency of  $\omega_{ti} = 20 \text{ MHz}$  when  $C = 2 \text{ pF}$ ?

$$G_m = \frac{2\pi \times 20 \text{ MHz} \times 2 \text{ pF}}{1} = 0.251 \text{ mA/V} \quad (1)$$

or equivalently,

$$G_m = 1/3.98 \text{ k}\Omega \quad (2)$$

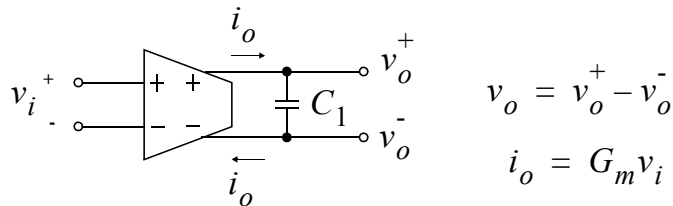
- which is related to unity-gain frequency by

$$2\pi \times 20 \text{ MHz} = \frac{1}{3.98 \text{ k}\Omega \times 2 \text{ pF}} \quad (3)$$



## Fully-Differential Integrators

- Better noise and linearity than single-ended.

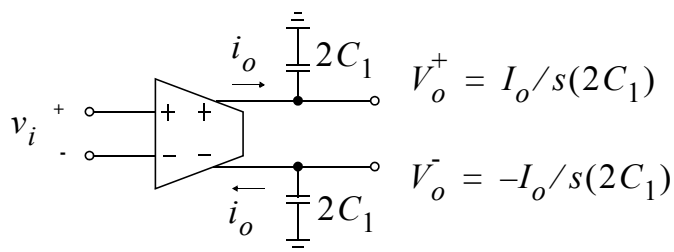


$$V_o = \frac{I_o}{sC_1} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1}$$

- Use a single capacitor between differential outputs
- Requires some sort of common-mode feedback to set output common-mode voltage
- Needs some extra caps for compensating common-mode feedback loop.



## Fully-Differential Integrators



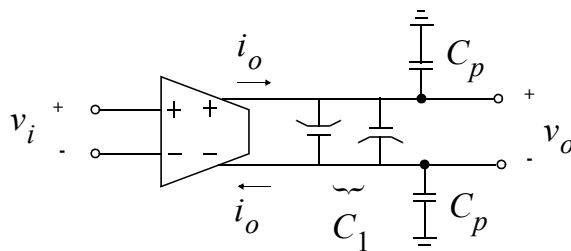
$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1} \quad v_o = v_o^+ - v_o^-$$

$$i_o = G_m v_i$$

- Use 2 grounded capacitors
- Still requires common-mode feedback but compensation caps for common-mode feedback can be the same grounded capacitors



## Fully-Differential Integrators

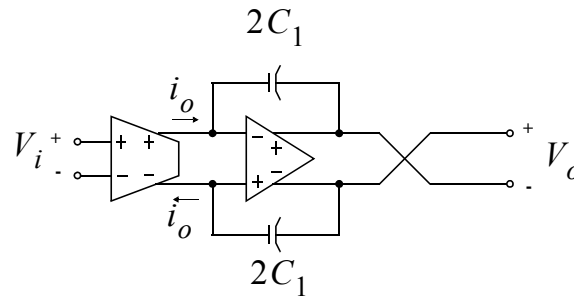


$$V_o = \frac{G_m V_i}{s(C_1 + C_p/2)} \quad \omega_{ti} = \frac{G_m}{(C_1 + C_p/2)}$$

- Integrated capacitors have top and bottom plate parasitic capacitances.
- To maintain symmetry, usually 2 parallel caps used as shown above
- Note that parasitic capacitance affects time-constant



## G<sub>m</sub>-C Opamp Integrator



$$V_o = \frac{2I_o}{s(2C_1)} = \frac{G_m V_i}{sC_1} \quad \omega_{ti} = \frac{G_m}{C_1}$$

- Use an extra opamp to improve linearity and noise performance
- Also known as a “Miller Integrator”



## G<sub>m</sub>-C Opamp Integrator

### Advantages

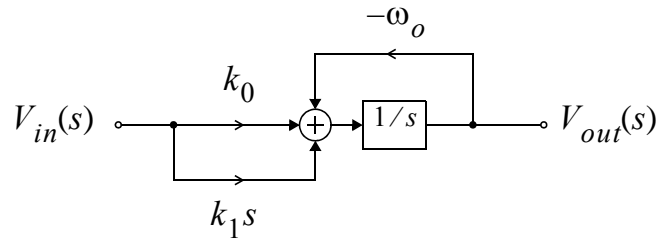
- Effect of parasitic caps reduced by opamp gain — more accurate time-constant and better linearity.
- Less sensitive to noise since transconductor output is low impedance (due to opamp feedback).
- $G_m$  cell drives virtual gnd — output-impedance of  $G_m$  cell can be lower and smaller voltage swing needed.

### Disadvantages

- Lower operating speed because it now relies on feedback
- Larger power dissipation
- Larger silicon area



## First-Order Filter



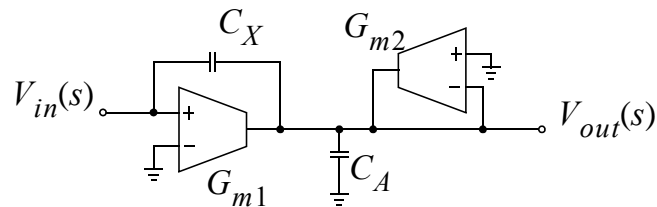
- General first-order transfer-function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{k_1 s + k_0}{s + \omega_0} \quad (4)$$

- Built with a single integrator and two feedin branches.
- $\omega_0$  sets the pole frequency



## First-Order Filter



$$C_X = \left( \frac{k_1}{1 - k_1} \right) C_A \text{ where } (0 \leq k_1 < 1) \quad \begin{aligned} G_{m1} &= k_0(C_A + C_X) \\ G_{m2} &= \omega_0(C_A + C_X) \end{aligned}$$

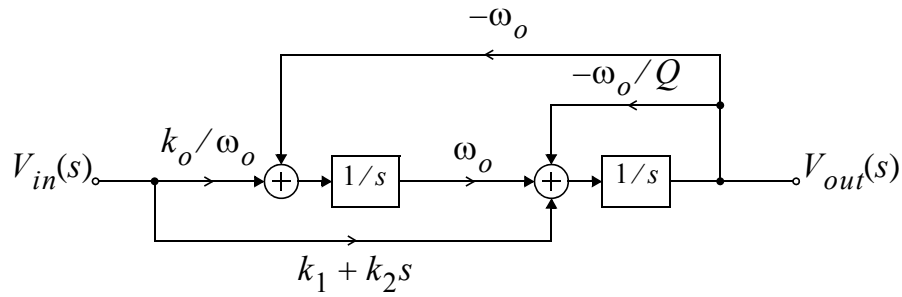
- Can show that the transfer function is given by

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{sC_X + G_{m1}}{s(C_A + C_X) + G_{m2}} = \frac{s \left( \frac{C_X}{C_A + C_X} \right) + \left( \frac{G_{m1}}{C_A + C_X} \right)}{s + \left( \frac{G_{m2}}{C_A + C_X} \right)} \quad (5)$$





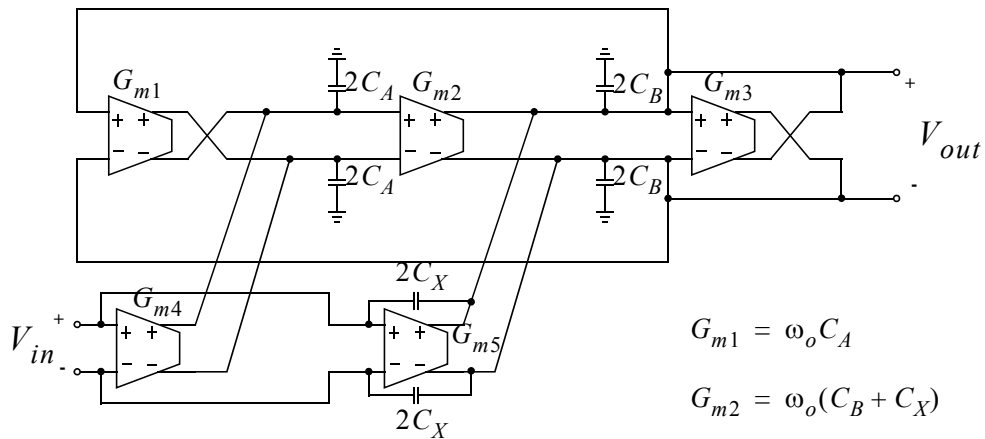
## Second-Order Filter



$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \quad (11)$$



## Second-Order Filter



$$G_{m1} = \omega_o C_A$$

$$G_{m2} = \omega_o (C_B + C_X)$$

$$G_{m3} = \frac{\omega_o (C_B + C_X)}{Q}$$

$$G_{m4} = (k_o C_A) / \omega_o$$

$$G_{m5} = k_1 (C_B + C_X)$$

$$C_X = C_B \left( \frac{k_2}{1 - k_2} \right) \text{ where } (0 \leq k_2 < 1)$$



## Second-Order Filter

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2 \left( \frac{C_X}{C_X + C_B} \right) + s \left( \frac{G_{m5}}{C_X + C_B} \right) + \left( \frac{G_{m2} G_{m4}}{C_A (C_X + C_B)} \right)}{s^2 + s \left( \frac{G_{m3}}{C_X + C_b} \right) + \left( \frac{G_{m1} G_{m2}}{C_A (C_X + C_B)} \right)} \quad (12)$$

- Note that there is a restriction on the high-frequency gain coeff  $k_2$  as in the first-order case.
- Note that  $G_{m3}$  sets the damping of this biquad
- $G_{m1}$  and  $G_{m2}$  form two integrators with unity-gain frequencies of  $\omega_0/s$ .



## Example

- Find values for a bandpass filter with a center frequency of 20MHz, a  $Q$  value of 5, and a center frequency gain of 1.
- Assume  $C_A = C_B = 2pF$

$$H(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = \frac{Gs \frac{\omega_o}{Q}}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} \quad (13)$$

where  $G = 1$  is the gain at the center frequency.



## Example

- Since,  $\omega_o = 2\pi \times 20\text{MHz}$  and  $Q = 5$ , we find

$$k_1 = G \frac{\omega_o}{Q} = 2.513 \times 10^7 \text{ rad/s} \quad (14)$$

- Since  $k_0$  and  $k_2$  are zero, we have  $C_x = G_{m4} = 0$
- The transconductance values are:

$$G_{m1} = \omega_o C_A = 0.2513 \text{ mA/V} \quad (15)$$

$$G_{m2} = \omega_o (C_B + C_X) = 0.2513 \text{ mA/V} \quad (16)$$

$$G_{m3} = G_{m5} = k_1 C_B = 50.27 \mu\text{A/V} \quad (17)$$



## Bipolar Transconductors

- 2 main methods

### Fixed Transconductor with Gain Cell

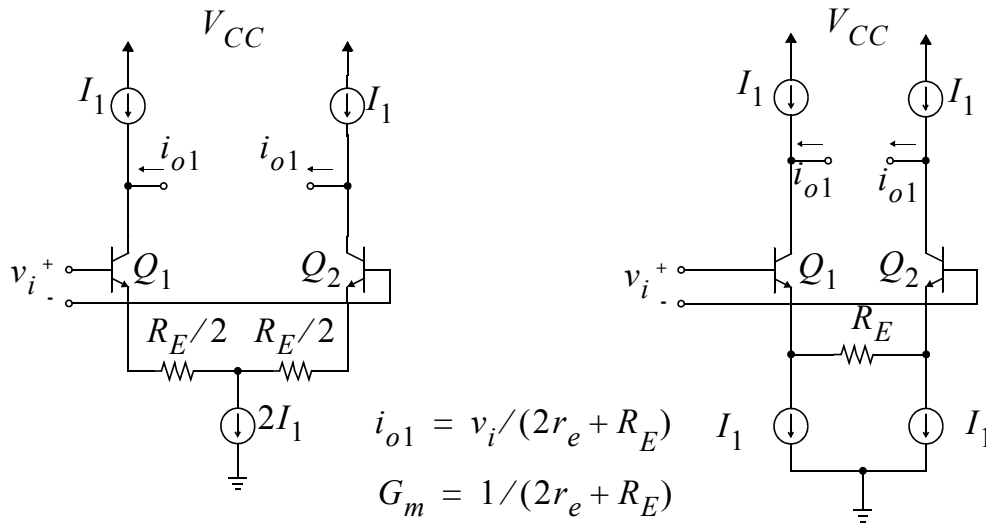
- Larger input range, lower transconductance
- Create a transconductor with a fixed  $G_m$  value using a resistor
- Tune the transconductance using a gain cell

### Multiple Differential Pairs

- Smaller input range, higher transconductance
- Use 2 diff pairs to extend linear input range
- Tuning done by adjusting bias current



## Fixed Transconductors using Resistors



- Left circuit needs higher common-mode voltage



## Max Differential Input Range

- Determine when one of diff transistors turns off
- For example, find when  $Q_2$  turns off in right circuit
- If  $Q_2$  off, then all of  $I_1$  flows through  $R_E$  resulting in

$$V_{i,max} = I_1 R_E \quad (18)$$

- However, there is significant distortion at this point since  $V_{be}$  is not constant
- Maximum input range might be half that resulting in

$$V_{i,max} = (I_1/2) R_E \quad (19)$$



## Distortion

- So far, have assumed  $V_{be}$  voltages remain constant which is reasonable if  $r_e \ll R_E$

$$r_e \equiv \frac{V_T}{I_E} \quad (20)$$

implying

$$r_{e, \max} = \frac{V_T}{I_{E, \min}} \ll R_E \quad (21)$$

or equivalently,

$$I_{E, \min} \gg \frac{V_T}{R_E} \quad (22)$$



## Distortion

### Example

- If  $R_E = 20k\Omega$  and  $V_T = 25mV$ , then  $I_{E, \min} \gg 1.25 \mu A$

### How much is “much greater than”?

- Depends on how much distortion can be tolerated
- If  $r_{e, \max} = 0.1R_E$  when  $V_{i, \max} = (I_1/2)R_E$ , the actual output current is 3% from ideal linear response.
- Results in about a 1% THD (3 times better than peak linearity error)
- Can use smaller input signals but then noise might dominate



## Transconductance

- Use small-signal T-model for bipolar transistors

$$i_{o1} = \frac{v_i}{r_{e1} + R_E + r_{e2}} = \frac{v_i}{2r_e + R_E} \quad (23)$$

where  $r_e$  is small-signal emitter resist ( $r_e = \alpha/g_m$ )

$$r_e = \frac{V_T}{I_E} = \frac{V_T}{I_1} \quad (24)$$

- Leading to

$$G_m = \frac{i_{o1}}{v_i} = \frac{1}{2r_e + R_E} \quad (25)$$



## Example

- Given  $R_E = 3k\Omega$  (i.e.  $G_m \approx 0.333 \text{ mA/V}$ ),  
 $V_{i, \max} = \pm 500 \text{ mV}$ , find  $I_1$  so  $r_{e, \max} < 0.1R_E$

- We have  $r_{e, \max} < 0.1R_E = 300\Omega$  which occurs when

$$I_{E2, \min} = \frac{V_T}{r_{e, \max}} = \frac{26 \text{ mV}}{300\Omega} = 86.7 \mu\text{A} \quad (26)$$

- For this same input voltage of 500 mV

$$I_{RE} \approx \frac{500 \text{ mV}}{3k\Omega} = 167 \mu\text{A} \quad (27)$$



## Example

- Since  $I_1 = I_{RE} + I_{E2}$

$$I_1 = 167 + 86.7 = 253 \mu A \quad (28)$$

- Thus, a minimum bias current of  $253 \mu A$  should be chosen resulting in a nominal  $r_e$  and  $G_m$  given by

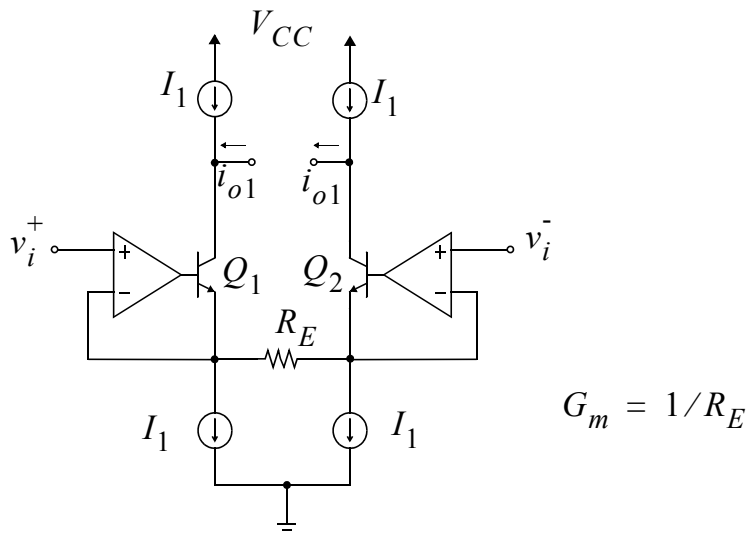
$$r_e = \frac{V_T}{I_1} = 103 \Omega \quad (29)$$

$$G_m = \frac{1}{(2r_e + R_E)} = 0.312 \text{ mA/V} \quad (30)$$

- A 4 times increase in  $I_1$  would improve distortion by about 10 times but use more power.



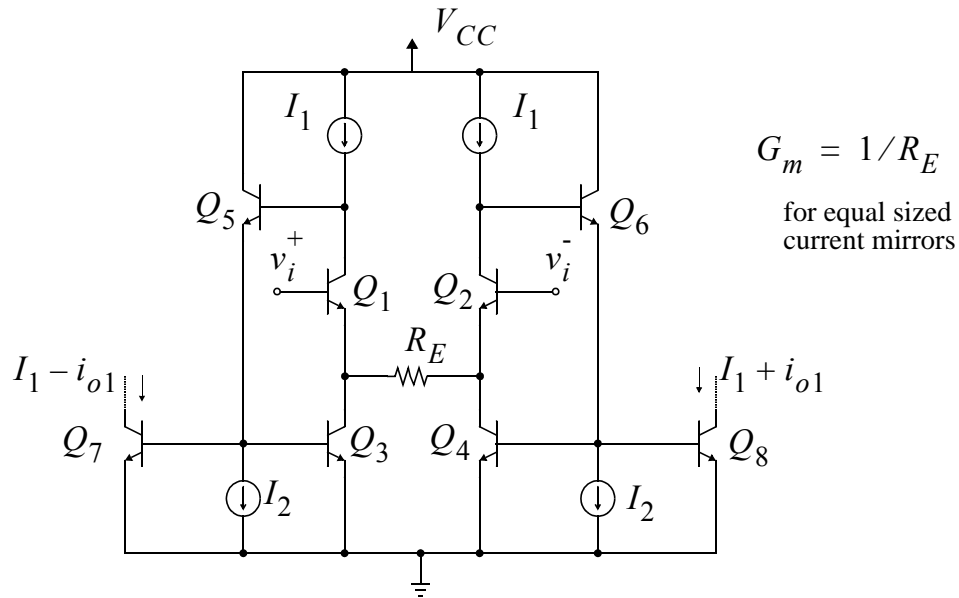
## Linear Transconductor — Opamps



- Feedback keeps input voltage across  $R_E$
- Simple opamps used (typically single stage)



## Linear Transconductor — Constant Current



- Fix  $I_C$  through diff pair with feedback

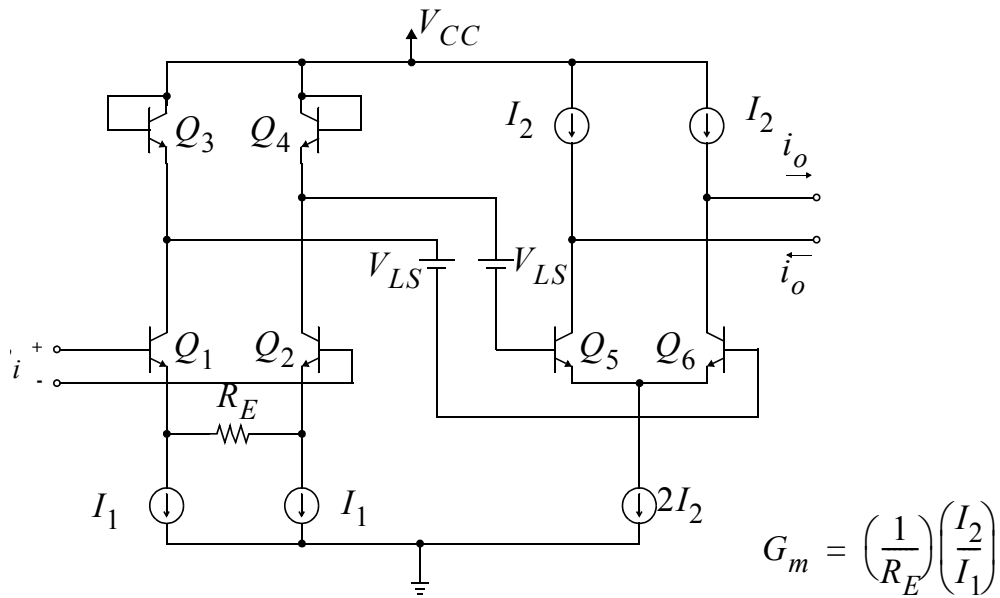


## Gain-Cell Transconductor

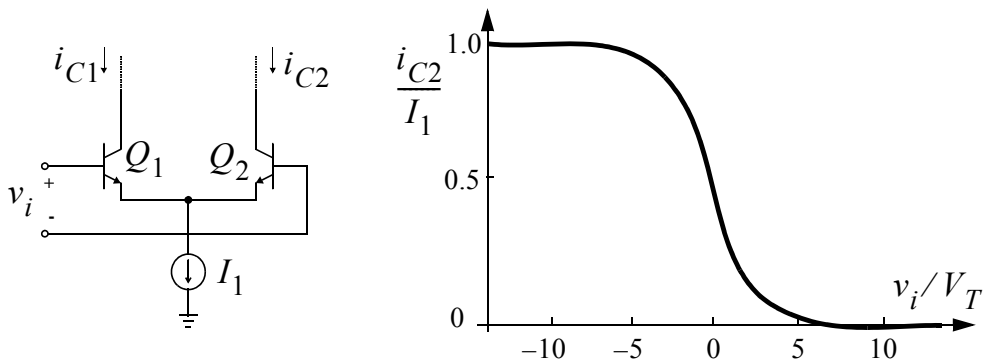
- Use a gain-cell to adjust output current
- Output current of gain-cell is a scaled version of input current determined by ratio of two currents
- Gain-cell is a translinear circuit and is closely related to translinear multiplier (also known as a Gilbert multiplier)
- Gain-cell is highly linear
- Often requires the use of voltage level-shifters



## Gain-Cell Transconductor



## Differential Pair



$$i_{C2} = \frac{I_1}{1 + e^{v_i/V_T}} \quad (31)$$

- Relatively linear near  $v_i = 0$

$$G_m = \frac{1}{2r_e} = \frac{I_1}{4V_T} \quad (32)$$

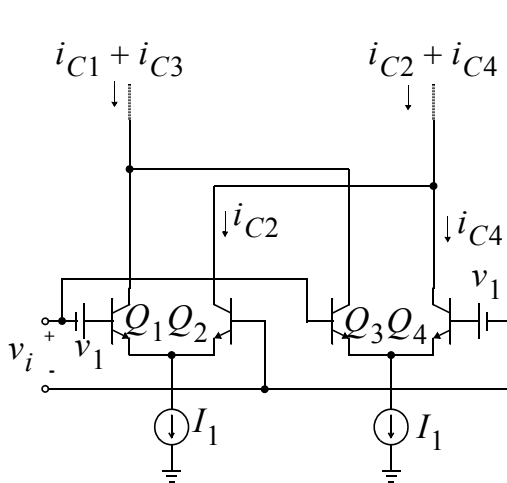


## Differential Pair

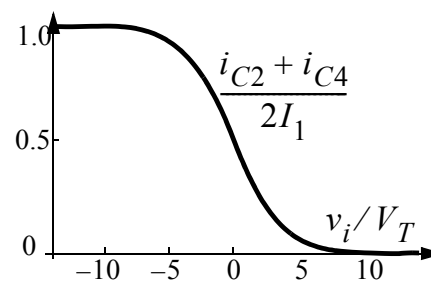
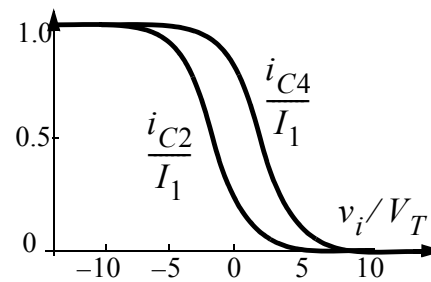
- $G_m$  proportional to  $I_1$
- However, limited input range — when  $v_i > 32\text{mV}_{pp}$ , THD > 1%.
- Use multiple diff pairs to increase linear input range
- Conceptual — use 2 diff pairs with dc offset
- Actual — replace dc offsets by resizing transistors in differential pairs
- Increases input range to  $v_i > 96\text{mV}_{pp}$  for 1% THD



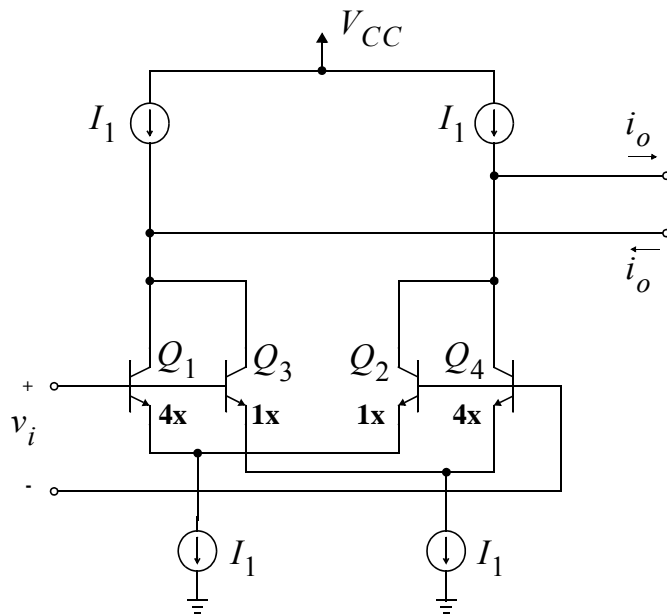
## Multiple Diff-Pairs



Choose  $v_1 = 1.317V_T$



## Multiple Diff-Pairs



$$G_m = \frac{8I_1}{25V_T}$$



## Multiple Diff-Pair

- When  $v_i = 0$ ,  $I$  through  $Q_1$  and  $Q_2$  are  $0.8I_1$  and  $0.2I_1$ .

$$G_m = \frac{1}{r_{e1} + r_{e2}} + \frac{1}{r_{e3} + r_{e4}} \quad (33)$$

$$r_{e1} = r_{e4} = \frac{V_T}{0.8I_1} \quad (34)$$

$$r_{e2} = r_{e3} = \frac{V_T}{0.2I_1} \quad (35)$$

$$G_m = \frac{8I_1}{25V_T} \quad (36)$$

- which is 28% larger than diff pair but uses twice the current — same current results in 36% less  $G_m$



## CMOS Transconductors

- A large variety of methods
- Best approach depends on application
- 2 main classifications — triode or active transistor based

### Triode vs. Active

- Triode based tends to have better linearity
- Active tend to have faster speed for the same operating current



## Triode Transconductors

- Recall n-channel triode equation

$$I_D = \mu_n C_{ox} \left( \frac{W}{L} \right) \left( (V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (37)$$

where to remain in triode

$$V_{DS} < V_{eff} \quad \text{where} \quad V_{eff} = V_{GS} - V_{tn} \quad (38)$$

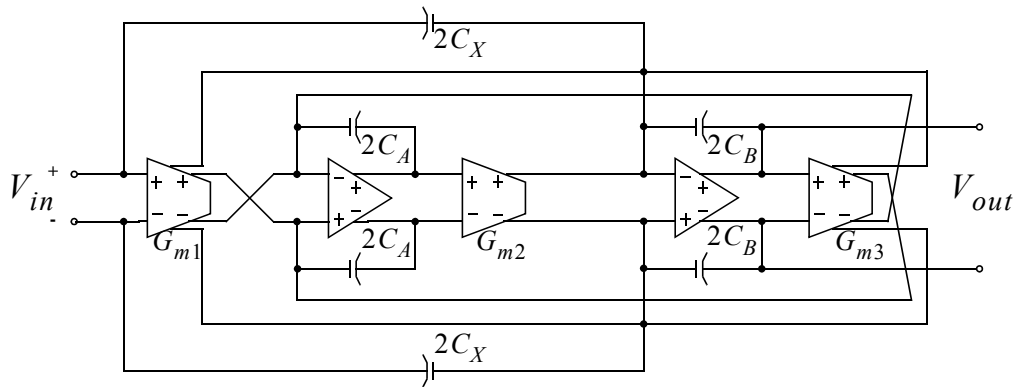
or equivalently,  $V_{GS} > V_{DS} + V_{tn}$

- Above models are only reasonably accurate (
- Not nearly as accurate as exponential model in BJTs
- Use fully-differential architectures to reduce even-order distortion terms — also improves common-mode noise rejection





## Biquad using Multiple Outputs



- Can make use of multiple outputs to build a biquad filter — scale extra outputs to desired ratio
- Reduces the number of transconductors — saves power and die area
- Above makes use of Miller integrators



## Active-Based Transconductors

- Active transistors are those operating in the active region
- Active region also referred to as pinch-off or saturation region
- In active region

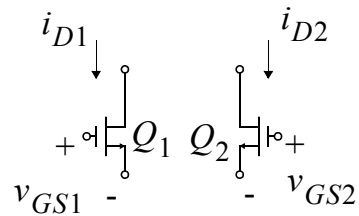
$$I_D = K_i(V_{GS} - V_{tn})^2 \quad (41)$$

when  $V_{DS} \geq V_{GS} - V_{tn} = V_{eff}$  and  $V_{GS} \geq V_{tn}$

- Here,  $K_i \equiv (\mu_n C_{ox} / 2)(W/L)_i$



## Constant Sum of Gate-Source Voltages



(matched devices)

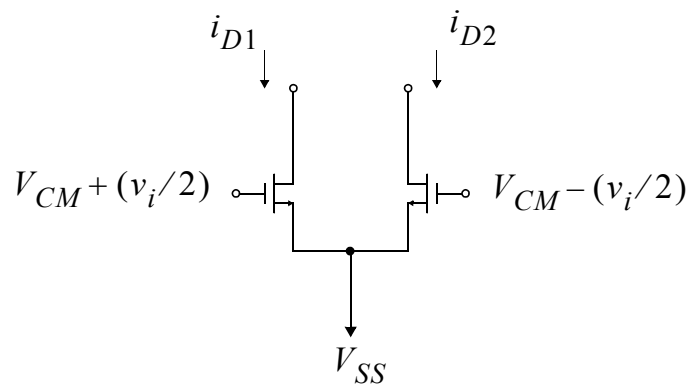
$$(i_{D1} - i_{D2}) = K(v_{GS1} + v_{GS2} - 2V_{tn})(v_{GS1} - v_{GS2}) \quad (42)$$

$$K = (\mu_n/2)C_{ox}\left(\frac{W}{L}\right) \quad (43)$$

- If  $V_{GS1} + V_{GS2} = \text{constant}$  then linear transconductor
- Note — Differential output current linear but single-ended currents have large second-order distortion.



## Source-Connected Differential Pair



$$(i_{D1} - i_{D2}) = 2K(V_{CM} - V_{SS} - V_{tn})(v_i)$$

$$G_m = 2K(V_{CM} - V_{SS} - V_{tn})$$

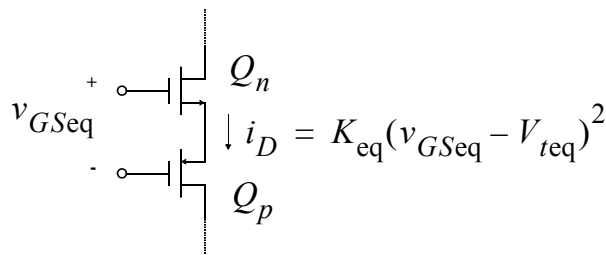


## Source-Connected Differential Pair

- Input signal varies symmetrically around a common-mode voltage
- Linearity limited due to square-law model being inaccurate
- In addition, even-order harmonics occur if the difference between two drain currents not exact.
- Limited to less than 50 dB linearity
- Adjust  $G_m$  by varying  $V_{CM}$
- In a short channel process, velocity saturation limits transconductance variation



## CMOS Pair



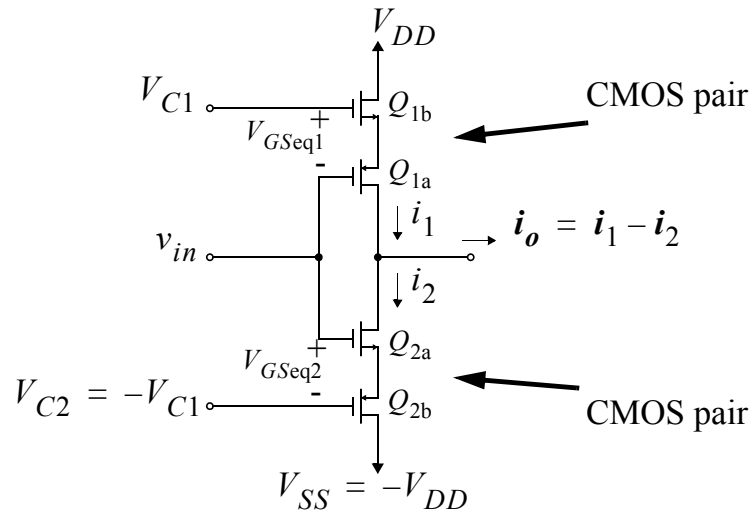
$$K_{eq} = \frac{K_n K_p}{(\sqrt{K_n} + \sqrt{K_p})^2} \quad V_{teq} = V_{tn} - V_{tp}$$

(where  $V_{tn} > 0$  and  $V_{tp} < 0$ )

- Above circuit acts as a single transistor with threshold  $V_{teq}$  and parameter  $K_{eq}$



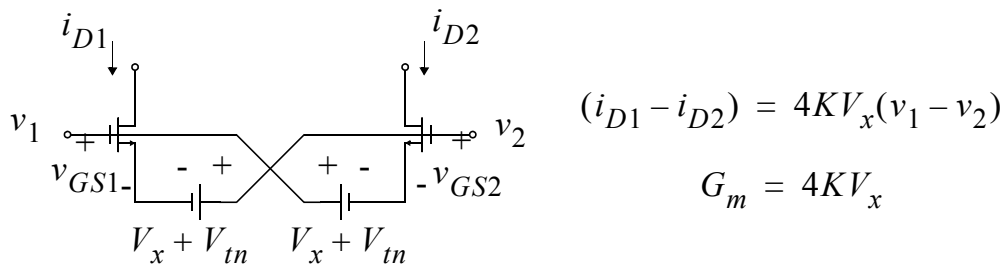
## Inverter-Based



$$G_m = 4K_{eq}(V_{C1} - V_{teq})$$



## Diff-Pair with Floating Voltage Sources



$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2)$$

$$G_m = 4KV_x$$

- Writing a voltage equation around the loop

$$v_{GS1} - (V_x + V_{tn}) + v_{GS2} - (V_x + V_{tn}) = 0 \quad (44)$$

implying

$$v_{GS1} + v_{GS2} = 2(V_x + V_{tn}) \quad (45)$$

- Thus, a constant sum of gate-source voltages occurs — even if input signal is not balanced



## Diff-Pair with Floating Voltage Sources

$$v_1 - v_{GS1} + V_x + V_{tn} = v_2 \quad (46)$$

$$v_2 - v_{GS2} + V_x + V_{tn} = v_1 \quad (47)$$

- Subtracting (46) from (47), we obtain

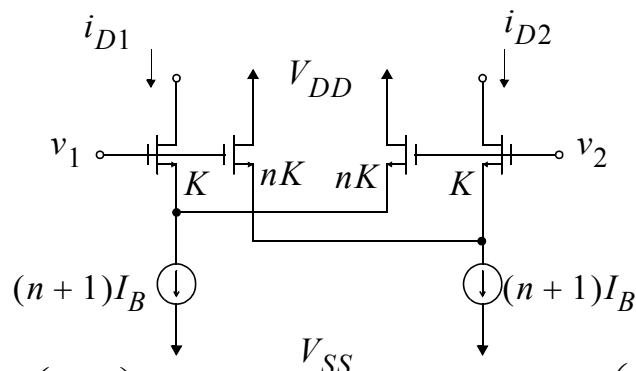
$$v_{GS1} - v_{GS2} = 2(v_1 - v_2) \quad (48)$$

- Finally, output diff current found from (42)

$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2) \quad (49)$$



## Approach #1

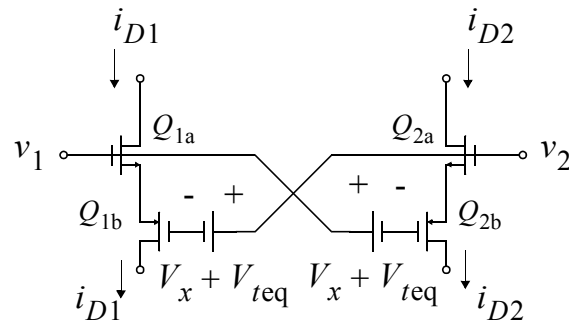


$$(i_{D1} - i_{D2}) = \left(\frac{n}{n+1}\right) 4\sqrt{KI_B}(v_1 - v_2) \quad G_m = \left(\frac{n}{n+1}\right) 4\sqrt{KI_B}$$

- Floating voltage sources built using large transistors ( $n$  times larger with  $n$  typically greater than 5)
- Disadvantage — large bias current and moderate linearity



## Approach #2

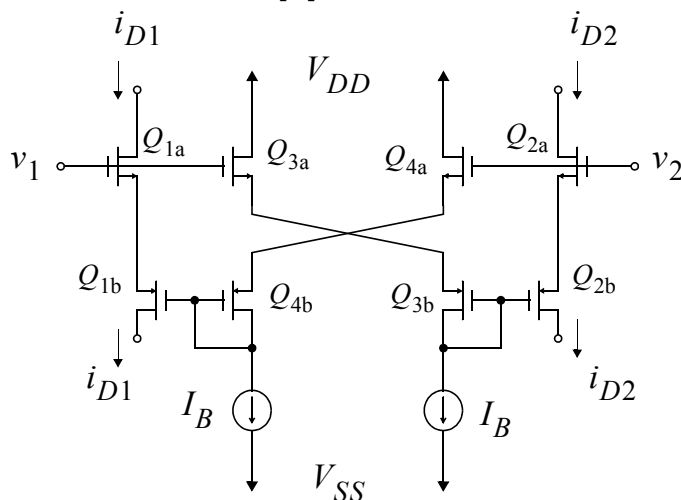


$$(i_{D1} - i_{D2}) = 4K_{eq} V_x (v_1 - v_2)$$

- Replace diff-pair transistors with CMOS pairs
- Now replace floating voltage sources with CMOS pairs



## Approach #2



$$(i_{D1} - i_{D2}) = 4\sqrt{K_{eq} I_B} (v_1 - v_2)$$

$$G_m = 4\sqrt{K_{eq} I_B}$$

- $G_m$  proportional to  $\sqrt{I_B}$
- Requires a large power supply



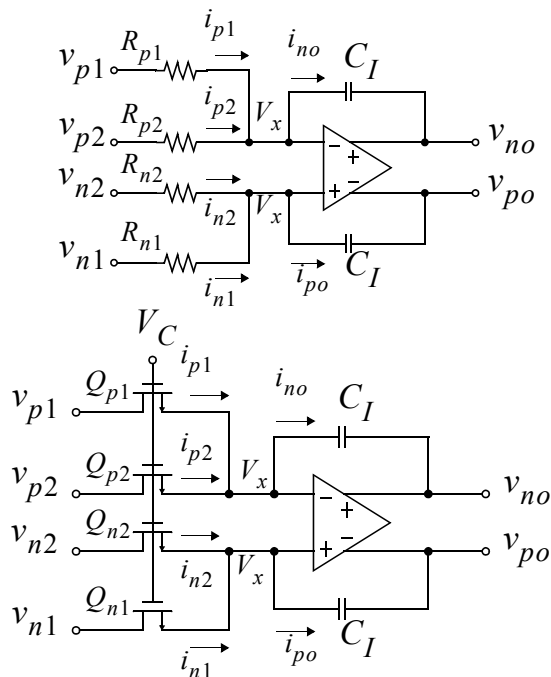


## MOSFET-C Filters

- Gm-C filters are most common but MOSFET-C show promise in BiCMOS where power is important
- MOSFET-C filters similar to active-RC filters but resistors replaced with MOS transistors in triode
- Generally slower than Gm-C filters since opamps capable of driving resistive loads required
- Also rely on Miller integrators



## Two-Transistor Integrators



## Two-Transistor Integrators

- For resistor integrator

$$v_{\text{diff}} = \frac{1}{sR_1C_I}(v_{p1} - v_{n1}) + \frac{1}{sR_2C_I}(v_{p2} - v_{n2}) \quad (53)$$

- Negative integration — cross-couple wires
- For MOSFET-C integrator

$$r_{DS} = \left( \mu_n C_{ox} \left( \frac{W}{L} \right) (v_{GS} - V_{tn}) \right)^{-1} \quad (54)$$

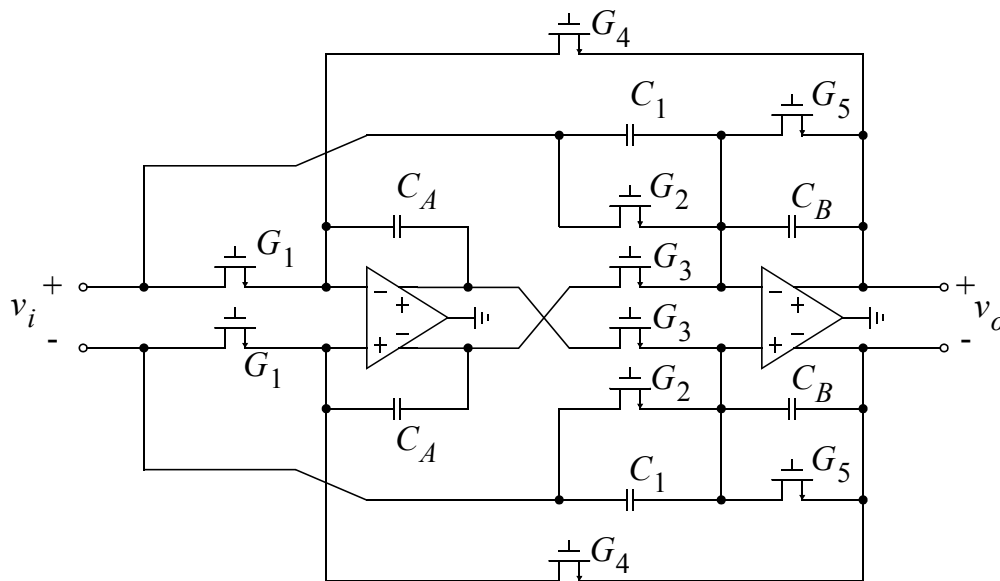
leading to

$$v_{\text{diff}} = \frac{1}{sr_{DS1}C_I}(v_{p1} - v_{n1}) + \frac{1}{sr_{DS2}C_I}(v_{p2} - v_{n2}) \quad (55)$$

$$r_{DSi} = \left( \mu_n C_{ox} \left( \frac{W}{L} \right)_i (V_C - V_x - V_{tn}) \right)^{-1} \quad (56)$$



## MOSFET-C Biquad Filter



## Dynamic Range Performance

- Linearity limits the value of the largest useful signals
- Noise limits the value of the smallest useful signals
- Linearity and noise together determine dynamic range of a filter
- Integrated continuous-time filters are often seriously impaired by their dynamic range performance

### Measures

- Total Harmonic Distortion (THD)
- Third-order intercept point (IP3)
- Spurious-Free Dynamic Range (SFDR)



## Total-Harmonic-Distortion (THD)

$$\text{THD} = 10 \log \left( \frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \dots}{V_f^2} \right) \text{ in dB} \quad (57)$$

- $V_f$  — amplitude of the fundamental
- $V_{hi}$  — amplitude of the  $i$ 'th harmonic component.

$$\text{THD} = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \dots}}{V_f} \times 100 \text{ in \%} \quad (58)$$

- Typically, only power of first few harmonics used since distortion components usually fall off quickly



## THD Limits

- THD will give be optimistic if harmonics fall in stopband
- However, if a lower fundamental frequency is used, then THD is optimistic as distortion often degrades with high input frequencies
- Would like to measure distortion with input signals near the upper passband edge.
- Need an intermodulation test!

### Example

- A 21MHz lowpass filter is being tested
- A 5MHz input signal has harmonics at 10, 15 and 20 but then fall in the stopband
- Want to test the filter with a 20MHz input



## Third-Order Intercept Point (IP3)

- Here IP3 is described as third-order distortion often dominates in fully-diff circuits — can also define IP2
- Consider

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + \dots \quad (59)$$

- The linear term is  $a_1$
- $a_2$ ,  $a_3$ , and  $a_4$  determine second, third and fourth order distortion terms.
- In fully-differential circuits, all even terms small and typically  $a_3$  dominates

$$v_o(t) \approx a_1 v_{in}(t) + a_3 v_{in}^3(t) \quad (60)$$



## Third-Order Intercept Point (IP3)

- If  $v_{in}(t)$  is a sinusoidal

$$v_{in}(t) = A \cos(\omega t) \quad (61)$$

$$v_o(t) \approx a_1 A \cos(\omega t) + \frac{a_3}{4} A^3 (3 \cos(\omega t) + \cos(3\omega t)) \quad (62)$$

- Define  $H_{D1}$  and  $H_{D3}$  to be the amplitudes of the fundamental and third-harmonic terms

$$v_o(t) \equiv H_{D1} \cos(\omega t) + H_{D3} \cos(3\omega t) \quad (63)$$

- Since typically,  $(3/4)a_3 A^3 \ll a_1 A$ , then approximate

$$H_{D1} = a_1 A \quad (64)$$



## Third-Order Intercept Point (IP3)

- Amplitude of third-order term is

$$H_{D3} = \frac{a_3}{4} A^3 \quad (65)$$

- Unfortunately, distortion term lies at  $3\omega t$  for a single sinusoidal input and thus we resort to an intermodulation test
- Consider now

$$v_{in}(t) = A \cos(\omega_1 t) + A \cos(\omega_2 t) \quad (66)$$

- Can show that

$$I_{D1} = a_1 A \quad (67)$$

$$I_{D3} = \frac{3a_3}{4} A^3 \quad (68)$$

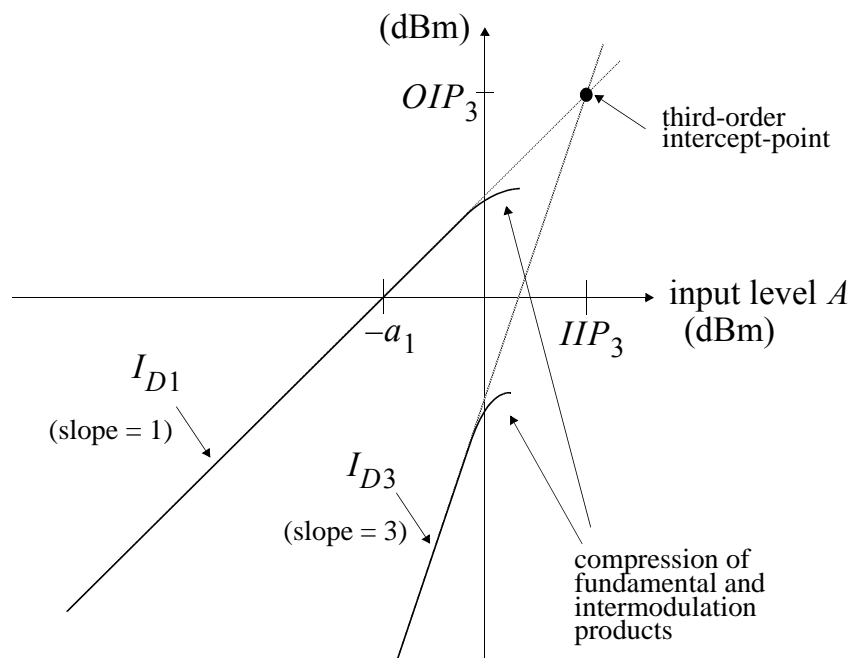


## Third-Order Intercept Point (IP3)

- The fundamental appears at  $\omega_1$  and  $\omega_2$
- The third-order term appears at  $2\omega_2 - \omega_1$  and  $2\omega_1 - \omega_2$
- As  $A$  increased, fundamental rises linearly while third-order term rises as a cubic.
- Every 1dB increase in signal level increases the fundamental by 1dB but the intermod term by 3dB.
- **There is a 2dB worse intermod ratio for every 1dB increase in signal level.**
- Third-order intercept defined to be the point where third-order term will equal fundamental term
- Not physically possible (but an extrapolation) since other distortion terms will start to become important



## Third-Order Intercept Point (IP3)



## Third-Order Intercept Point (IP3)

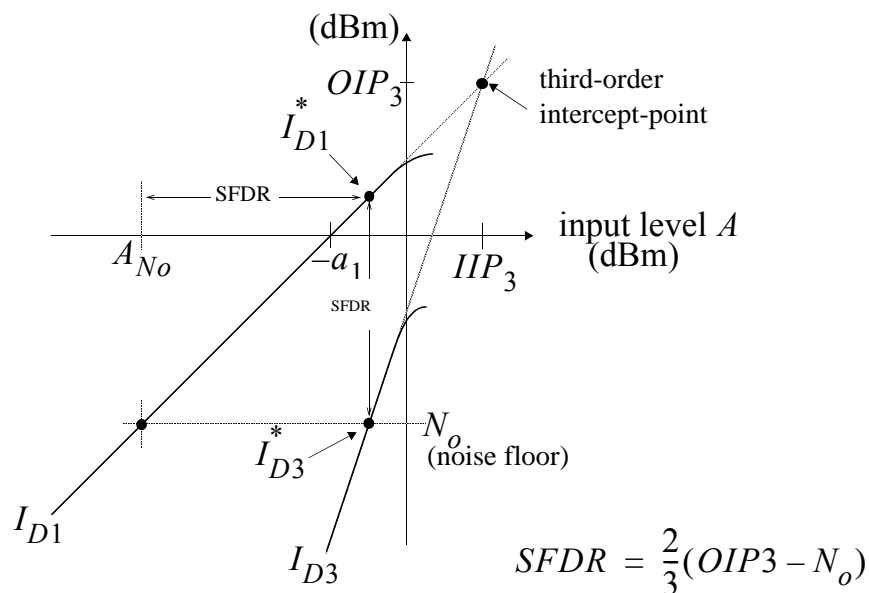
- Knowing IP3 is useful to determine what signal level should be used for a certain intermodulation-ratio

### Example

- If  $OIP_3 = 20dBm$ , what output signal level should be used such that the third-order intermodulation products are  $60dB$  below the fundamental?
- Since we obtain a  $2dB$  improvement for every  $dB$  drop in output signal level and we want a  $60dB$  improvement from the intercept point, we need to lower the output by  $60/2 = 30dB$
- The output level should be  $-10dBm$



## Spurious-Free Dynamic Range (SFDR)



## SFDR

- Spurious-free dynamic range (SFDR) is the SNR when the power of the third-order intermodulation products equals the noise power.
- If the signal is larger, the distortion dominates
- If the signal is smaller, the noise dominates
- Actual dynamic range is 3dB lower since noise and distortion are equal



## Example

- At an input signal level of 0dBm, an intermodulation ratio  $-40dB$  was measured in an filter with a gain of 2dB.
- Since performance worsens by 2dB for each 1dB increase in signal level, the intermodulation ratio will be 0dB at an input level of 20dBm. Therefore,  $IIP3=20dBm$  and  $OIP3=22dBm$
- If one desires an intermodulation ratio of  $-45dB$  then the input should be lowered by 2.5dB or equivalently, it should be at a level of  $-2.5dBm$
- If the noise power at the output is measured to be  $-50dBm$ , the expected SFDR is found by

$$SFDR = \frac{2}{3}(22 + 50) = 48dB \quad (69)$$



## Example

- In other words, the intermod ratio should be 48dB for the distortion power to equal the noise power.
- In intermod of 48dB is obtained for an input signal value of  $-4\text{dBm}$  and an output signal value of  $-2\text{dBm}$
- A higher level implies that the distortion dominates while a lower signal level implies that the noise dominates.
- Signal-to-noise+distortion (SNDR) equals 45dB.

