Advanced Current Mirrors and Opamps

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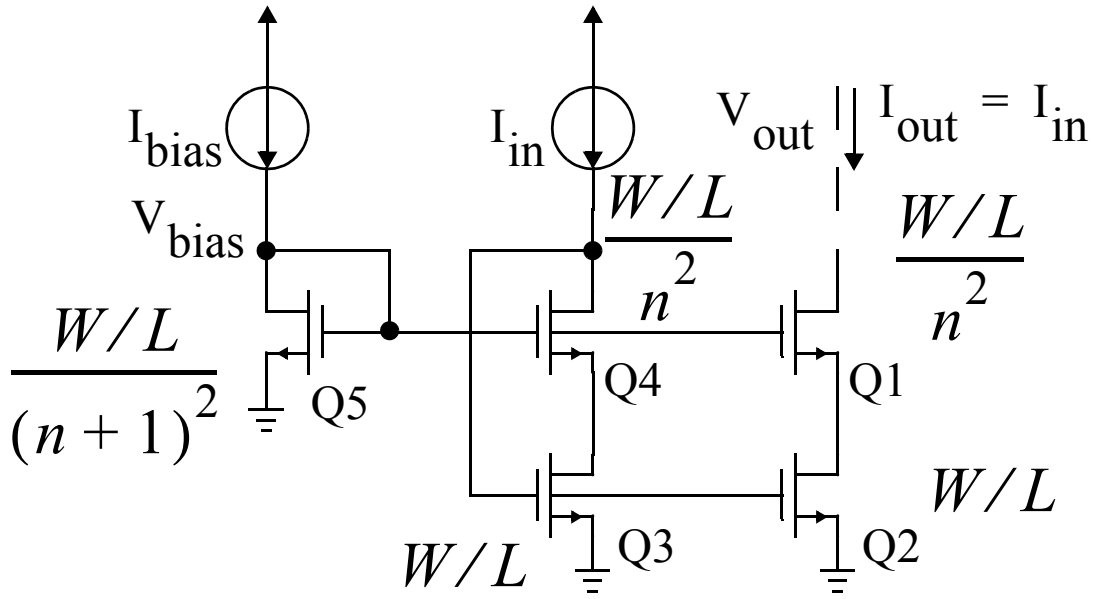
Wide-Swing Current Mirrors



- Used to increase signal swing in cascode mirror
- Bias drains of Q2 and Q3 close to triode region
- I_{bias} set to nominal or max value of I_{in}

Wide-Swing Current Mirrors

- Q3 and Q4 act like a single transistor

$$V_{eff} = V_{eff2} = V_{eff3} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)}} \quad (1)$$

- Q_5 has same drain current but $(n+1)^2$ times smaller

$$V_{eff5} = (n+1)V_{eff} \quad (2)$$

- Similarily

$$V_{eff1} = V_{eff4} = nV_{eff} \quad (3)$$

$$V_{G5} = V_{G4} = V_{G1} = (n+1)V_{eff} + V_{tn} \quad (4)$$

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{eff} + V_{tn}) = V_{eff} \quad (5)$$

- Puts Q2 and Q3 right at edge of triode

Wide-Swing Current Mirrors

- Min allowable output voltage

$$V_{out} > V_{eff1} + V_{eff2} = (n+1)V_{eff} \tag{6}$$

- If $n = 1$

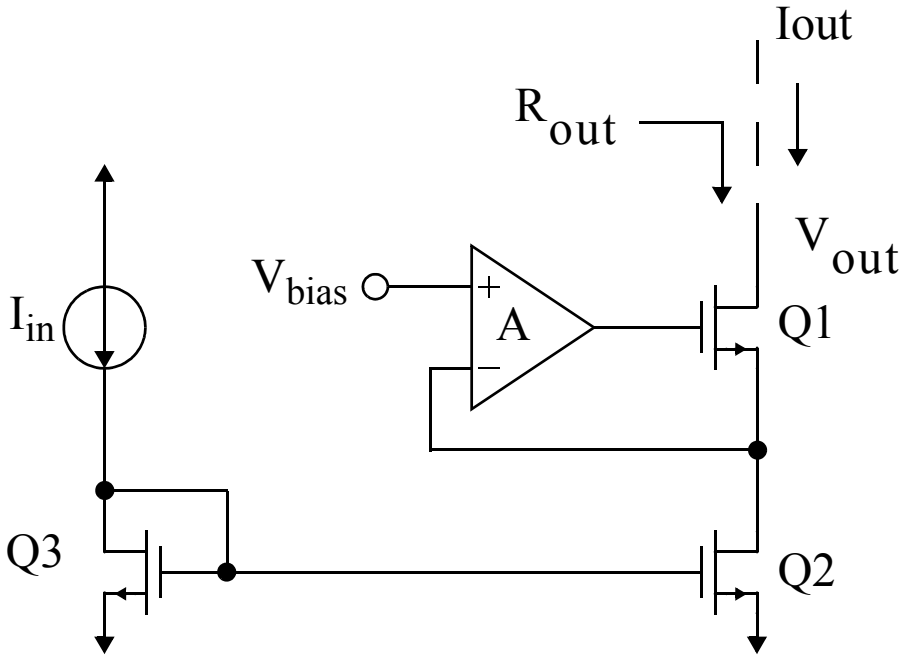
$$V_{out} > 2V_{eff} \tag{7}$$

- With typical value of V_{eff} of 0.2 V, wide-swing mirror can operate down to 0.4 V
- Analyzed with $I_{bias} = I_{in}$. If I_{in} varies, setting I_{bias} to max I_{in} will ensure transistors remain in active region
- Setting I_{bias} to nominal I_{in} will result in low output impedance during slewing (can often be tolerated)

Design Hints

- Usually designer would take $(W/L)_5$ smaller to bias Q_2 and Q_3 slightly larger than minimum
- To save power, bias Q_5 with lower currents while keeping same current densities (and Veff)
- Choose lengths of Q_2 and Q_3 close to minimum allowable gate length (since Vds are quite small)
  — maximizes freq response
- Choose Q_1 and Q_4 to have longer gate lengths since Q_1 often has larger voltages (perhaps twice minimum allowable gate length)
  — Reduces short-channel effects

Enhanced Output-Impedance Current Mirror

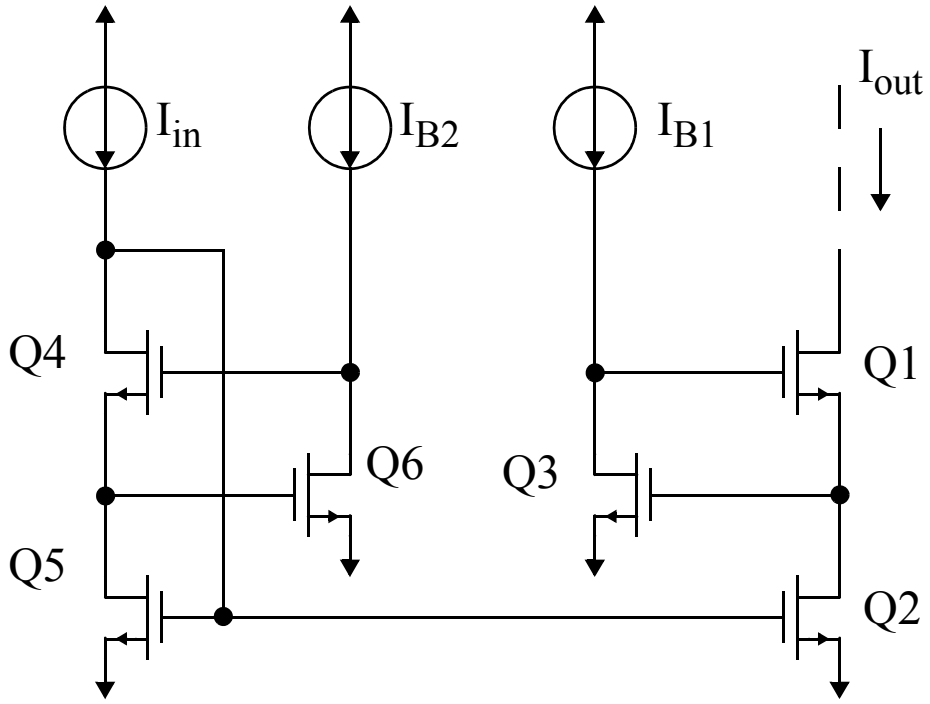


- Use feedback to keep Vds across Q_2 stable

$$R_{out} \cong g_{m1} r_{ds1} r_{ds1} (1 + A) \qquad (8)$$

- Limited by parasitic conductance between drain and substate of Q1

Simplified Enhanced Output-Impedance Mirror



- Rather than build extra opamps, use above
- Feedback amplifier realized by common-source amplifier of Q_3 and current source I_{B1}

Simplified Enhanced Output-Impedance Mirror

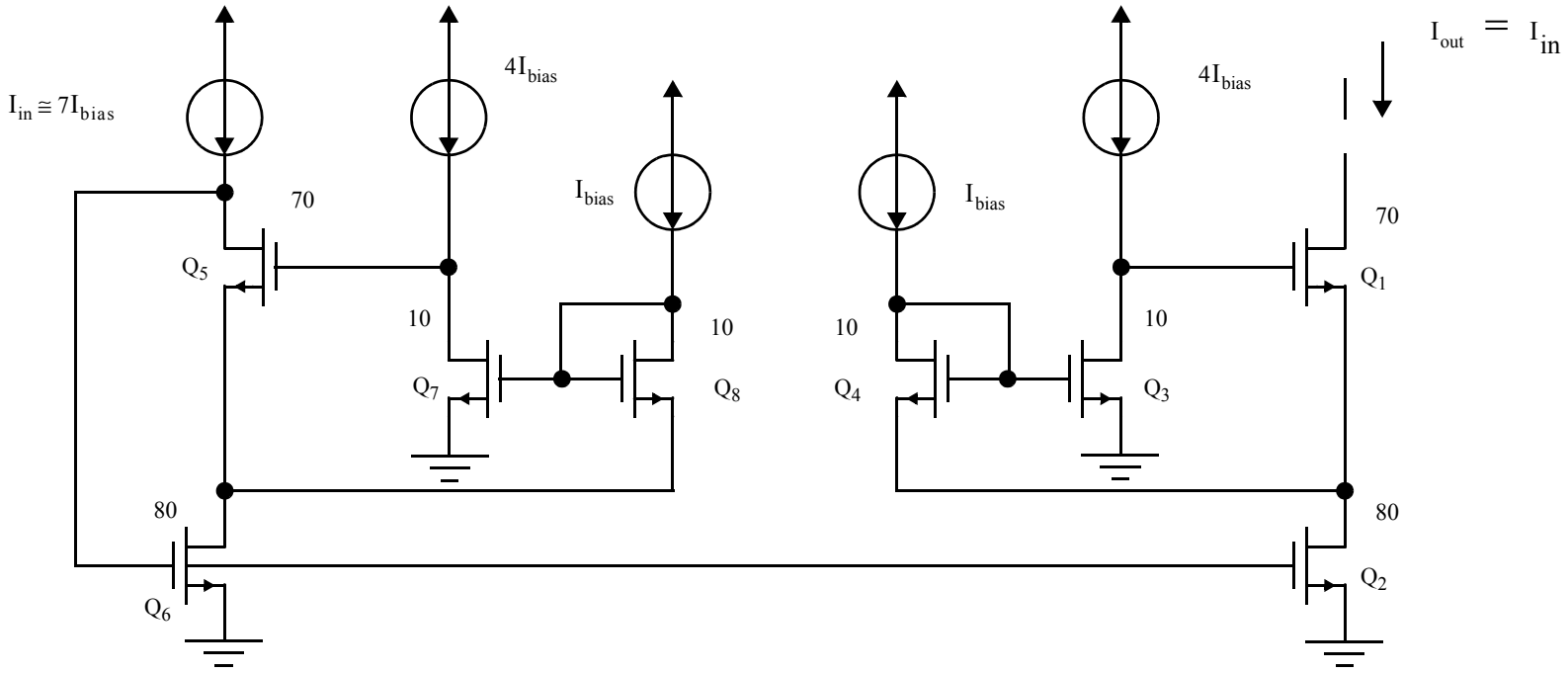
- Assuming output impedance of I_{B1} is equal to r_{ds3}, loop gain will be $(g_{m3}r_{ds3})/2$, resulting in

$$r_{out} \cong \frac{g_{m1}g_{m3}r_{ds1}r_{ds2}r_{ds3}}{2} \tag{9}$$

- Circuit consisting of Q_4, Q_5, Q_6, I_{in}, and I_{B2} operates like a diode-connected transistor — results in accurate matching of I_{out} to I_{in}
- Note that shown circuit is NOT wide-swing — requires output to be $2V_{eff} + V_{tn}$ above lower supply

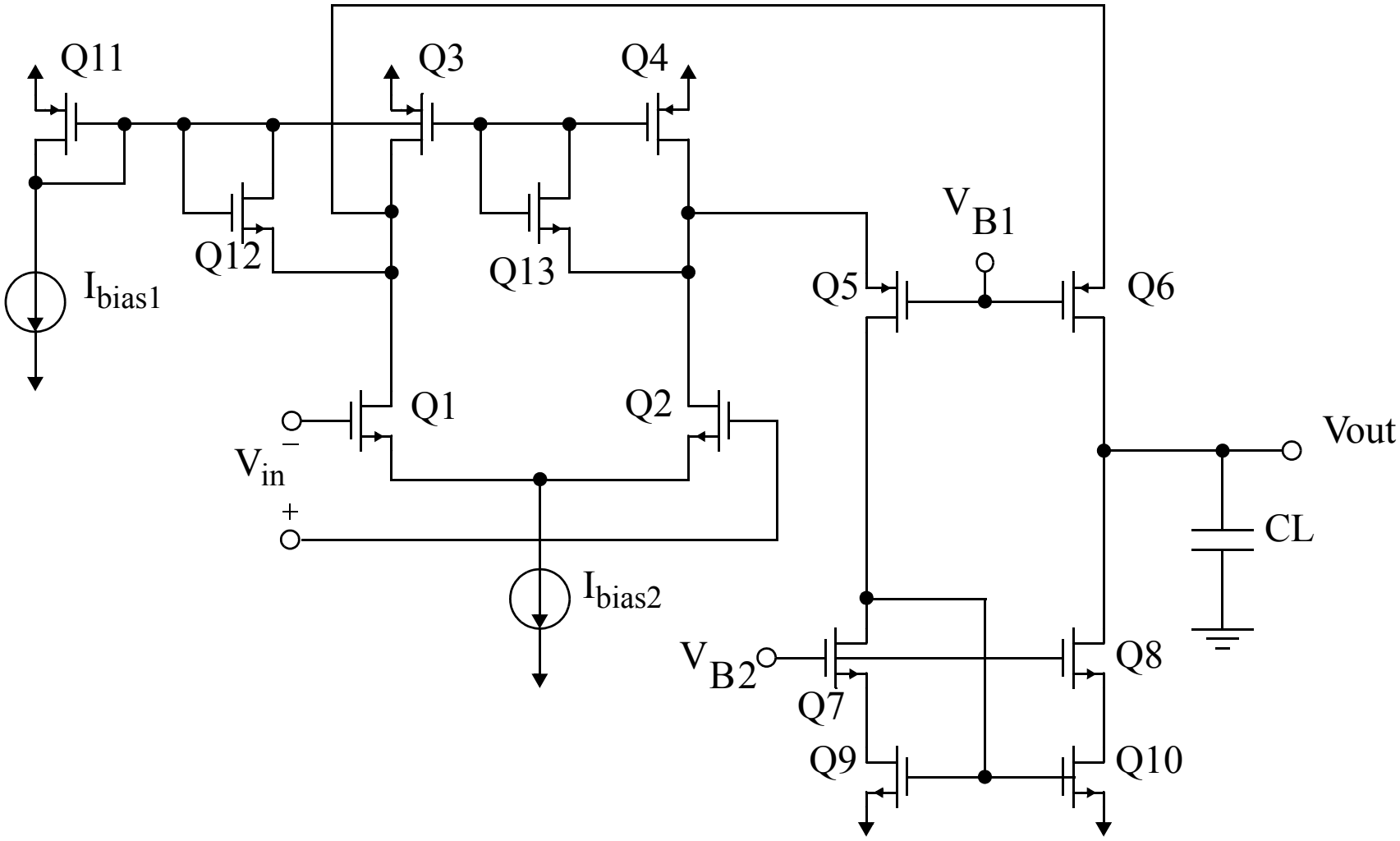
Wide-Swing with Enhanced Output Impedance

- Add wide-swing to improve output voltage swing



- Q3 and Q7 biased at 4 times current density — $2V_{eff}$
- Requires roughly twice power dissipation
- Might need local compensation capacitors

Folded-Cascode Opamp



Folded-Cascode Opamp

- Compensation achieved using load capacitor
- As load increases, opamp slower but more stable
- Useful for driving capacitive loads only
- Large output impedance (not useful for driving resistive loads)
- Single-gain stage but dc gain can still be quite large (say 1,000 to 3,000)
- Shown design makes use of wide-swing mirrors
- Simplified bias circuit shown
- Inclusion of Q12 and Q13 for improved slew-rate

Folded-Cascode Opamp

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s) \tag{10}$$

$$A_V = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L} \tag{11}$$

- r_{out} is output impedance of opamp (roughly $g_m r_{ds}^2 / 2$)
- For mid-band freq, capacitor dominates

$$A_V \cong \frac{g_{m1}}{sC_L} \tag{12}$$

$$\omega_t = \frac{g_{m1}}{C_L} \tag{13}$$

Folded-Cascode Opamp

- Maximizing gm of input maximizes freq response (if not limited by second-poles
- Choose current of input stage larger than output stage (also maximizes dc gain)
- Might go as high as 4:1 ratio
- Large input gm results in better thermal noise
- Second poles due to nodes at sources of Q5 and Q6
- Minimize areas of drains and sources at these nodes with good layout techniques
- For high-freq, increase current in output stage

Folded-Cascode Slew-Rate

- If Q2 turned off due to large input voltage

$$\text{SR} = \frac{I_{\text{D4}}}{\text{C}_{\text{L}}} \tag{14}$$

- But if $I_{\text{bias2}} > I_{D3}$, drain of Q1 pulled near negative power supply
- Would require a long time to recover from slew-rate
- Include Q12 (and Q13) to clamp node closer to positive power supply
- Q12 (and Q13) also dynamically increase bias currents during slew-rate limiting (added benefit)
- They pull more current through Q11 thereby increasing bias current in Q3 and Q4

Folded-Cascode Example

Design Goals

- +-2.5V power supply and 2mW opamp with 4:1 ratio of current in input stage to output stage
- Set bias current in Q11 to be 1/30 of Q3 (or Q4)
- Channel lengths of 1.6um and max width of 300um with Veff=0.25 (except input transistors)
- Load cap = 10pF

Circuit Design

$$I_{\text{total}} = 2(I_{D1} + I_{D6}) = 2(4I_B + I_B) = 10I_B \tag{15}$$

$$I_B = I_{D5} = I_{D6} = \frac{I_{\text{total}}}{10} = \frac{(2mW)/5\ \text{V}}{10} = 40\ \mu\text{A} \tag{16}$$

$$I_{D3} = I_{D4} = 5I_{D5} = 200\ \mu\text{A} \tag{17}$$

$$I_{D1} = I_{D2} = 4I_{D5} = 160\ \mu A \tag{18}$$

- To find transistor sizing:

$$\left(\frac{W}{L}\right)_i = \frac{2I_{Di}}{\mu_i C_{ox} V_{effi}^2} \tag{19}$$

rounding to nearest factor of 10 (and limiting to 300um width) results in

Q_1	300/1.6	Q_6	60/1.6	Q_{11}	10/1.6
Q_2	300/1.6	Q_7	20/1.6	Q_{12}	10/1.6
Q_3	300/1.6	Q_8	20/1.6	Q_{13}	10/1.6
Q_4	300/1.6	Q_9	20/1.6		
Q_5	60/1.6	Q_{10}	20/1.6		

- Widths of Q_{12} and Q_{13} were somewhat arbitrarily chosen to equal the width of Q_{11}
- Transconductance of input transistors

$$g_{m1} = \sqrt{2 I_{D1} \mu_n C_{ox} (W/L)_1} = 2.4 \text{ mA/V} \quad (20)$$

- Unity-gain frequency

$$\omega_t = \frac{g_{m1}}{C_L} = 2.4 \times 10^8 \text{ rad/s} \Rightarrow f_t = 38 \text{ MHz} \quad (21)$$

- Slew rate ***without*** clamp transistors

$$\text{SR} = \frac{I_{D4}}{C_L} = 20 \text{ V/}\mu\text{s} \quad (22)$$

- Slew rate ***with*** clamp transistors

$$I_{D12} + I_{D3} = I_{bias2} = 320 \ \mu\text{A} \quad (23)$$

$$I_{D3} = 30 I_{D11} \quad (24)$$

$$I_{D11} = 6.6 \ \mu\text{A} + I_{D12} \quad (25)$$

- Solving above results in

$$I_{D11} = 10.53\ \mu A \tag{26}$$

which implies

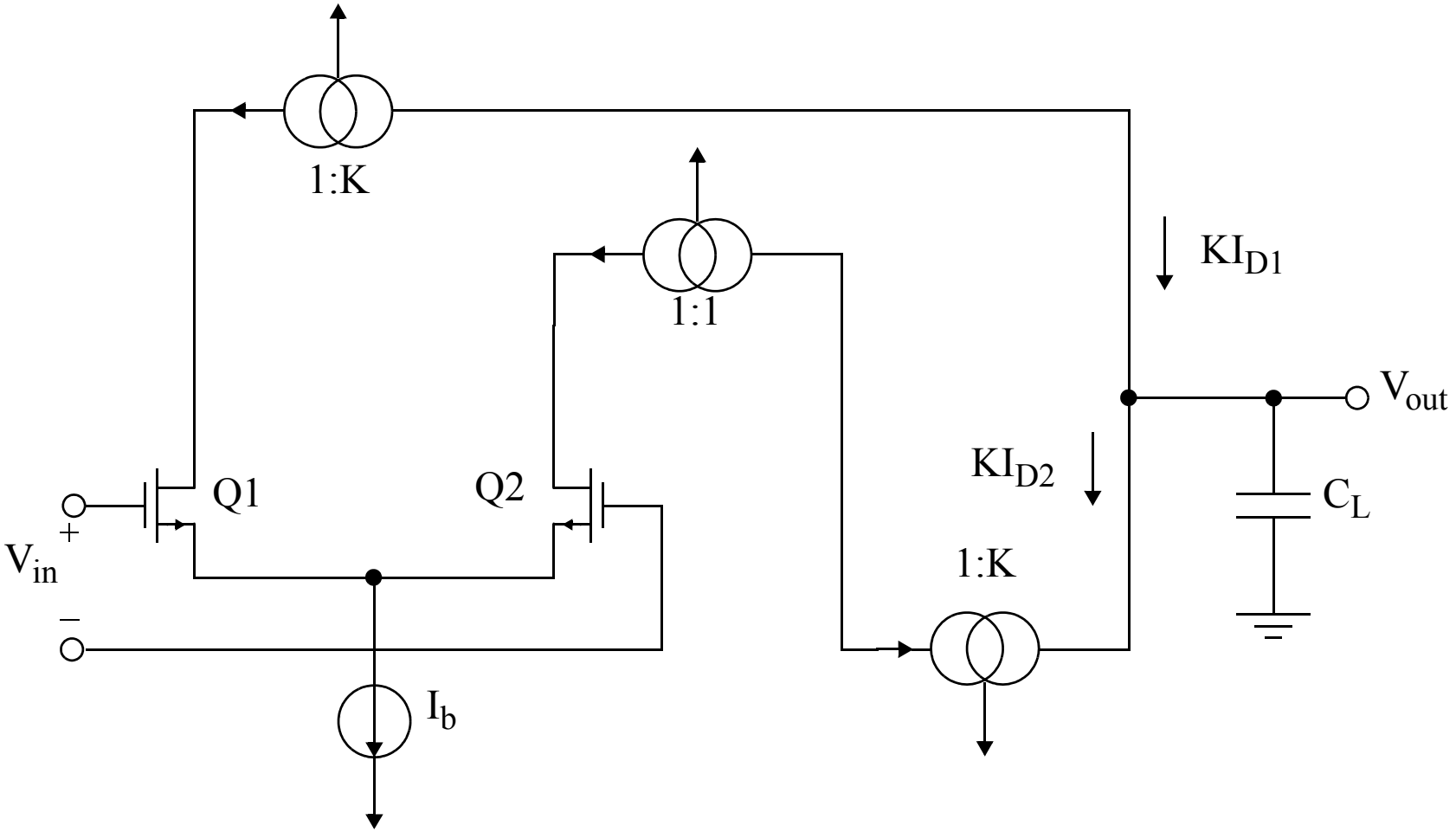
$$I_{D3} = I_{D4} = 30 I_{D11} = 0.32\ mA \tag{27}$$

leading to slew-rate

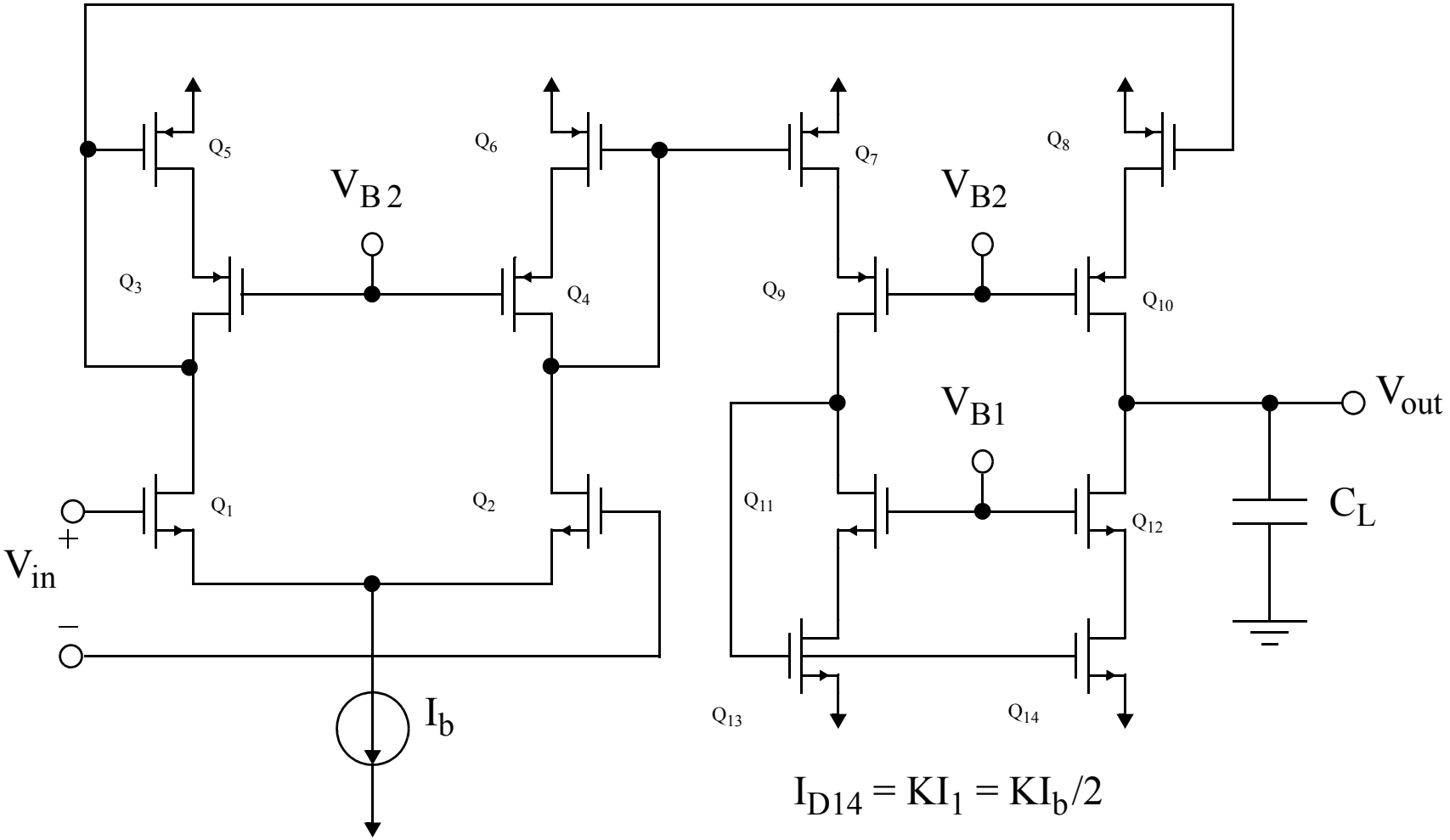
$$SR = \frac{I_{D4}}{C_L} = 32\ V/\mu s \tag{28}$$

- More importantly, time to recover from slew-rate limiting is decreased.

Current-Mirror Opamp



Current-Mirror with Wide-Swing Cascodes



$$I_{D14} = KI_1 = KI_b/2$$

Current-Mirror Opamp

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = Kg_{m1}Z_L(s) = \frac{Kg_{m1}r_{out}}{1 + sr_{out}C_L} \cong \frac{Kg_{m1}}{sC_L} \qquad (29)$$

- K factor is the current gain from mirrors

$$\omega_t = \frac{Kg_{m1}}{C_L} = \frac{K\sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1}}{C_L} \qquad (30)$$

- If output capacitance set max speed, higher K results in higher speed
- If second-poles set max speed, higher K results in lower speed (increases capacitances of nodes)
- A reasonable choice for a general-purpose opamp is $K = 2$ (for max speed, $K = 1$)

Current-Mirror Opamp Slew-Rate

$$SR = \frac{KI_b}{C_L} \tag{31}$$

- For given power, SR maximized by large K
- Example: $K = 4$ results in 4/5 of total bias current used in charging C_L
- Usually has better SR than folded-cascode
- Usually has better bandwidth than folded-cascode
- Folded-cascode has better thermal noise

Current-Mirror Opamp Example

Design goals

Same as in folded-cascode. Use K=2

Circuit Design

- With 2mW power limit and 5V supply, $I_{\text{total}} = 400\ \mu\text{A}$

$$I_{\text{total}} = (3 + K)I_{D1} \tag{32}$$

$$I_{D1\text{-}7} = I_{D9} = I_{D11} = I_{D13} = 80\ \mu\text{A} \tag{33}$$

$$I_{D8} = I_{D10} = I_{D12} = I_{D14} = 160\ \mu\text{A} \tag{34}$$

$$I_b = 160\ \mu\text{A} \tag{35}$$

and setting V_{eff} around 0.25V, we find transistor sizes...

- Resulting in:

Q_1	300/1.6	Q_7	60/1.6	Q_{13}	30/1.6
Q_2	300/1.6	Q_8	120/1.6	Q_{14}	60/1.6
Q_3	60/1.6	Q_9	60/1.6		
Q_4	60/1.6	Q_{10}	120/1.6		
Q_5	60/1.6	Q_{11}	30/1.6		
Q_6	60/1.6	Q_{12}	60/1.6		

$$g_{m1} = \sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1} = 1.7 \text{ mA/V} \tag{36}$$

$$\omega_t = \frac{Kg_{m1}}{C_L} = 3.4\times10^8 \text{rad/s} \Rightarrow f_t = 54 \text{ MHz} \tag{37}$$

$$SR = (KI_b)/C_L = 32 \text{ V/}\mu\text{s} \tag{38}$$

- which is better than 20 V/μs for the folded-cascode opamp without clamp transistors

Linear Settling Time

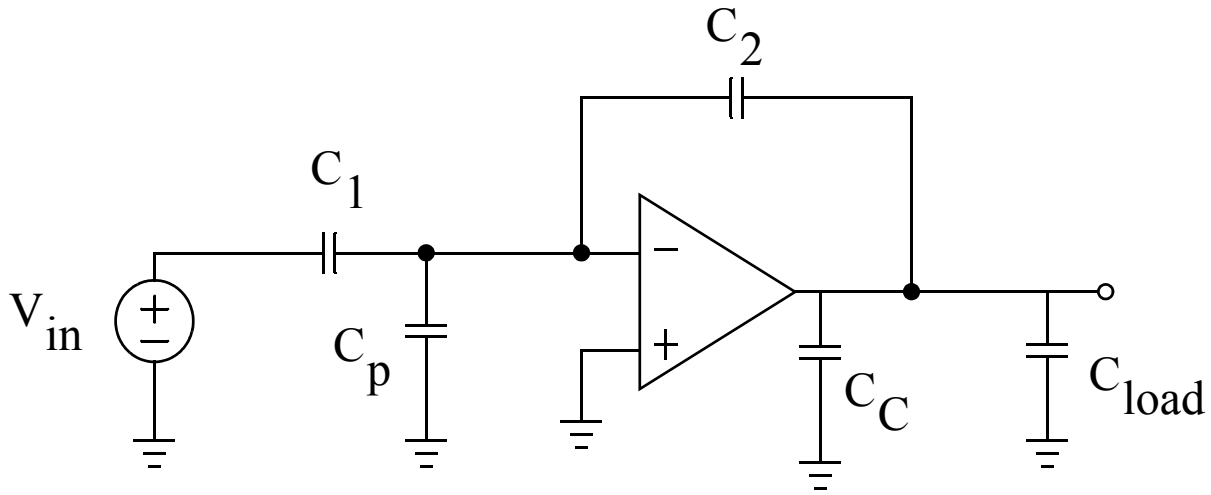
- Time constant for linear settling time equals inverse of closed-loop 3dB freq, ω_{3dB} where

$$\omega_{3dB} = \beta\omega_t \tag{39}$$

  where β is feedback factor and ω_t is unity-gain freq of amplifier (not including feedback factor)

- For 2-stage opamp, ω_t is relatively independent of load capacitance
- This is NOT the case where load capacitor is compensation capacitor (folded-cascode and current-mirror opamps)
- Need to find equivalent load capacitance

Linear Settling Time



$$\beta = \frac{1/[s(C_1 + C_p)]}{1/[s(C_1 + C_p)] + 1/(sC_2)} = \frac{C_2}{C_1 + C_p + C_2} \tag{40}$$

$$C_L = C_C + C_{load} + \frac{C_2(C_1 + C_p)}{C_1 + C_p + C_2} \tag{41}$$

Linear Settling Time Example

- Given $C_1 = C_2 = C_C = C_{load} = 5$ pF and $C_p = 0.46$ pF, find settling time for 0.1 percent accuracy (i.e. 7τ) for the current-mirror opamp

Solution:

- Equivalent load capacitance

$$C_L = 5 + 5 + \frac{5(5 + 0.46)}{5 + 5 + 0.46} = 12.61 \text{ pF} \tag{42}$$

which results in a unity gain freq of

$$\omega_t = \frac{Kg_{m1}}{C_L} = \frac{2 \times 1.7 \text{ mA/V}}{12.61 \text{ pF}} = 2.70 \times 10^8 \text{ rad/s} \tag{43}$$

Linear Settling Time Example

- Feedback factor given by

$$\beta = \frac{5}{5 + 0.46 + 5} = 0.48 \tag{44}$$

causing a first-order time constant

$$\tau = \frac{1}{\beta \omega_t} = 7.8 \text{ ns} \tag{45}$$

- For 0.1 percent accuracy, we need a linear settling time of 7τ or 54 ns.

- This does not account for any slew-rate limiting time.

Fully Differential Opamps

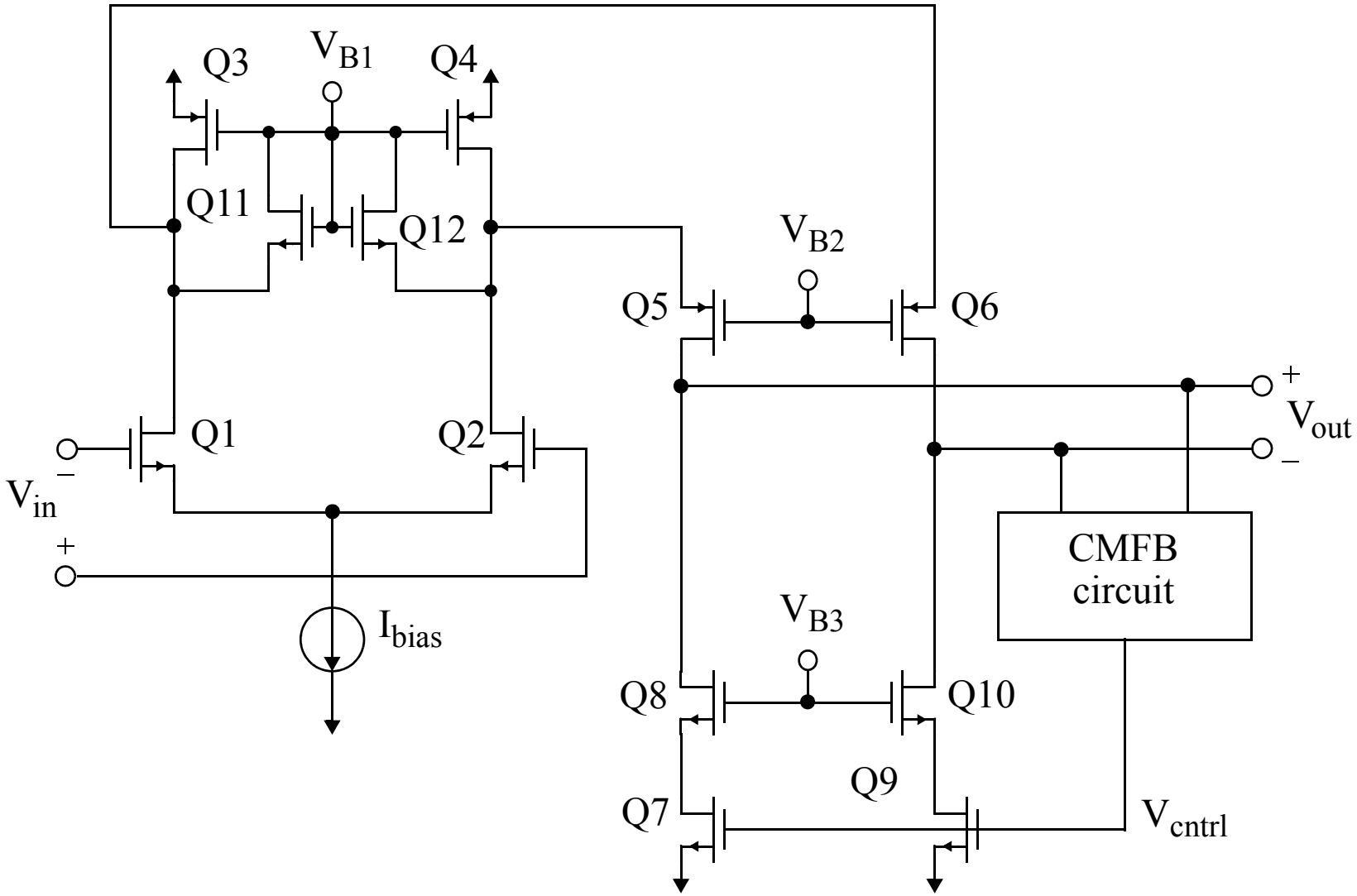
Advantages

- Use of fully-differential signals helps to reject common-mode noise and even-order linearities
  — rejection only partial due to non-linearities but much better than single-ended designs
- Fast since no extra current mirror needed

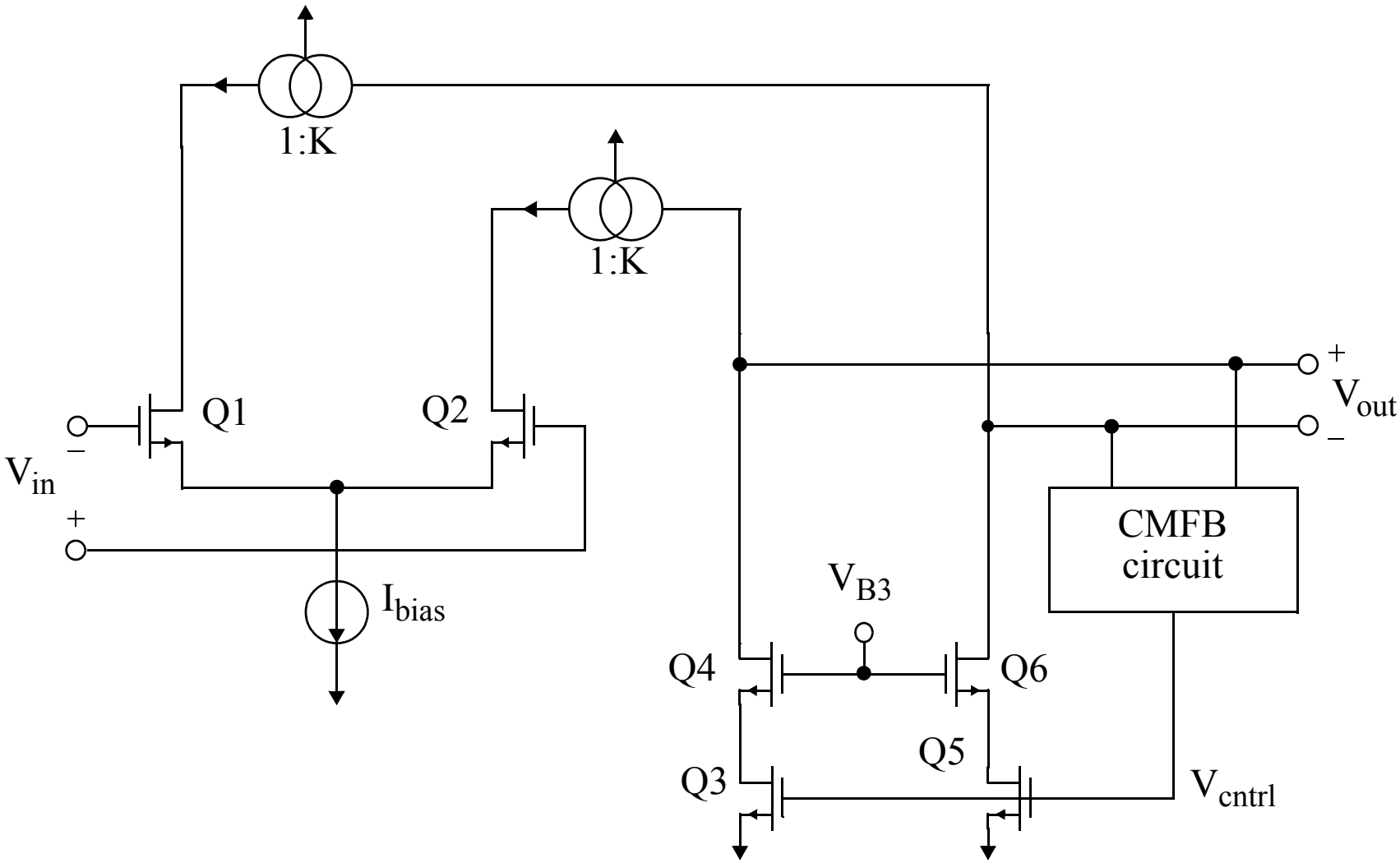
Disadvantages

- Requires common-mode feedback (CMFB) circuitry
  — sets average output voltage level, should be fast
  — adds some capacitance to output stage
  — might limit output signal swing
- Negative going single-ended slew-rate slower since set by bias current — not dynamic

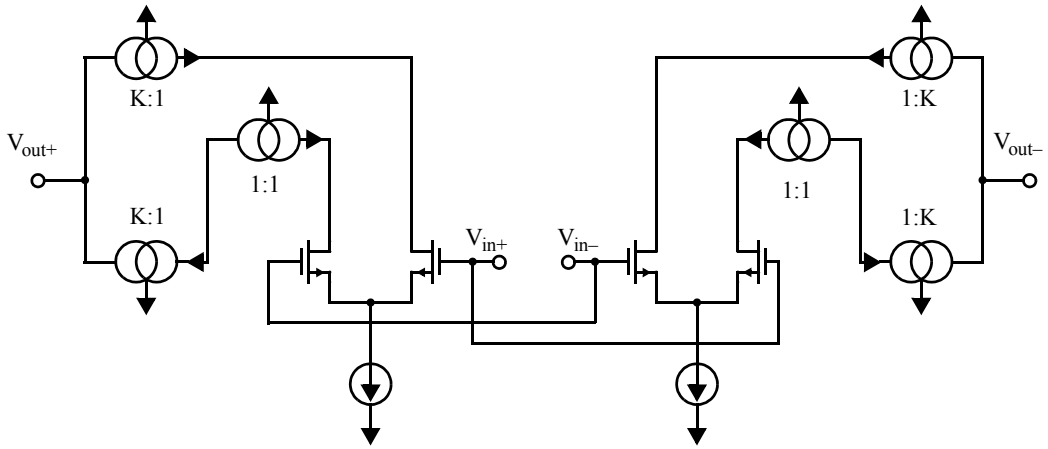
Fully Differential Folded-Cascode Opamp



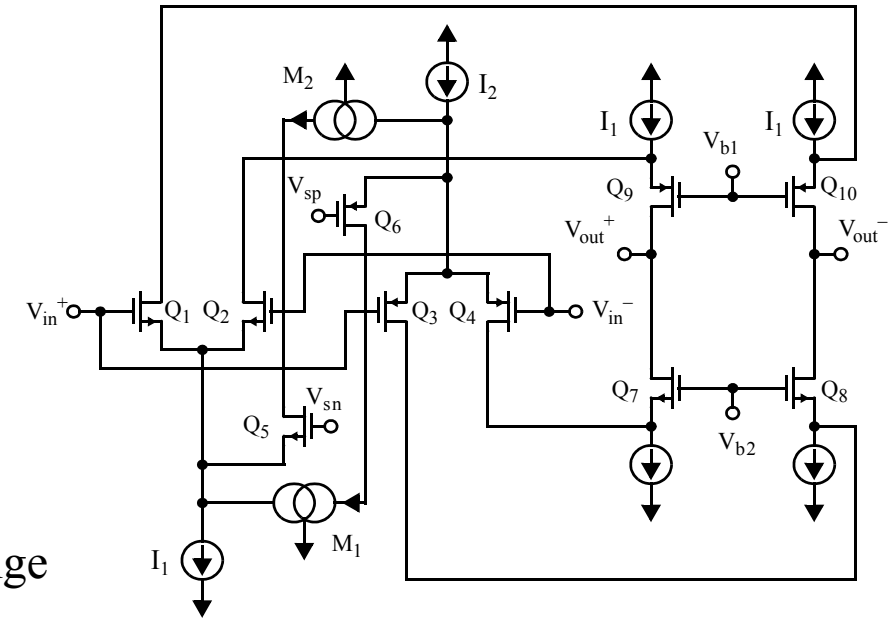
Fully-Diff Current-Mirror Opamp



Other Fully-Diff Opamps

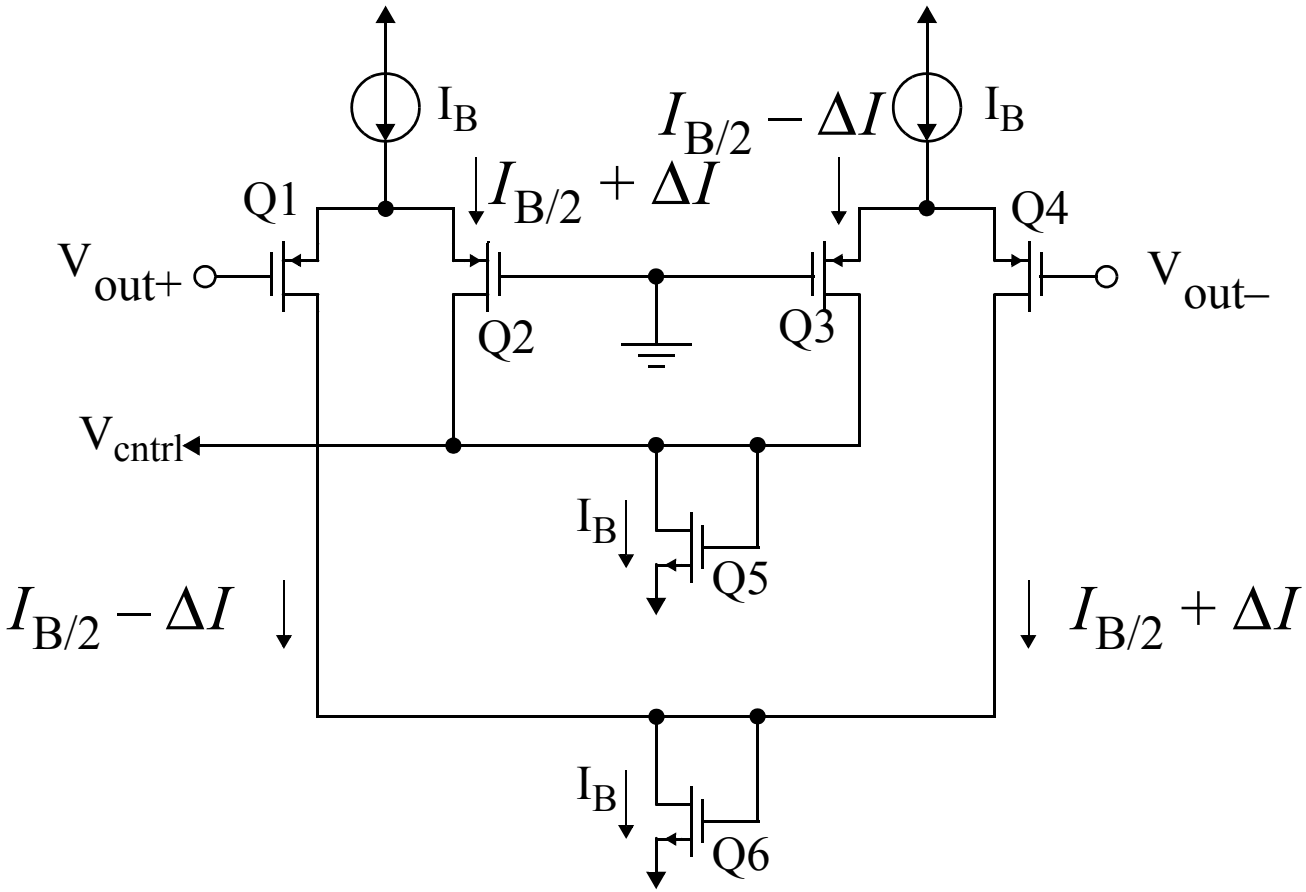


Using 2 single-ended opamps



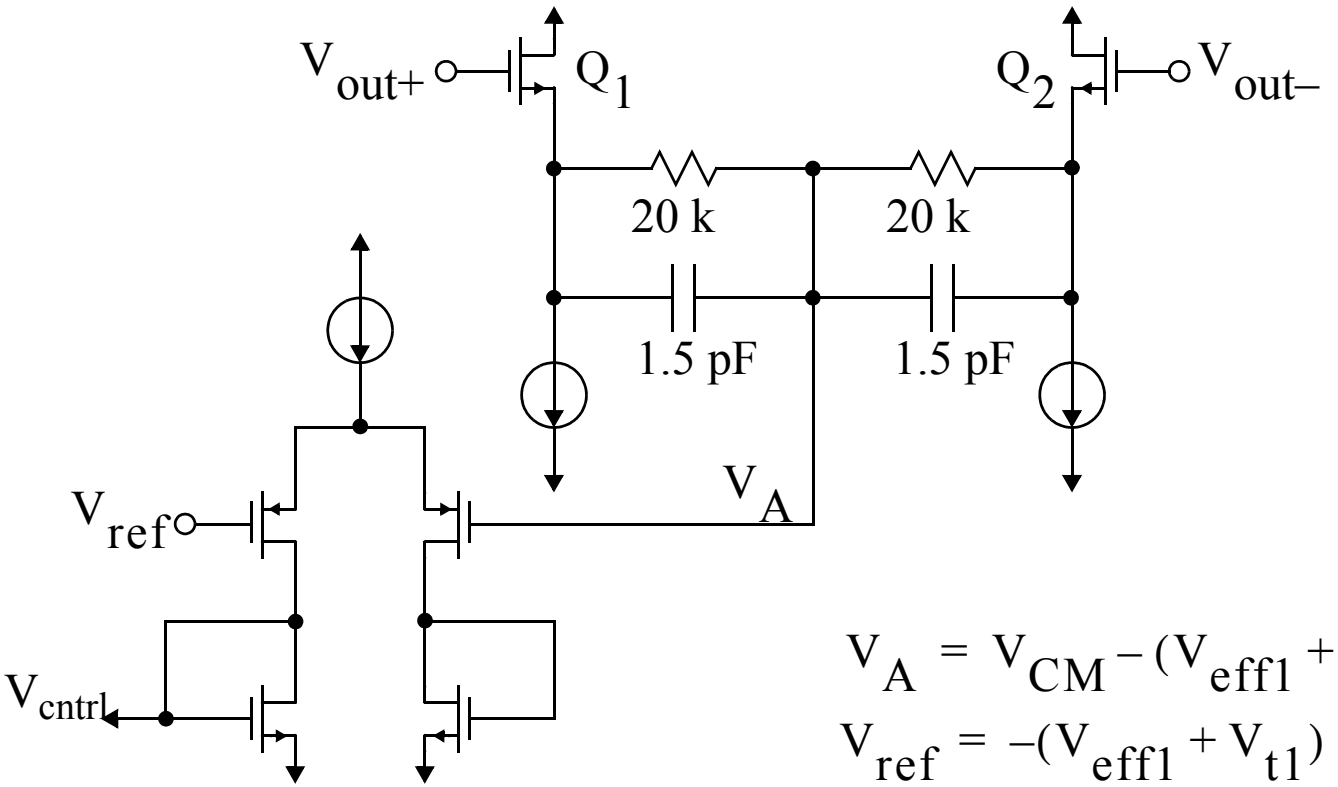
Rail-to-rail input common-mode range

Common-Mode Feedback Circuits



- Balanced signal on Vout does not affect Vcntrl
- Does not depend on small-signal analysis

Common-Mode Feedback Circuits

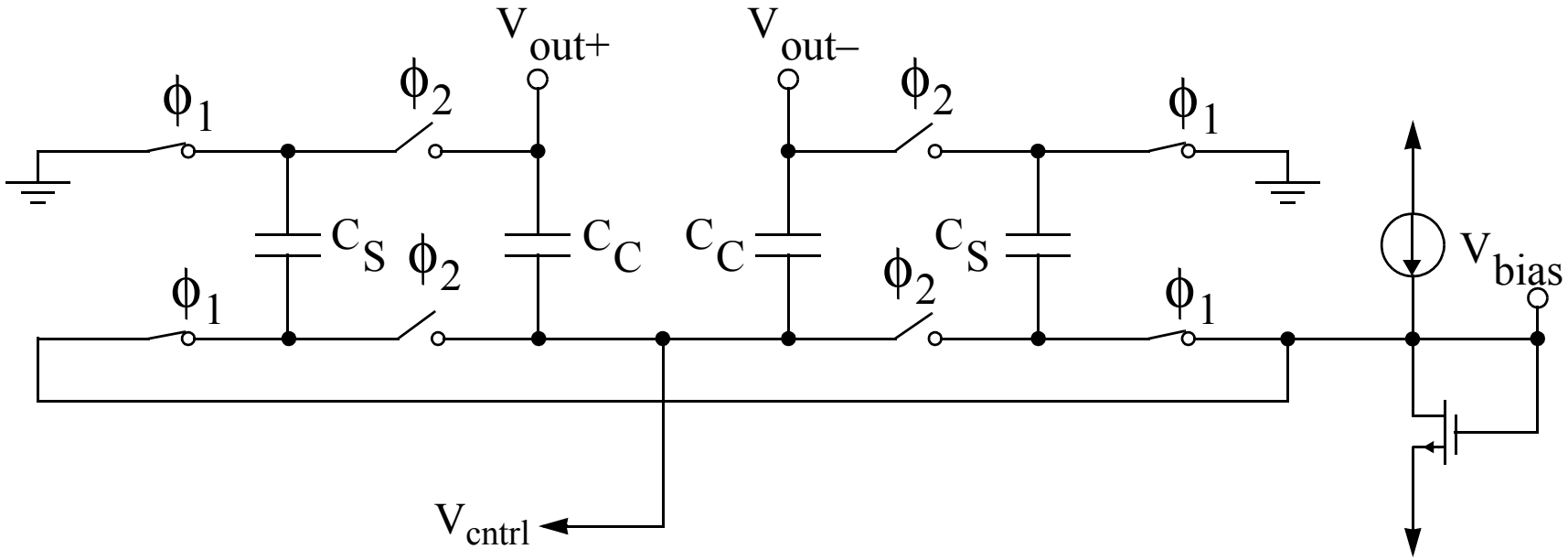


$$V_A = V_{CM} - (V_{eff1} + V_{t1})$$

$$V_{ref} = -(V_{eff1} + V_{t1})$$

- Limited differential swing
- Should ensure CMFB loop is stable

Common-Mode Feedback Circuits



- Useful for switched-capacitor circuits
- Caps Cs set nominal dc bias at bottom of Cc
- Large output signal swing allowed