# Phase-Locked Loops

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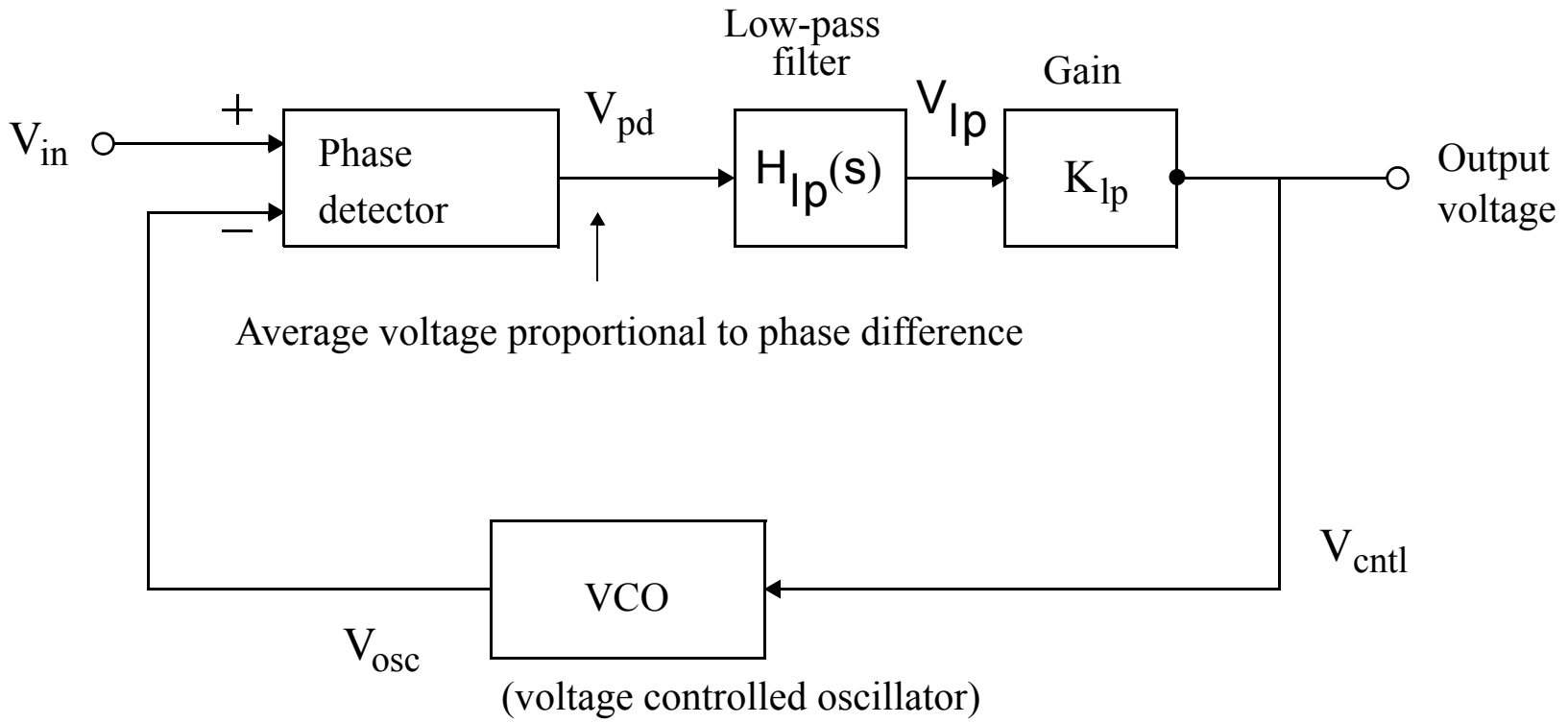
# Common PLL Applications

- **Clock multiplier**
  - input is a fixed frequency clock
  - output is a higher frequency clock signal that is a multiple of input clock frequency
- **Frequency synthesizer**
  - input is a fixed frequency clock
  - output is a clock signal with arbitrary frequency
- **Clock and data recovery**
  - input is a data signal (from a serial link)
  - output is digital data as well as clock signal
  - phase detector is different than other applications
- **FM demodulation**
  - input is a radio signal
  - output is demodulated signal

# PLL Basic Architecture




- In general, output may be $V_{cntl}$ or $V_{osc}$

# PLL Basics

- Feedback causes $V_{\text{in}}$ to be phase locked to $V_{\text{osc}}$
- We start with a simple phase detector of ...

$$V_{pd} = K_M V_{in} V_{osc} \tag{1}$$

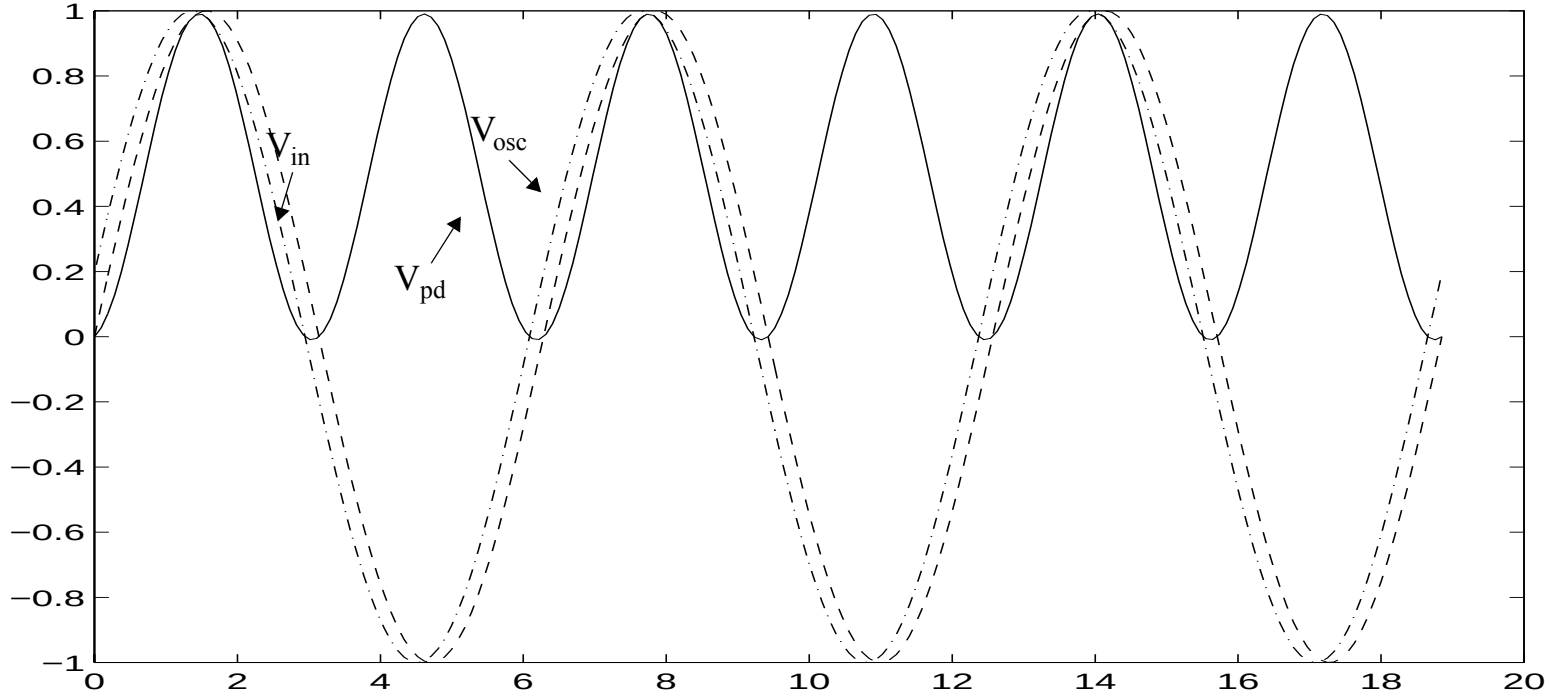
$K_M$ is a multiplication constant

- Also assume filter is ...

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p} \tag{2}$$

which is a lead-lag filter. Usually $\tau_z \ll \tau_p$

# Example Waveforms




$$V_{in} = E_{in} \sin(\omega t) \tag{3}$$

$$V_{osc} = E_{osc} \sin(\omega t - \phi_d + 90°) = E_{osc} \cos(\omega t - \phi_d) \tag{4}$$

- Above shows an example of $\phi_d \approx 90$ (slightly less)

# PLL Basics

- Can show

$$V_{pd} = K_M \frac{E_{in}E_{osc}}{2}[\sin(\phi_d) + \sin(2\omega t - \phi_d)] \quad (5)$$

- The lowpass filter removes second term and for small $\phi_d$ ...

$$V_{cntl} \cong K_{lp}K_M \frac{E_{in}E_{osc}}{2}\phi_d = K_{lp}K_{pd}\phi_d \quad (6)$$

where we define

$$K_{pd} = K_M \frac{E_{in}E_{osc}}{2} \quad (7)$$

# PLL Basics

- Oscillator frequency given by

$$\omega_{osc} = K_{osc} V_{\text{cntl}} + \omega_{fr} \tag{8}$$

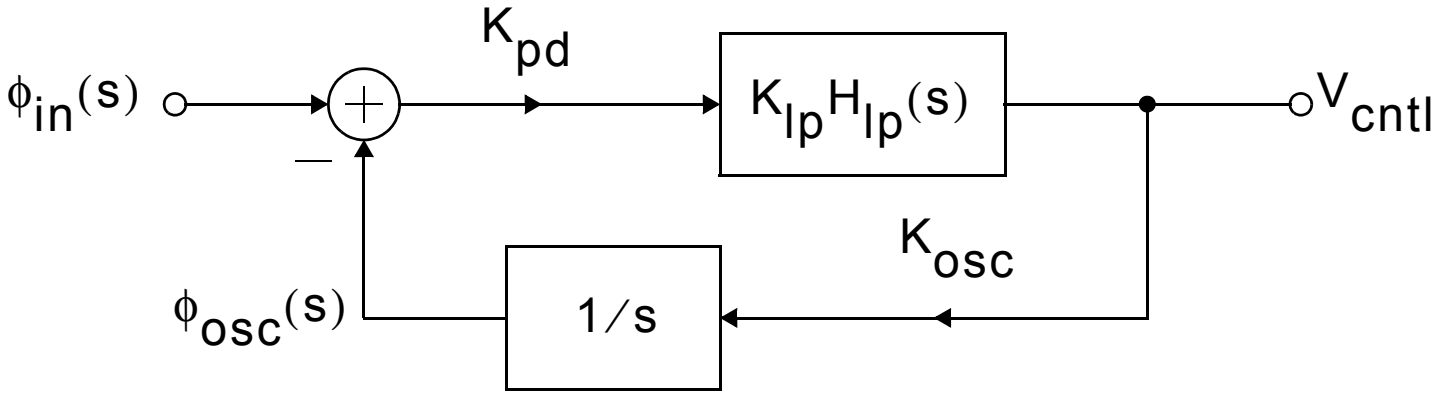
  $\omega_{fr}$ is the free running freq of oscillator

  $K_{osc}$ is the VCO gain constant

- Feedback forces $\omega_{osc}$ to equal $\omega_{in}$
- However, if $\omega_{in}$ does not equal $\omega_{fr}$, and loop filter does NOT have infinite gain at dc, then phase difference when in lock given by:

$$\phi_d = \frac{V_{\text{cntl}}}{K_{lp} K_{pd}} = \frac{\omega_{\text{in}} - \omega_{\text{fr}}}{K_{lp} K_{pd} K_{\text{osc}}} \tag{9}$$

# PLL Linear Model




$$V_{\text{cntl}}(s) = K_{pd}K_{lp}H_{lp}(s)[\phi_{in}(s) - \phi_{osc}(s)] \tag{10}$$

$$\phi_{osc}(s) = \frac{K_{osc}V_{\text{cntl}}(s)}{s} \tag{11}$$

# PLL Equations

- Combining above 2 equations ...

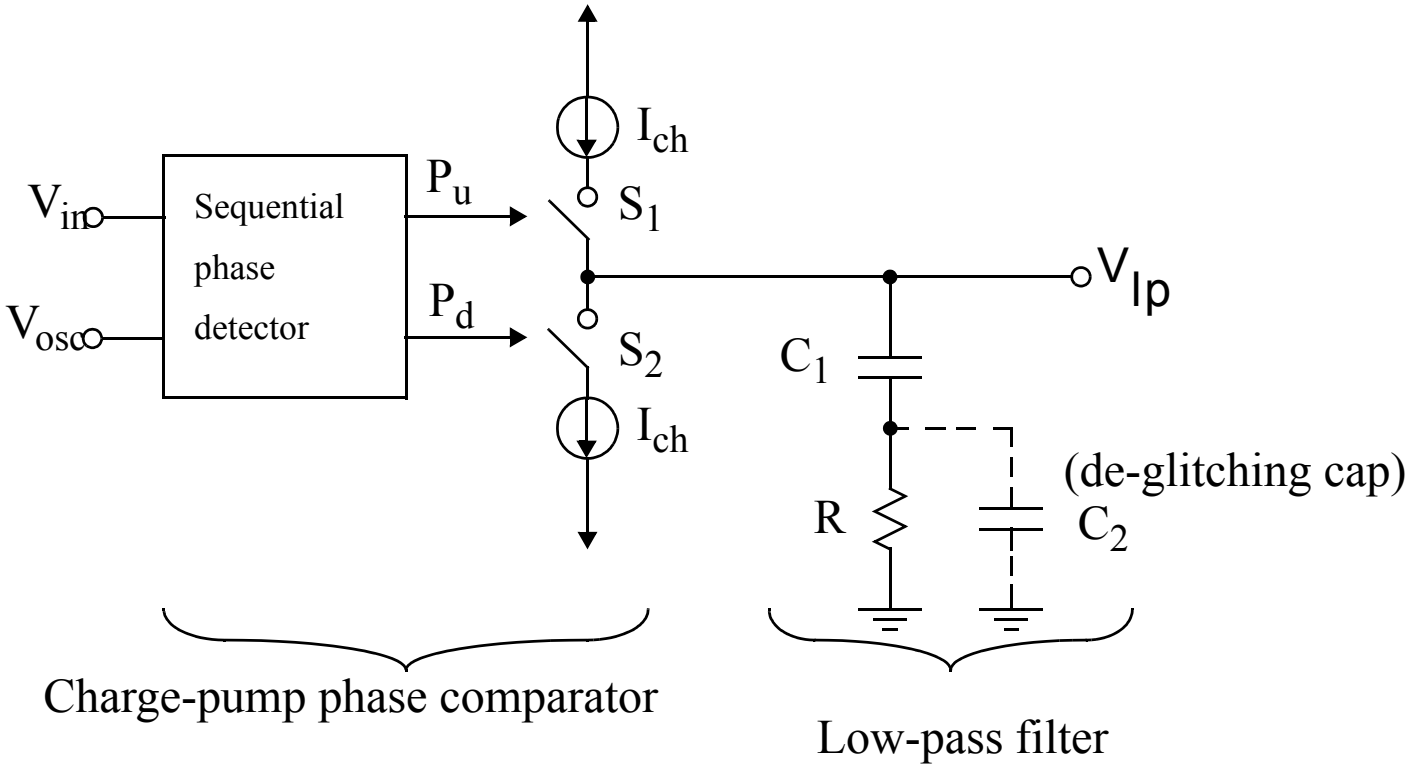
$$\frac{V_{\text{cntl}}(s)}{\phi_{in}(s)} = \frac{sK_{pd}K_{lp}H_{lp}(s)}{s + K_{pd}K_{lp}K_{\text{osc}}H_{lp}(s)} \tag{12}$$

- This is a highpass response from input phase to control voltage
- Can also be written as

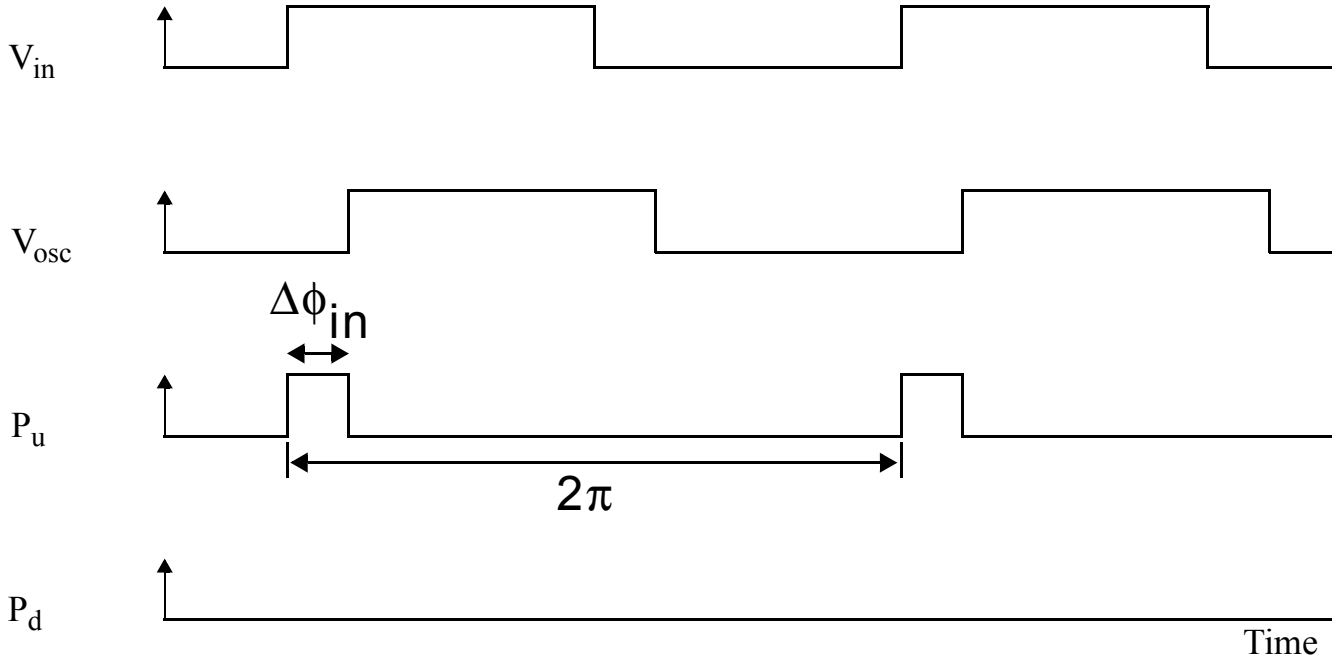
$$\frac{\phi_{\text{osc}}(s)}{\phi_{\text{in}}(s)} = \frac{K_{\text{pd}}K_{\text{lp}}K_{\text{osc}}H_{\text{lp}}(s)}{s + K_{\text{pd}}K_{\text{lp}}K_{\text{osc}}H_{\text{lp}}(s)} \tag{13}$$

- This is a lowpass response from input phase to output phase

# Charge Pump PLL



# Sequential Phase Detector




- If $V_{in}$ leads $V_{osc}$, $P_u$ (pulse up) goes high for lead time
- If $V_{osc}$ leads $V_{in}$, $P_d$ (pulse down) goes high for lead time.

# Charge Pump PLL Equations

- Average current flowing into lowpass filter is ...

$$I_{avg} = \frac{\Delta\phi_{in}}{2\pi} I_{ch} \tag{14}$$

- Lowpass filter is (ignoring $C_2$)...

$$H_{lp}(s) = \frac{V_{lp}(s)}{I_{avg}(s)} = R + \frac{1}{sC_1} = \frac{1 + sRC_1}{sC_1} \tag{15}$$

- which results in

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{(1 + sRC_1)}{1 + sRC_1 + \dfrac{s^2 C_1}{K_{pd} K_{osc}}} \tag{16}$$

# Charge Pump PLL Equations

- The phase transfer curve is second-order (ignores de-glitching cap $C_2$) so $\omega_0$ and $Q$ can be found as

$$\omega_0 = \frac{1}{\tau_{pll}} = \sqrt{\frac{I_{\text{ch}} K_{osc}}{2\pi C_1}} \tag{17}$$

$$Q = \frac{1}{RC_1\omega_0} = \frac{1}{R}\sqrt{\frac{2\pi}{C_1 \mathrm{I}_{ch} K_{\text{osc}}}} \tag{18}$$

# Charge Pump Example

- Let $K_{osc} = 2\pi \times 50\ M\text{rad}/V$ and $I_{ch} = 10\ \mu\text{A}$.
- $\omega_{fr} = 2\pi \times 50\ M\text{rad}/s$ . Desired loop time constant of 100 cycles, or 2 μs. Find loop filter components.

**SOLUTION**

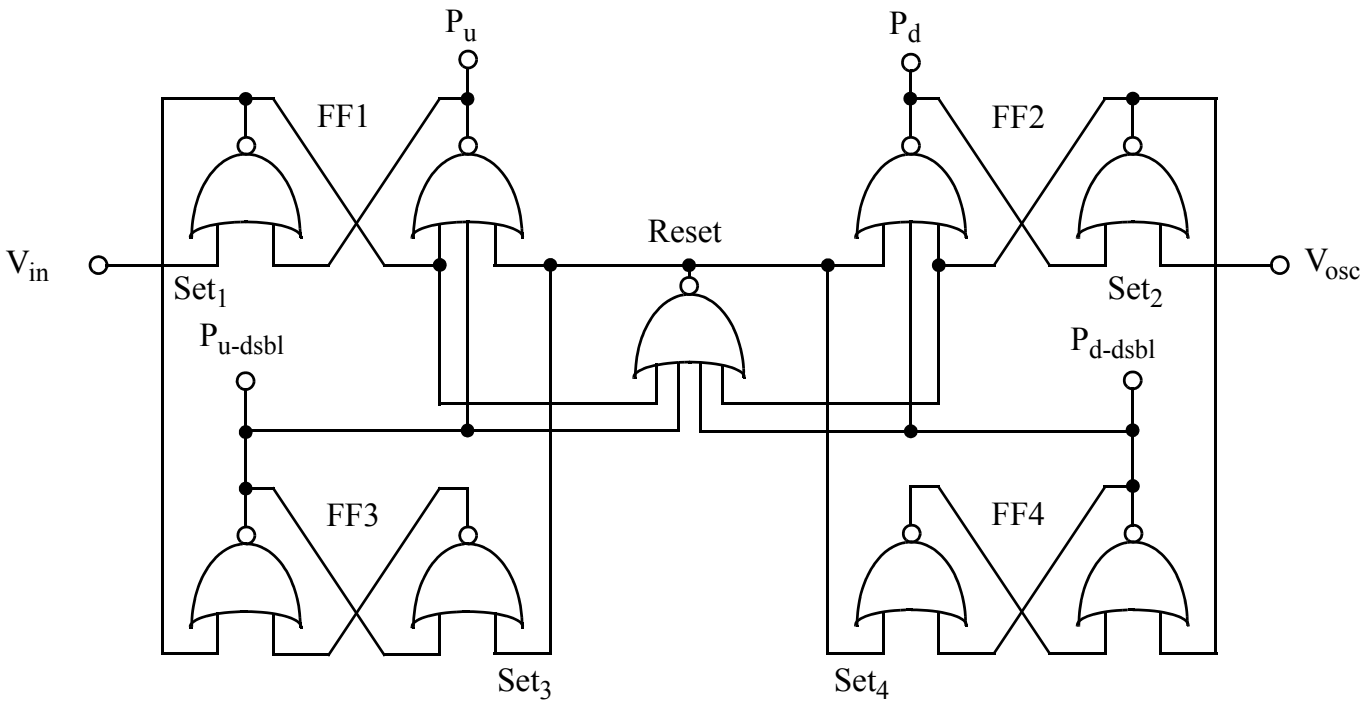
$$\omega_0 = \frac{1}{2\ \mu\text{s}} = 500\ \text{krad}/\text{s} \tag{19}$$

$$C_1 = \frac{1}{\omega_0^2}\frac{I_{ch}}{2\pi}K_{osc} = 2\ \text{nF} \tag{20}$$

- Let $C_2 = C_1/10 = 2.5\ \text{pF}$ and $Q = 0.4$

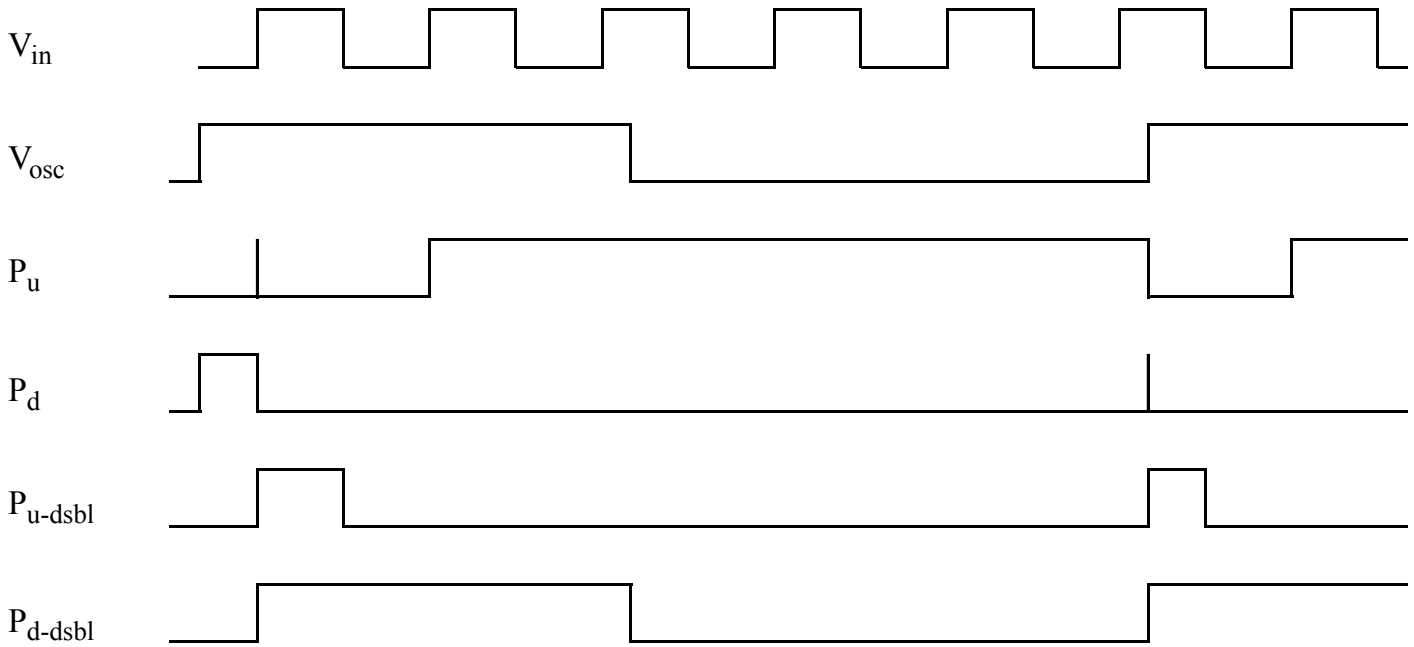
$$R = \frac{1}{Q}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}} = 31.4\ k\Omega \tag{21}$$

# Phase Frequency Detector



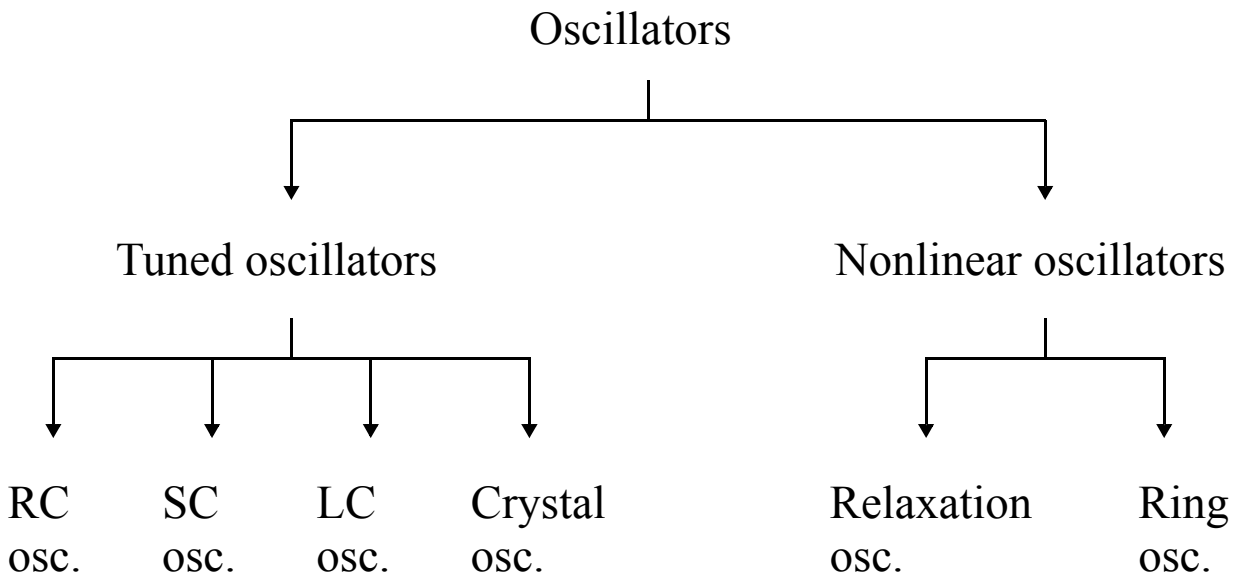

- Can be used for sequential phase detector but also works when large frequency differences between osc freq and input freq

# Phase Frequency Detector



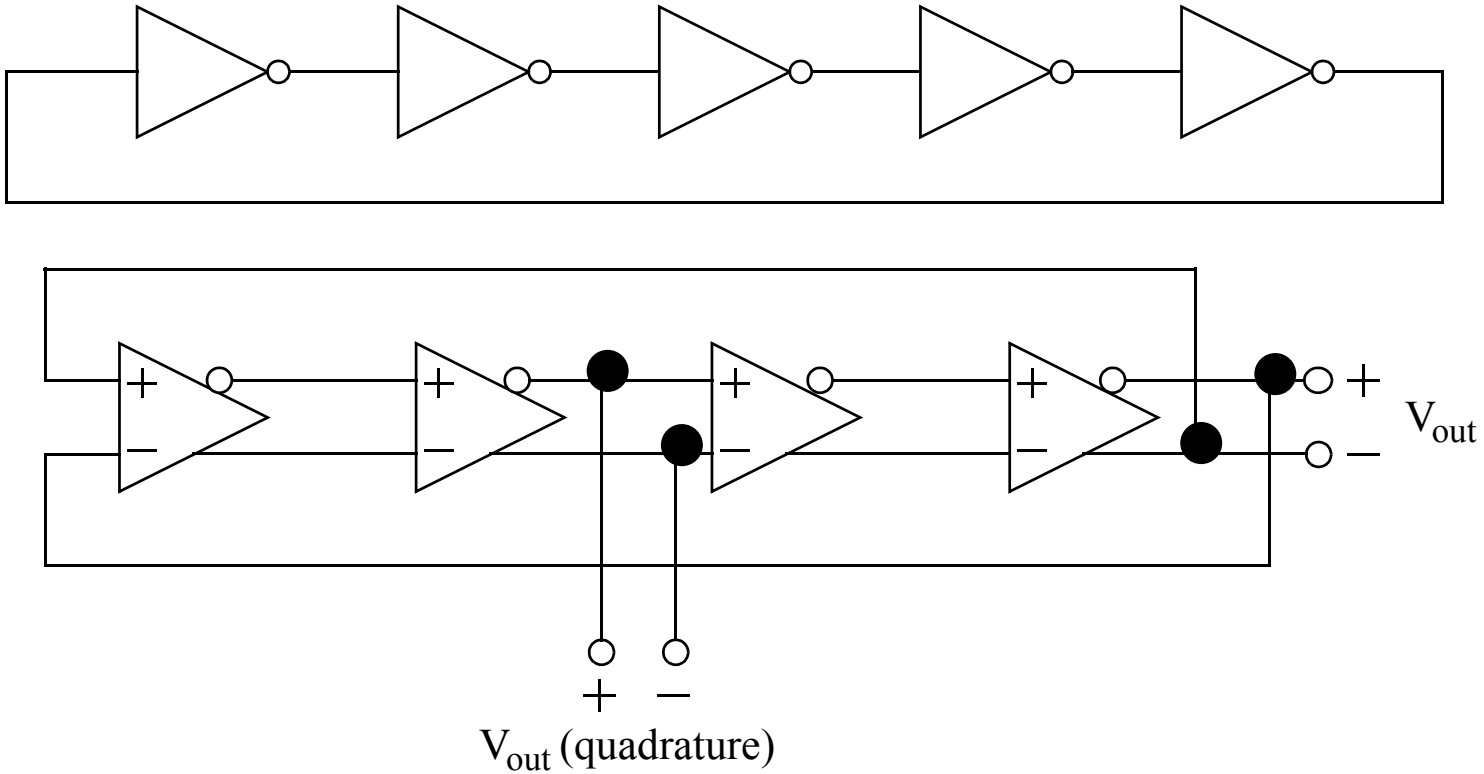

- Above example is for osc freq much lower than input freq
- Note that $P_u$ is high much longer than $P_d$

# Oscillators




- Two main classes of oscillators
- Most common are LC osc and Ring osc (Crystal osc is good but difficult to tune away from center freq)

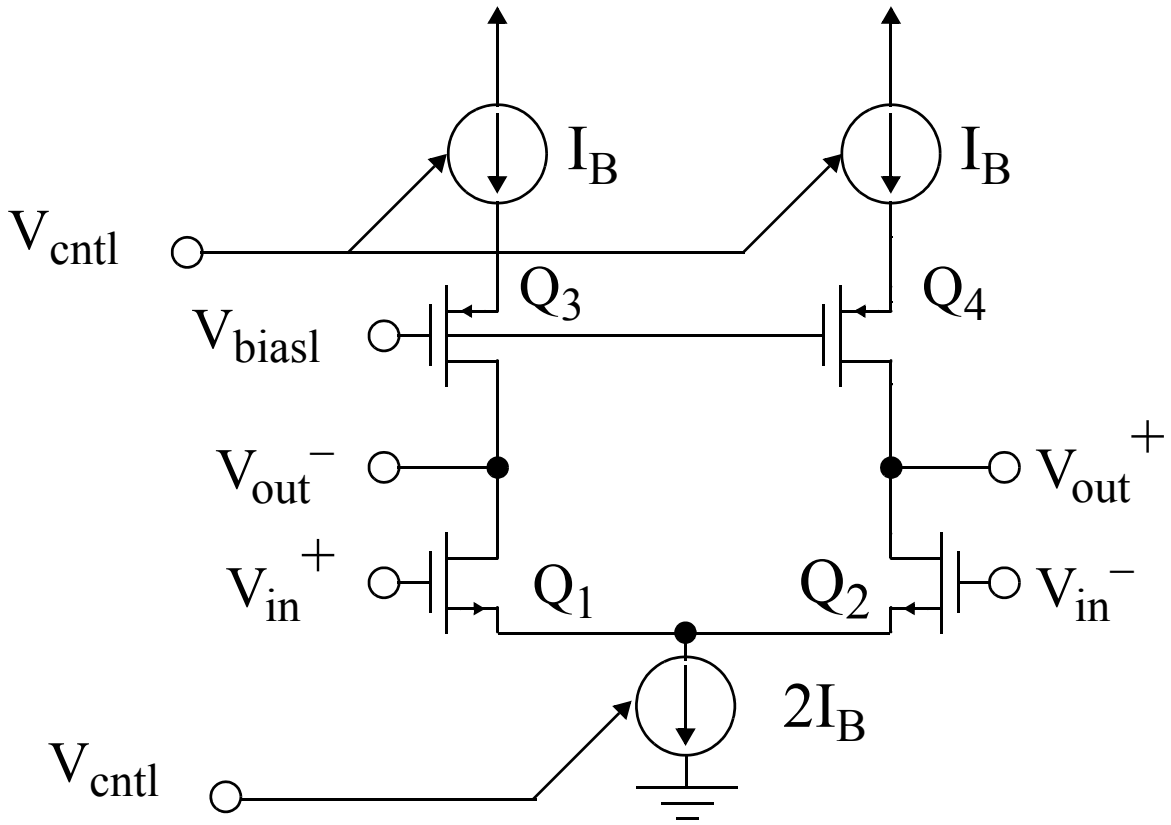
# Ring Oscillators



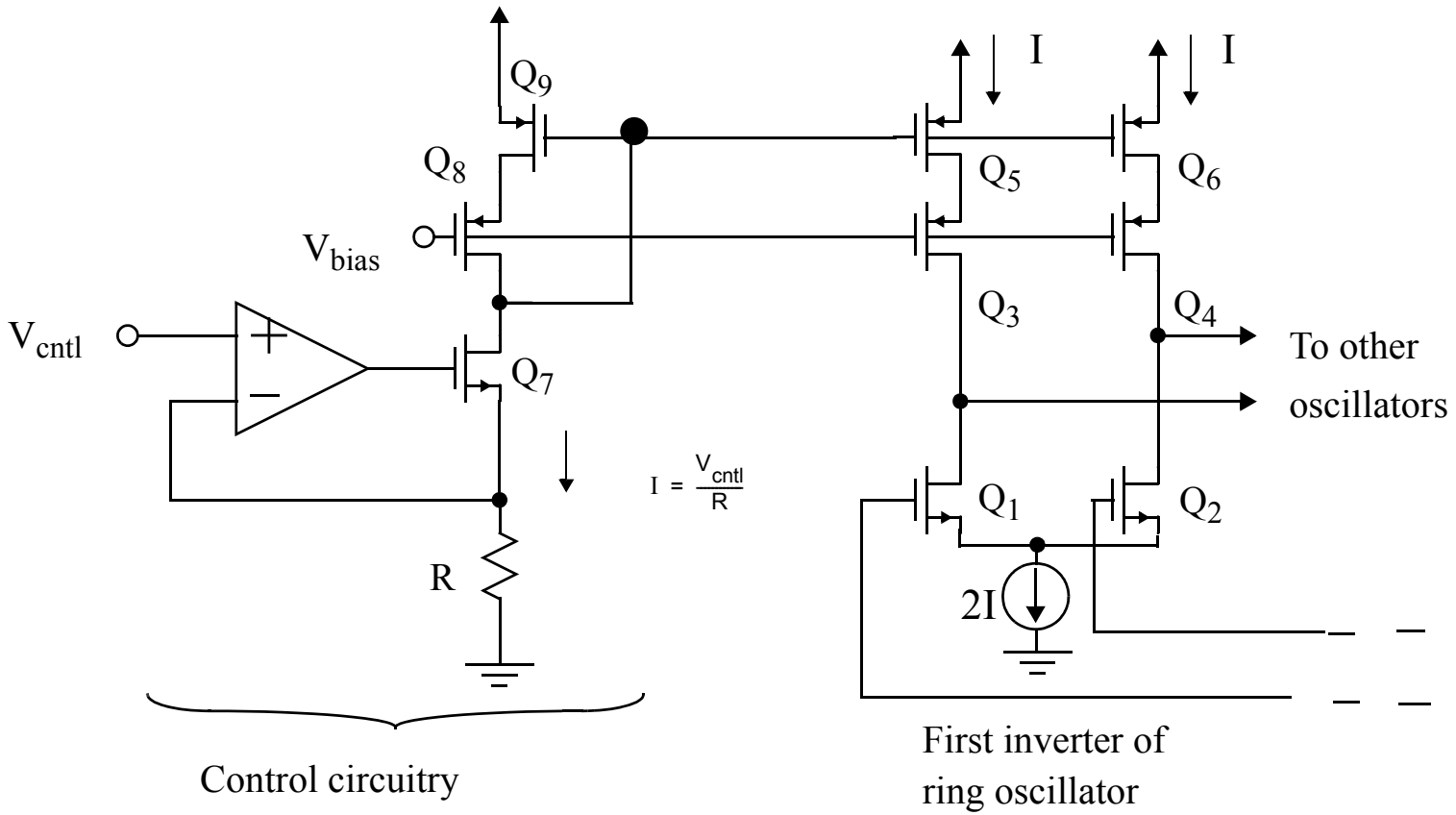

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_{inv}} \tag{22}$$

where $\tau_{inv}$ is delay of each inverter

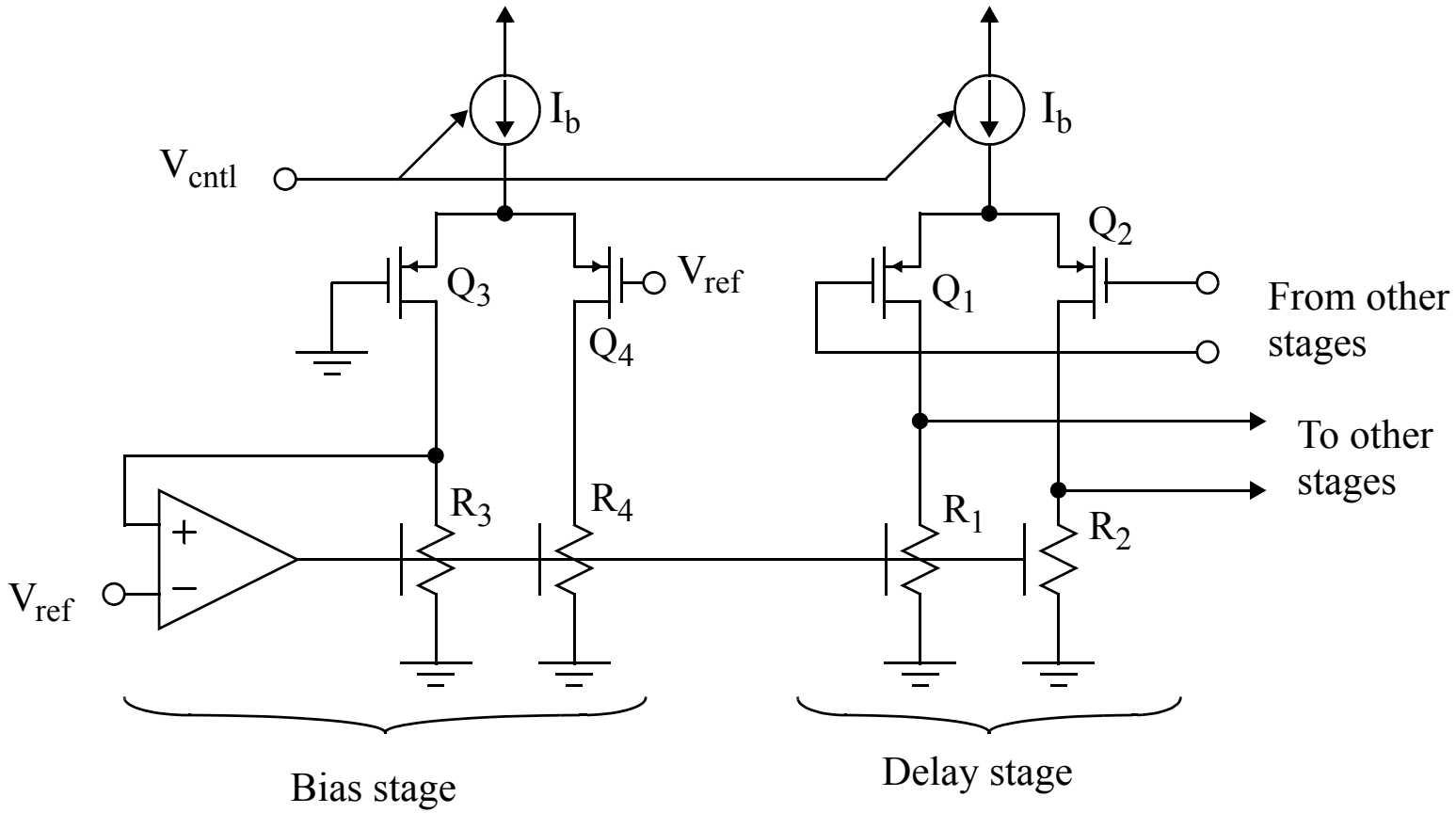
# Fully Differential Delay Stage



# V2I Conversion



# Alternative Biasing



# Computer Simulation of PLLs

- Simulation times can be very long due to large variations in time-constants
- Make use of bilinear transform to simulate analog signals in discrete timesteps.
- Loop Filter example
- Impedance looking into loop filter is ... ($G = 1/R$)

$$Z_{lp}(s) = \frac{1}{sC_1} + \frac{1}{sC_2 + G} \tag{23}$$

- So voltage to charge relationship is ...

$$\frac{V_{lp}(s)}{Q_{lp}(s)} = \frac{G + s(C_1 + C_2)}{GC_1 + sC_1C_2} \tag{24}$$

# Discrete-time loop filter

- Use bilinear transform

$$s \leftarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{25}$$

- giving

$$M(z) = \frac{V_{\mathrm{lp}}(z)}{Q_{\mathrm{lp}}(z)} = \frac{2(1-z^{-1})(C_1+C_2)+GT(1+z^{-1})}{2C_1C_2(1-z^{-1})+C_1GT(1+z^{-1})} \tag{26}$$

  which can be written as

$$P(z) = \frac{V_{lp}(z)}{\Delta Q_{lp}(z)} = \frac{m_1 + m_2 z^{-1}}{1 + z^{-1}(k-2) + z^{-2}(1-k)} \tag{27}$$

$$= \left(\frac{1}{1 - z^{-1}}\right)\left(\frac{m_1 + m_2 z^{-1}}{1 - z^{-1} + kz^{-1}}\right)$$

where

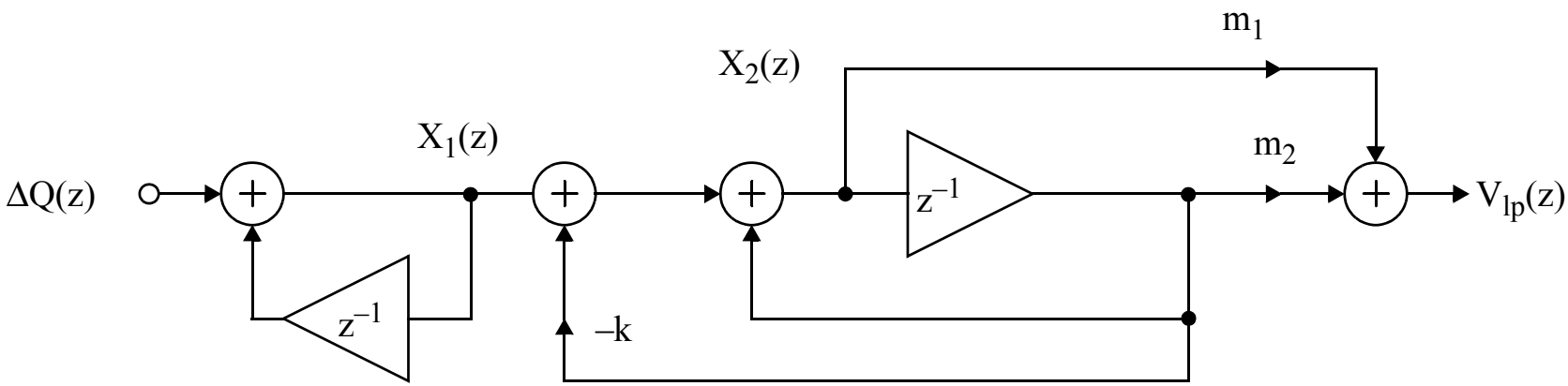
$$k = \frac{2GC_1T}{D} \tag{28}$$

$$m_1 = \frac{2(C_1 + C_2) + GT}{D} \tag{29}$$

$$m_2 = \frac{-2(C_1 + C_2) + GT}{D} \tag{30}$$

$$D = 2C_1C_2 + GC_1T \tag{31}$$

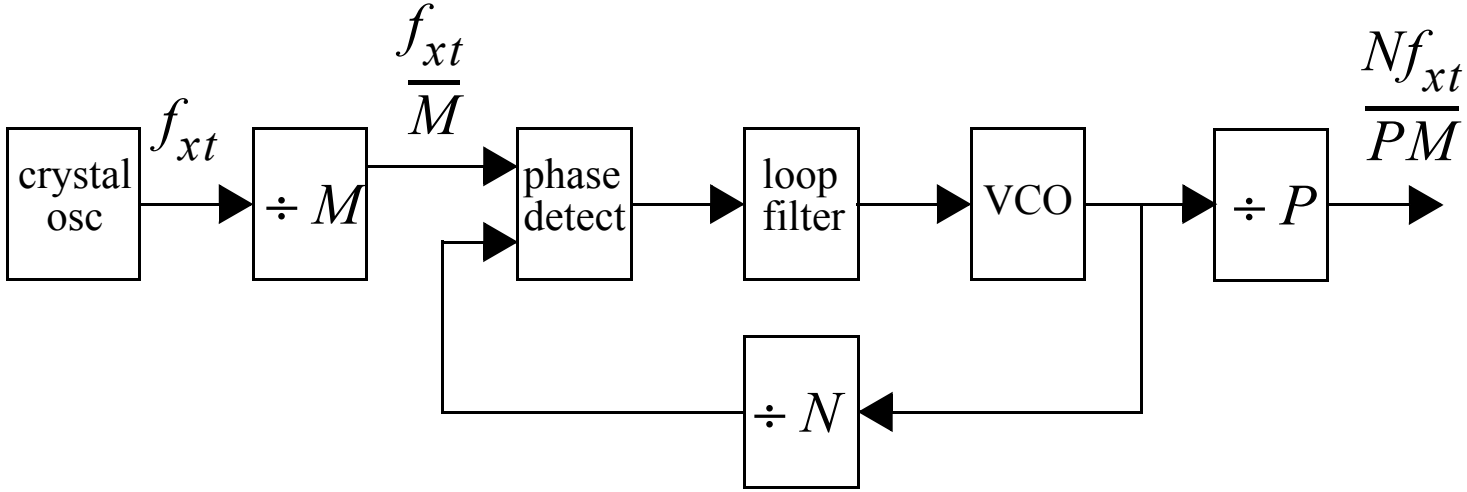
# Discrete-time Loop Filter




- Can use Matlab, Simulink, C, etc to simulate

# A Fractional-N Frequency Synthesizer

- Use oversampling within a PLL




$N = \{k\text{-}1, k, k\text{+}1\}$

A digital controlled oscillator