Switched-Capacitor Circuits

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Basic Building Blocks

Opamps

- Ideal opamps usually assumed.
- Important non-idealities

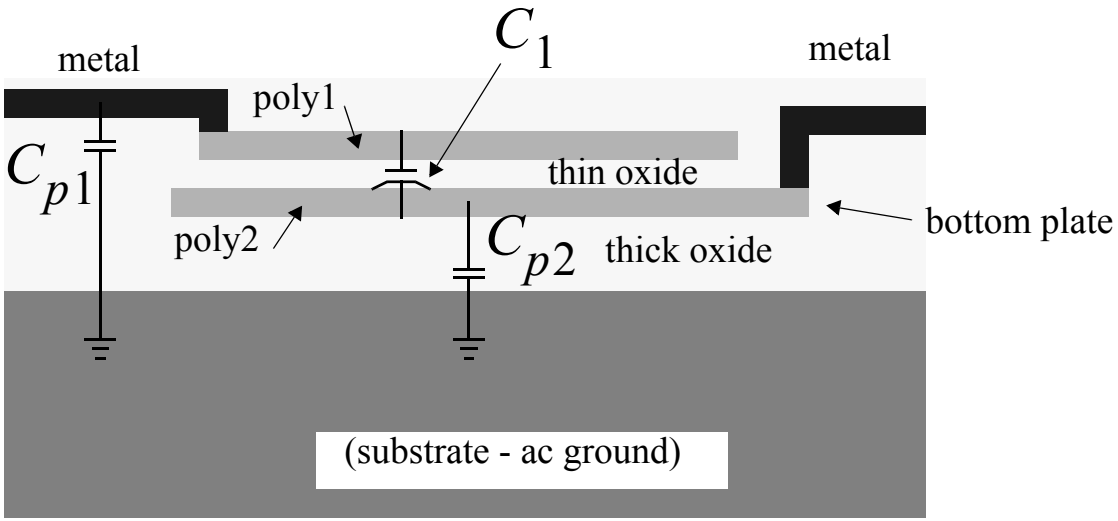
  — dc gain: sets the accuracy of charge transfer, hence, transfer-function accuracy.

  — unity-gain freq, phase margin & slew-rate: sets the max clocking frequency. A general rule is that unity-gain freq should be 5 times (or more) higher than the clock-freq.

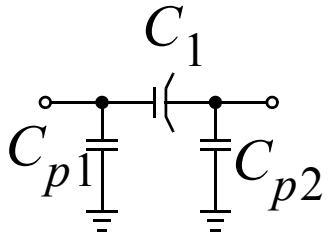
  — dc offset: Can create dc offset at output. Circuit techniques to combat this which also reduce 1/f noise.

Basic Building Blocks

Double-Poly Capacitors



cross-section view



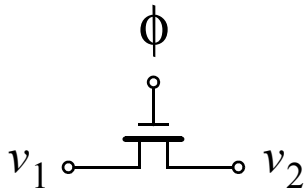
equivalent circuit

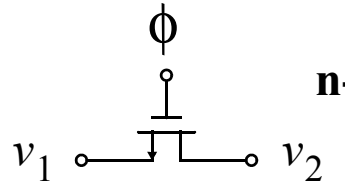
- Substantial parasitics with large bottom plate capacitance (20 percent of C_1)
- Also, metal-metal capacitors are used but have even larger parasitic capacitances.

Basic Building Blocks

Switches

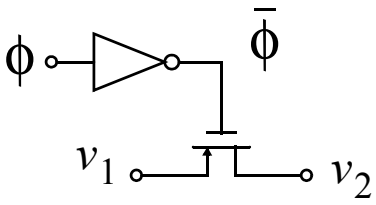
Symbol

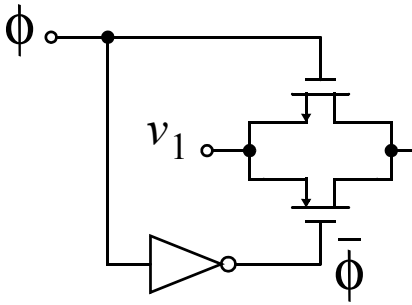




n-channel

p-channel





transmission gate

- Mosfet switches are good switches.

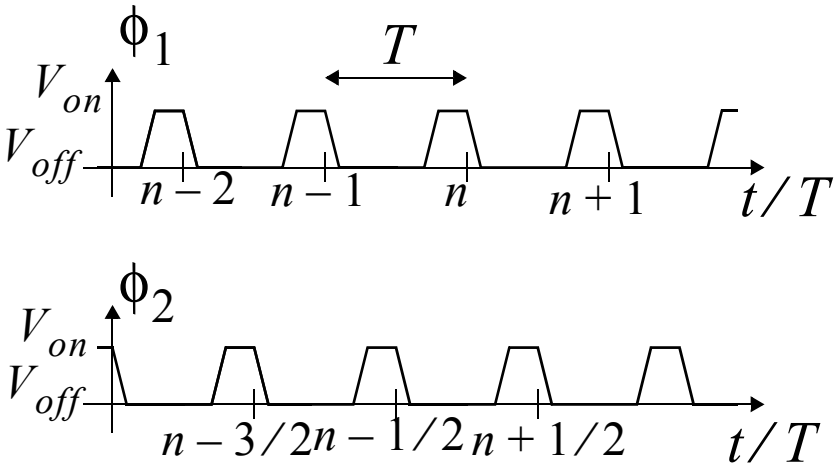
  — off-resistance near GΩ range

  — on-resistance in 100Ω to 5kΩ range (depends on transistor sizing)

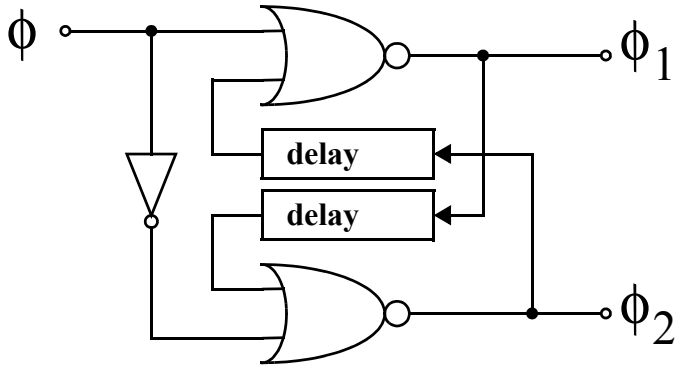
- However, have non-linear parasitic capacitances.

Basic Building Blocks

Non-Overlapping Clocks

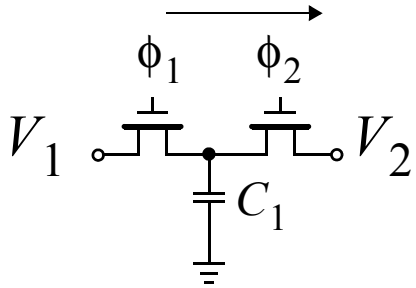


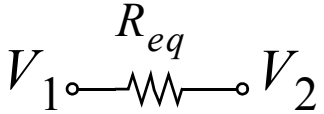
$$f_s \equiv \frac{1}{T}$$



- Non-overlapping clocks — both clocks are never on at same time
- Needed to ensure charge is not inadvertently lost.
- Integer values occur at end of ϕ_1.
- End of ϕ_2 is 1/2 off integer value.

Switched-Capacitor Resistor Equivalent





$\Delta Q = C_1(V_1 - V_2)$ every clock period

$$R_{eq} = \frac{T}{C_1}$$

$$Q_x = C_x V_x \tag{1}$$

- C_1 charged to V_1 and then V_2 during each clk period.

$$\Delta Q_1 = C_1(V_1 - V_2) \tag{2}$$

- Find equivalent average current

$$I_{avg} = \frac{C_1(V_1 - V_2)}{T} \tag{3}$$

where T is the clk period.

Switched-Capacitor Resistor Equivalent

- For equivalent resistor circuit

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}} \tag{4}$$

- Equating two, we have

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \tag{5}$$

- This equivalence is useful when looking at low-freq portion of a SC-circuit.
- For higher frequencies, discrete-time analysis is used.

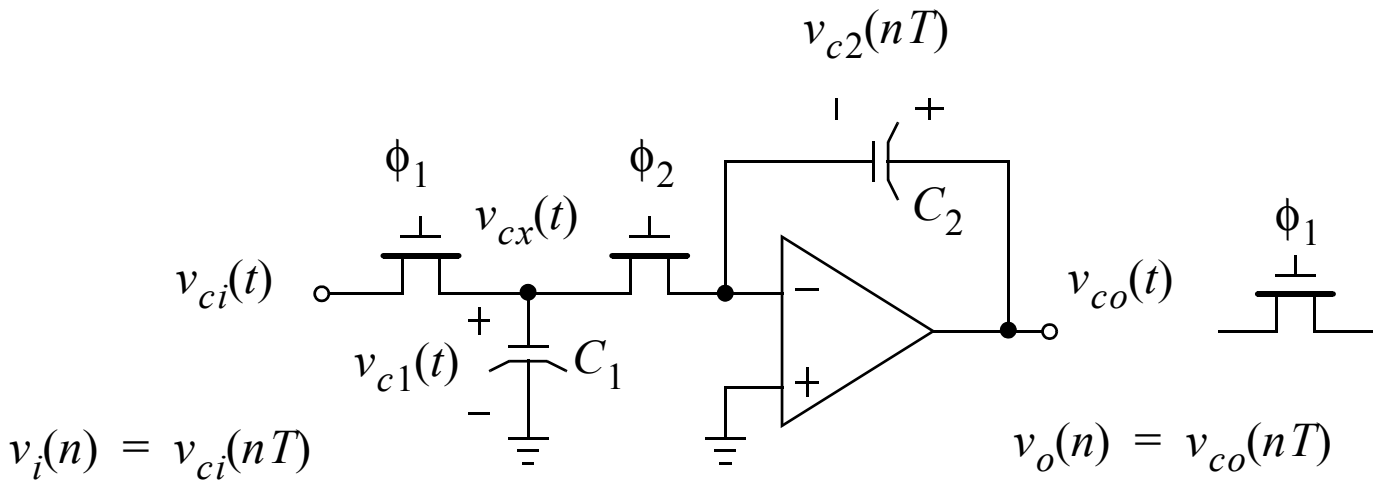
Resistor Equivalence Example

- What is the equivalent resistance of a $5pF$ capacitance sampled at a clock frequency of $100kHz$.
- Using (5), we have

$$R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^{3})} = 2M\Omega$$

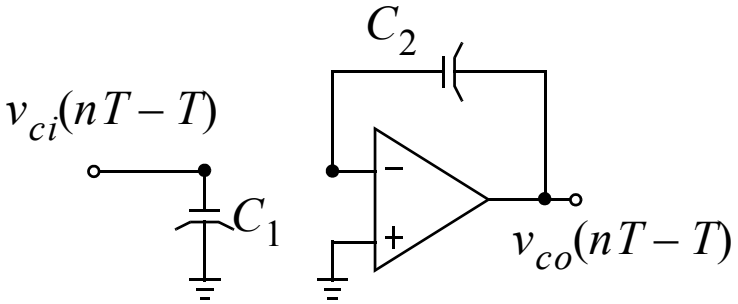
- Note that a very large equivalent resistance of $2M\Omega$ can be realized.
- Requires only 2 transistors, a clock and a relatively small capacitance.
- In a typical CMOS process, such a large resistor would normally require a huge amount of silicon area.

Parasitic-Sensitive Integrator

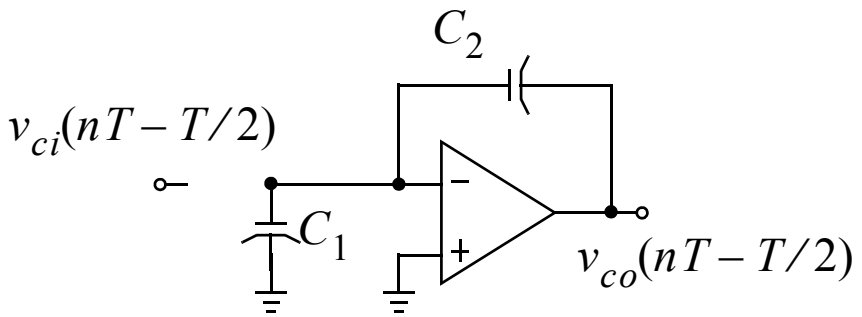


- Start by looking at an integrator which IS affected by parasitic capacitances
- Want to find output voltage at end of ϕ_1 in relation to input sampled at end of ϕ_1.

Parasitic-Sensitive Integrator



ϕ_1 on



ϕ_2 on

- At end of ϕ_2

$$C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T) \qquad (6)$$

- But would like to know the output at end of ϕ_1

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) \qquad (7)$$

- leading to

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T) - C_1 v_{ci}(nT - T) \qquad (8)$$

Parasitic-Sensitive Integrator

- Modify above to write

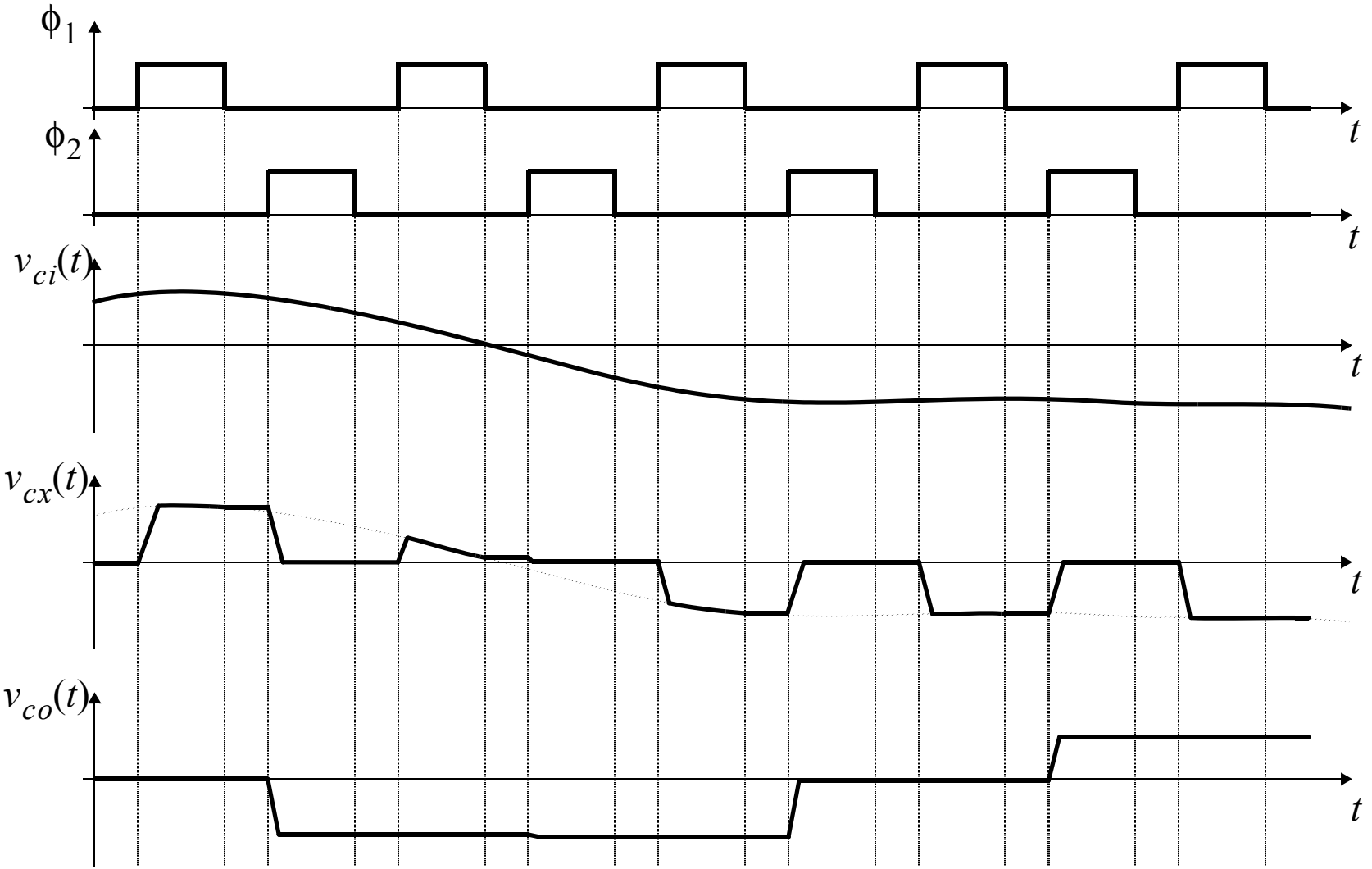
$$v_o(n) = v_o(n-1) - \frac{C_1}{C_2} v_i(n-1) \tag{9}$$

and taking z-transform and re-arranging, leads to

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1} \tag{10}$$

- Note that gain-coefficient is determined by a ratio of two capacitance values.
- Ratios of capacitors can be set VERY accurately on an integrated circuit (within 0.1 percent)
- Leads to very accurate transfer-functions.

Typical Waveforms



Low Frequency Behavior

- Equation (10) can be re-written as

$$H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{z^{1/2} - z^{-1/2}} \tag{11}$$

- To find freq response, recall

$$z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \tag{12}$$

$$z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right) \tag{13}$$

$$z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right) \tag{14}$$

$$H(e^{j\omega T}) = -\left(\frac{C_1}{C_2}\right)\frac{\cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)}{j2\sin\left(\frac{\omega T}{2}\right)} \tag{15}$$

Low Frequency Behavior

- Above is exact but when $\omega T \ll 1$ (i.e., at low freq)

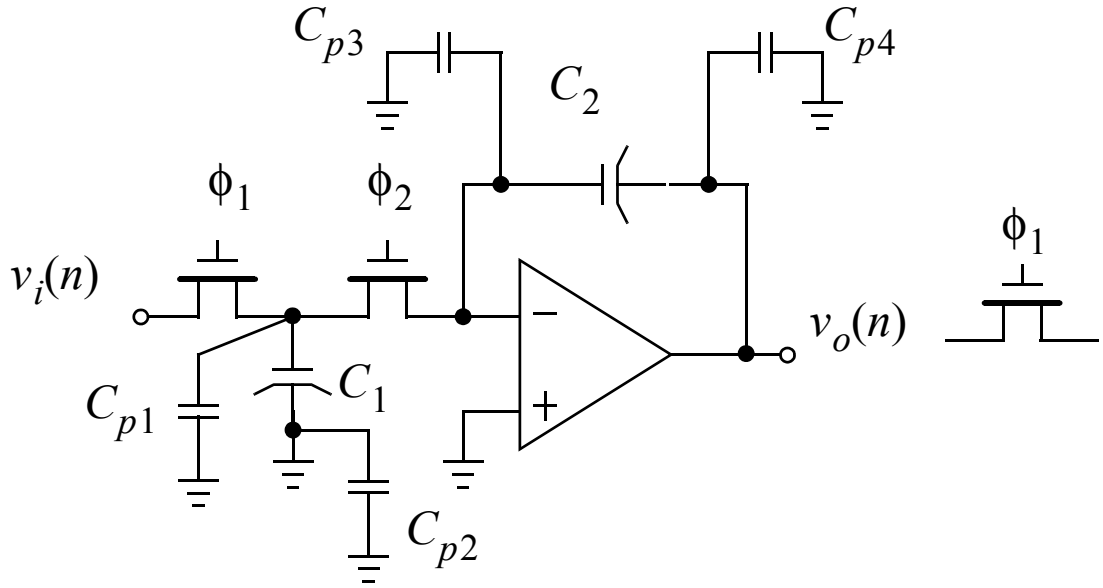
$$H(e^{j\omega T}) \cong -\left(\frac{C_1}{C_2}\right)\frac{1}{j\omega T} \tag{16}$$

- Thus, the transfer function is same as a continuous-time integrator having a gain constant of

$$K_I \cong \frac{C_1}{C_2}\frac{1}{T} \tag{17}$$

which is a function of the integrator capacitor ratio and clock frequency only.

Parasitic Capacitance Effects

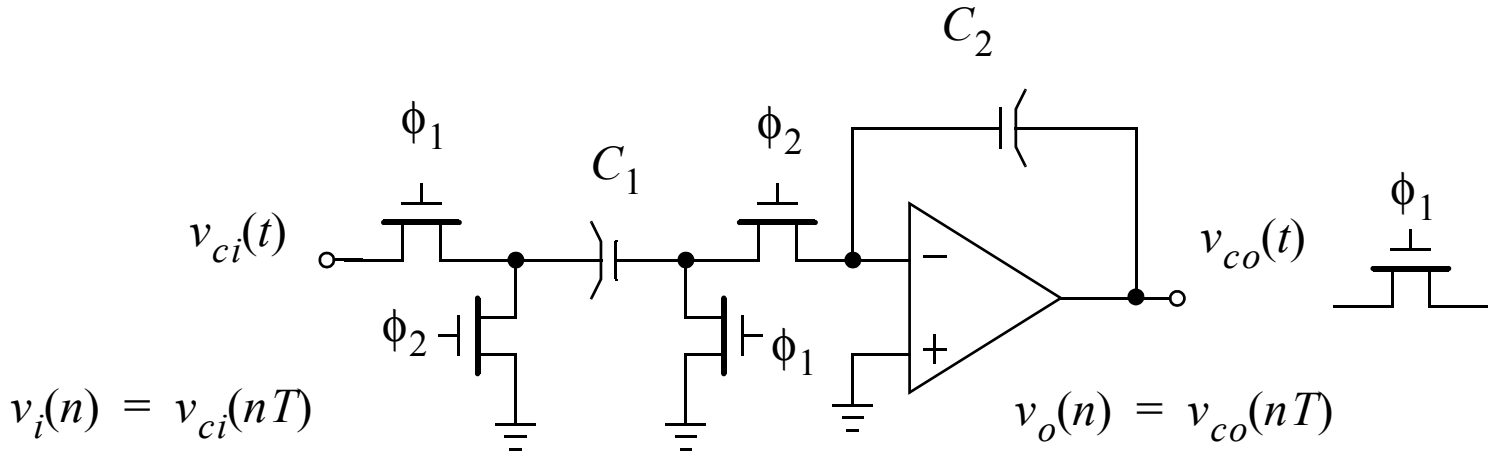


- Accounting for parasitic capacitances, we have

$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1} \qquad (18)$$

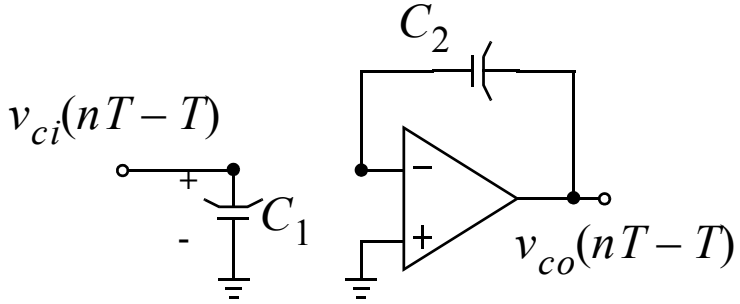
- Thus, gain coefficient is not well controlled and partially non-linear (due to C_{p1} being non-linear).

Parasitic-Insensitive Integrators

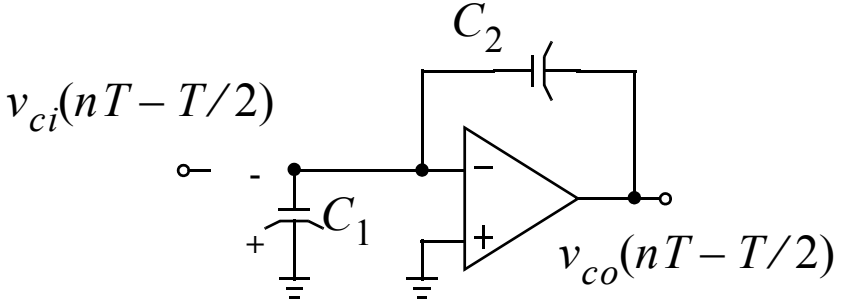


- By using 2 extra switches, integrator can be made insensitive to parasitic capacitances
  - — more accurate transfer-functions
  - — better linearity (since non-linear capacitances unimportant)

Parasitic-Insensitive Integrators



ϕ_1 on



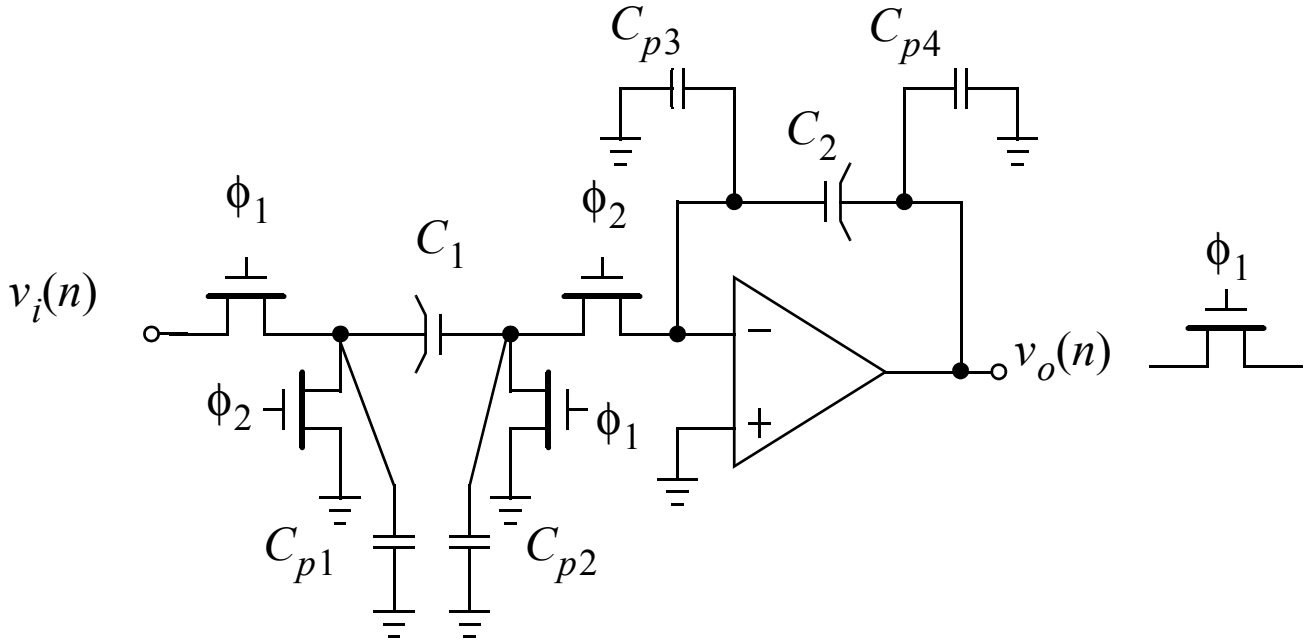
ϕ_2 on

- Same analysis as before except that C_1 is switched in polarity before discharging into C_2.

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1} \tag{19}$$

- A positive integrator (rather than negative as before)

Parasitic-Insensitive Integrators

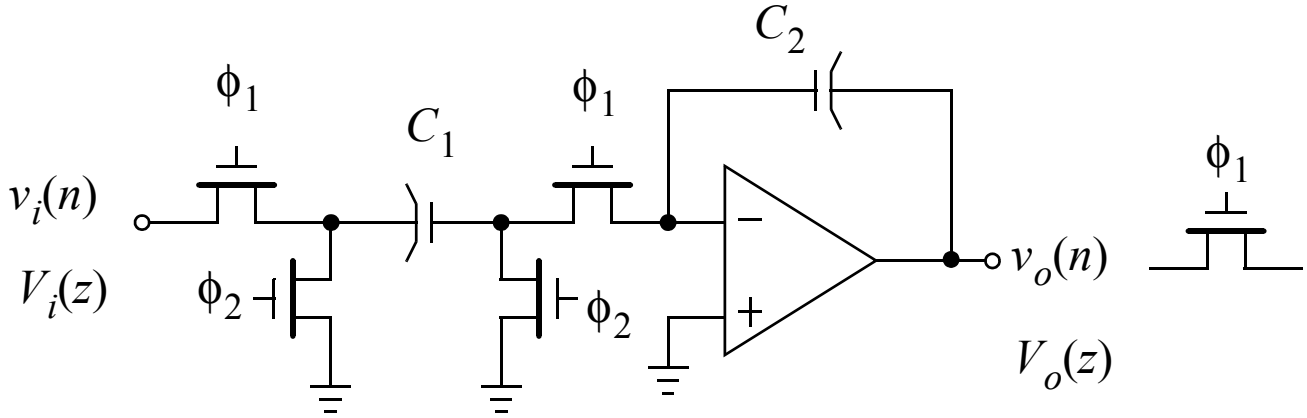


- C_{p3} has little effect since it is connected to virtual gnd
- C_{p4} has little effect since it is driven by output
- C_{p2} has little effect since it is either connected to virtual gnd or physical gnd.

Parasitic-Insensitive Integrators

- C_{p1} is continuously being charged to $v_i(n)$ and discharged to ground.
- ϕ_1 on — the fact that C_{p1} is also charged to $v_i(n-1)$ does not affect C_1 charge.
- ϕ_2 on — C_{p1} is discharged through the ϕ_2 switch attached to its node and does not affect the charge accumulating on C_2.
- While the parasitic capacitances may slow down settling time behavior, they do not affect the discrete-time difference equation

Parasitic-Insensitive Inverting Integrator



$$C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T) \tag{20}$$

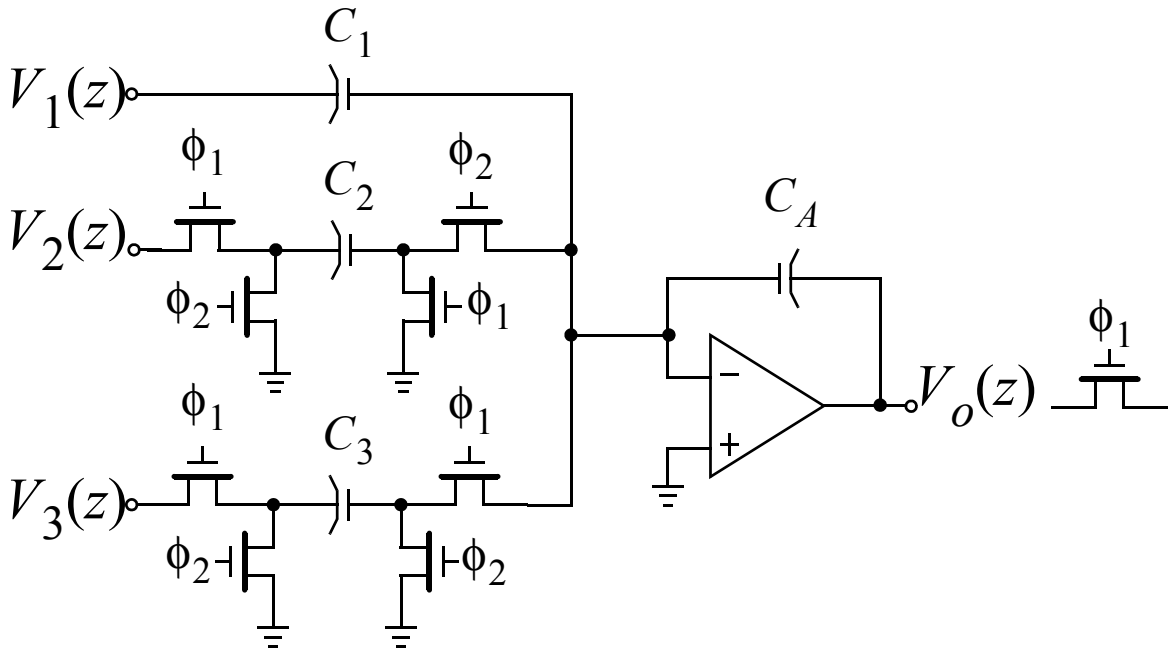
$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) - C_1 v_{ci}(nT) \tag{21}$$

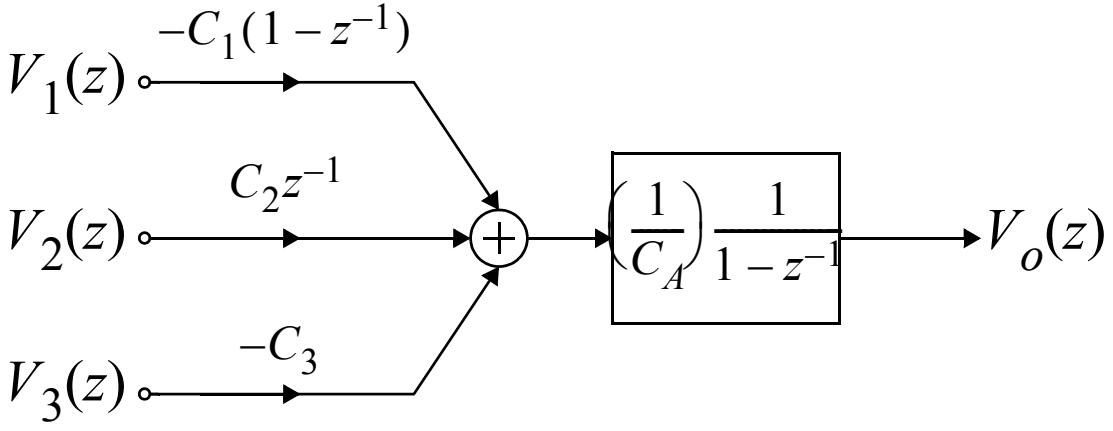
- Present output depends on present input ***(delay-free)***

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1} \tag{22}$$

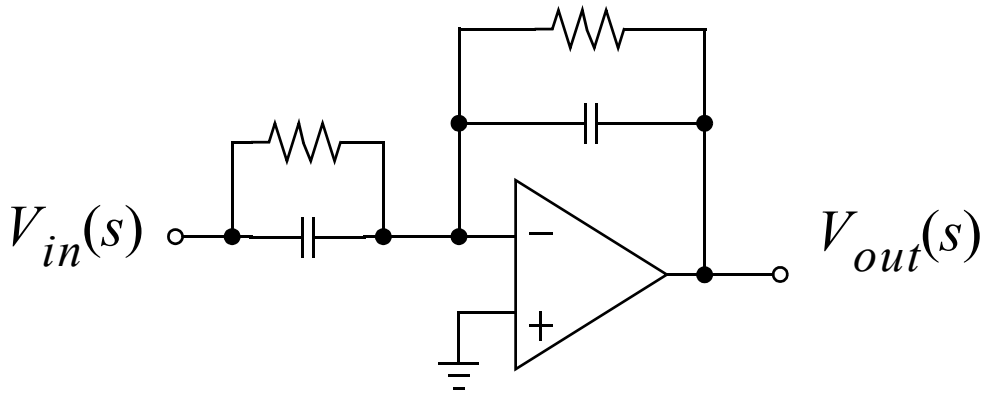
- Delay-free integrator has negative gain while delaying integrator has positive gain.

Signal-Flow-Graph Analysis



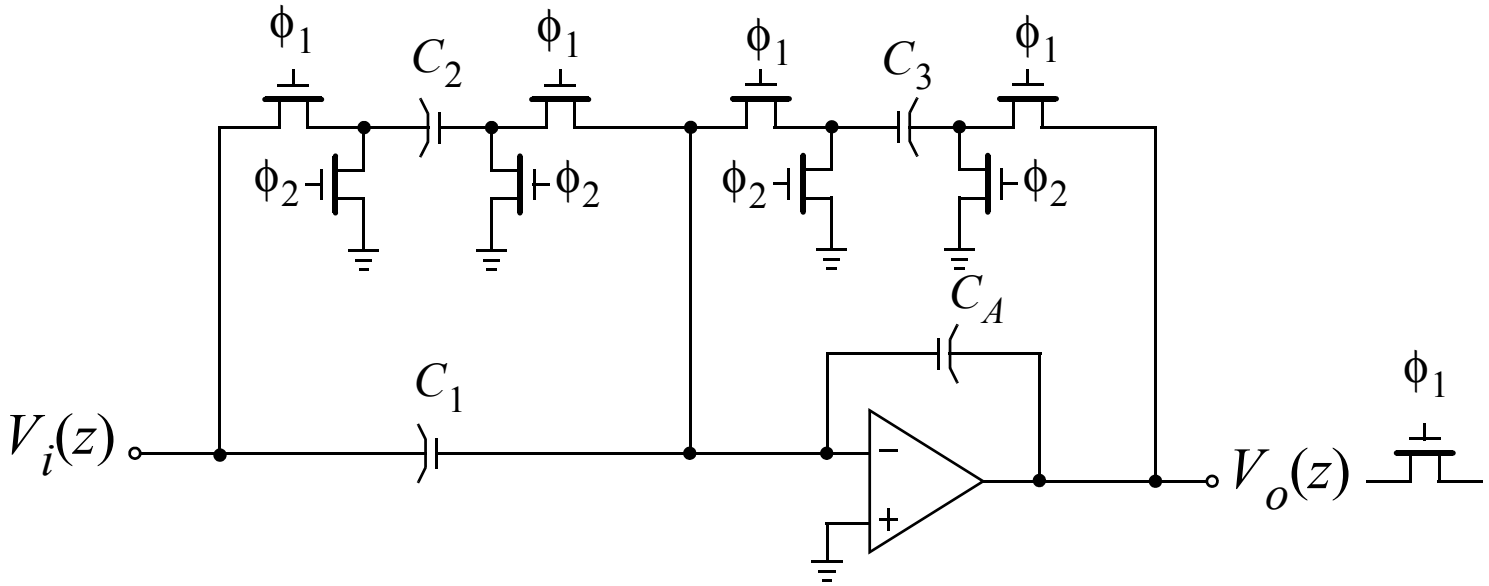


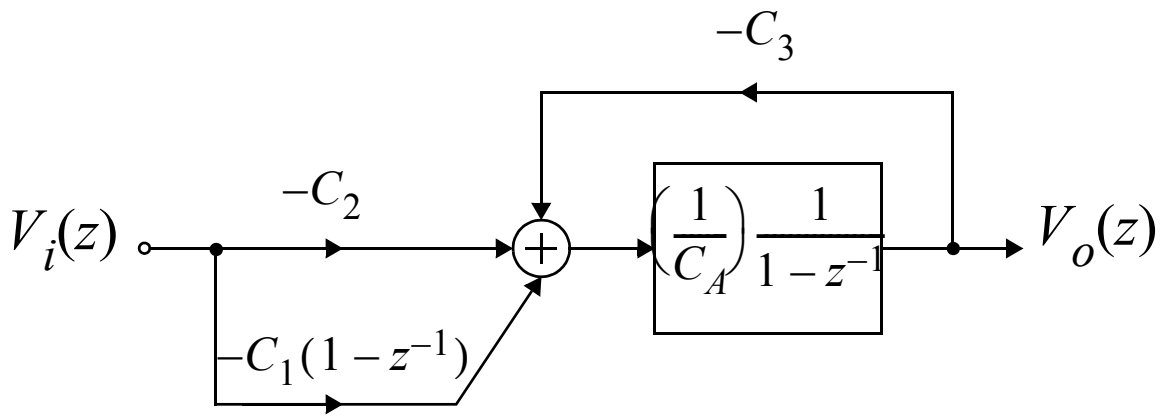
First-Order Filter



- Start with an active-RC structure and replace resistors with SC equivalents.
- Analyze using discrete-time analysis.

First-Order Filter





First-Order Filter

$$C_A(1-z^{-1})V_o(z) = -C_3V_o(z) - C_2V_i(z) - C_1(1-z^{-1})V_i(z) \quad (23)$$

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{\left(\frac{C_1}{C_A}\right)(1-z^{-1}) + \left(\frac{C_2}{C_A}\right)}{1 - z^{-1} + \frac{C_3}{C_A}} \quad (24)$$

$$= -\frac{\left(\frac{C_1 + C_2}{C_A}\right)z - \frac{C_1}{C_A}}{\left(1 + \frac{C_3}{C_A}\right)z - 1}$$

First-Order Filter

- The pole of (24) is found by equating the denominator to zero

$$z_p = \frac{C_A}{C_A + C_3} \tag{25}$$

- For positive capacitance values, this pole is restricted to the real axis between 0 and 1
  — circuit is always stable.
- The zero of (24) is found to be given by

$$z_z = \frac{C_1}{C_1 + C_2} \tag{26}$$

- Also restricted to real axis between 0 and 1.

First-Order Filter

The dc gain is found by setting $z = 1$ which results in

$$H(1) = \frac{-C_2}{C_3} \tag{27}$$

- Note that in a fully-differential implementation, effective negative capacitances for C_1, C_2 and C_3 can be achieved by simply interchanging the input wires.
- In this way, a zero at $z = -1$ could be realized by setting

$$C_1 = -0.5C_2 \tag{28}$$

First-Order Example

- Find the capacitance values needed for a first-order SC-circuit such that its 3dB point is at $10kHz$ when a clock frequency of $100kHz$ is used.
- It is also desired that the filter have zero gain at $50kHz$ (i.e. $z = -1$) and the dc gain be unity.
- Assume $C_A = 10pF$.

Solution

- Making use of the bilinear transform $p = (z-1)/(z+1)$ the zero at -1 is mapped to $\Omega = \infty$.
- The frequency warping maps the -3dB frequency of $10kHz$ (or 0.2π rad/sample) to

First-Order Example

$$\Omega = \tan\left(\frac{0.2\pi}{2}\right) = 0.3249 \tag{29}$$

- in the continuous-time domain leading to the continuous-time pole, p_p, required being

$$p_p = -0.3249 \tag{30}$$

- This pole is mapped back to z_p given by

$$z_p = \frac{1 + p_p}{1 - p_p} = 0.5095 \tag{31}$$

- Therefore, $H(z)$ is given by

$$H(z) = \frac{k(z+1)}{z - 0.5095} \tag{32}$$

First-Order Example

- where k is determined by setting the dc gain to one (i.e. $H(1) = 1$) resulting

$$H(z) = \frac{0.24525(z+1)}{z-0.5095} \tag{33}$$

- or equivalently,

$$H(z) = \frac{0.4814z + 0.4814}{1.9627z - 1} \tag{34}$$

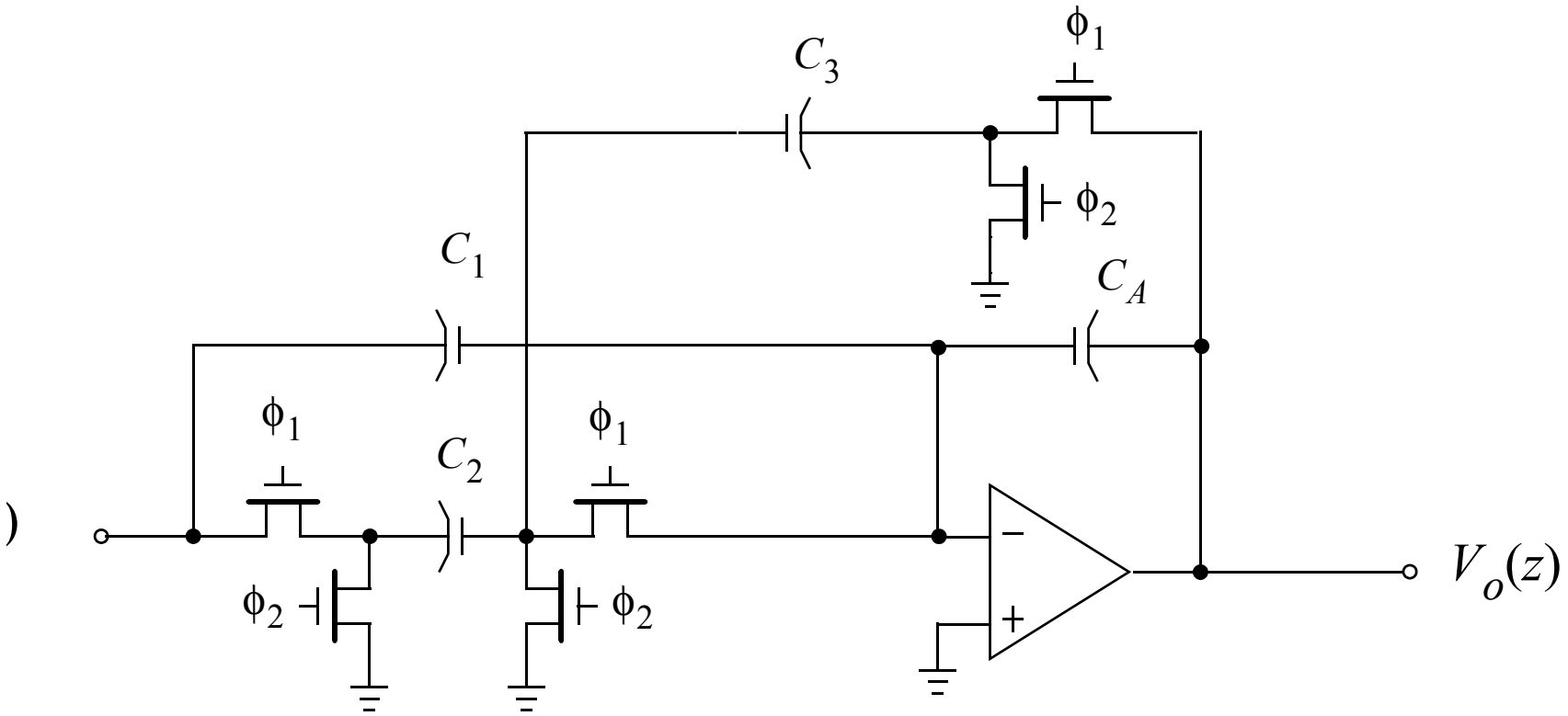
- Equating these coefficients with those of (24) (and assuming $C_A = 10pF$) results in

$$C_1 = 4.814pF \tag{35}$$

$$C_2 = -9.628pF \tag{36}$$

$$C_3 = 9.628pF \tag{37}$$

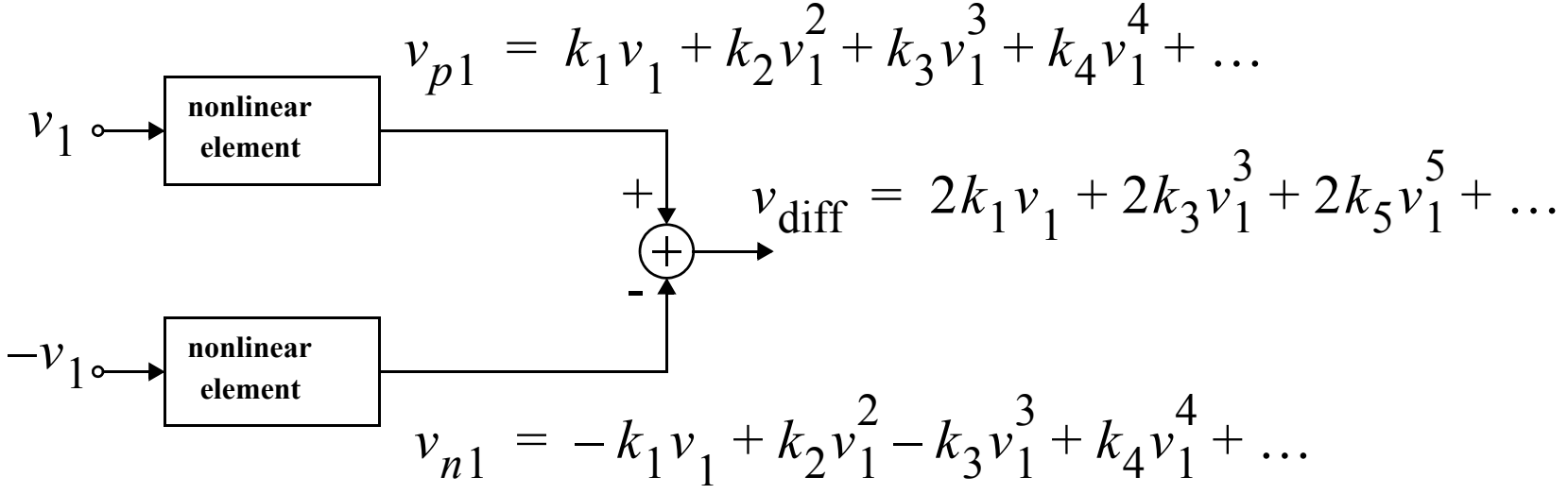
Switch Sharing



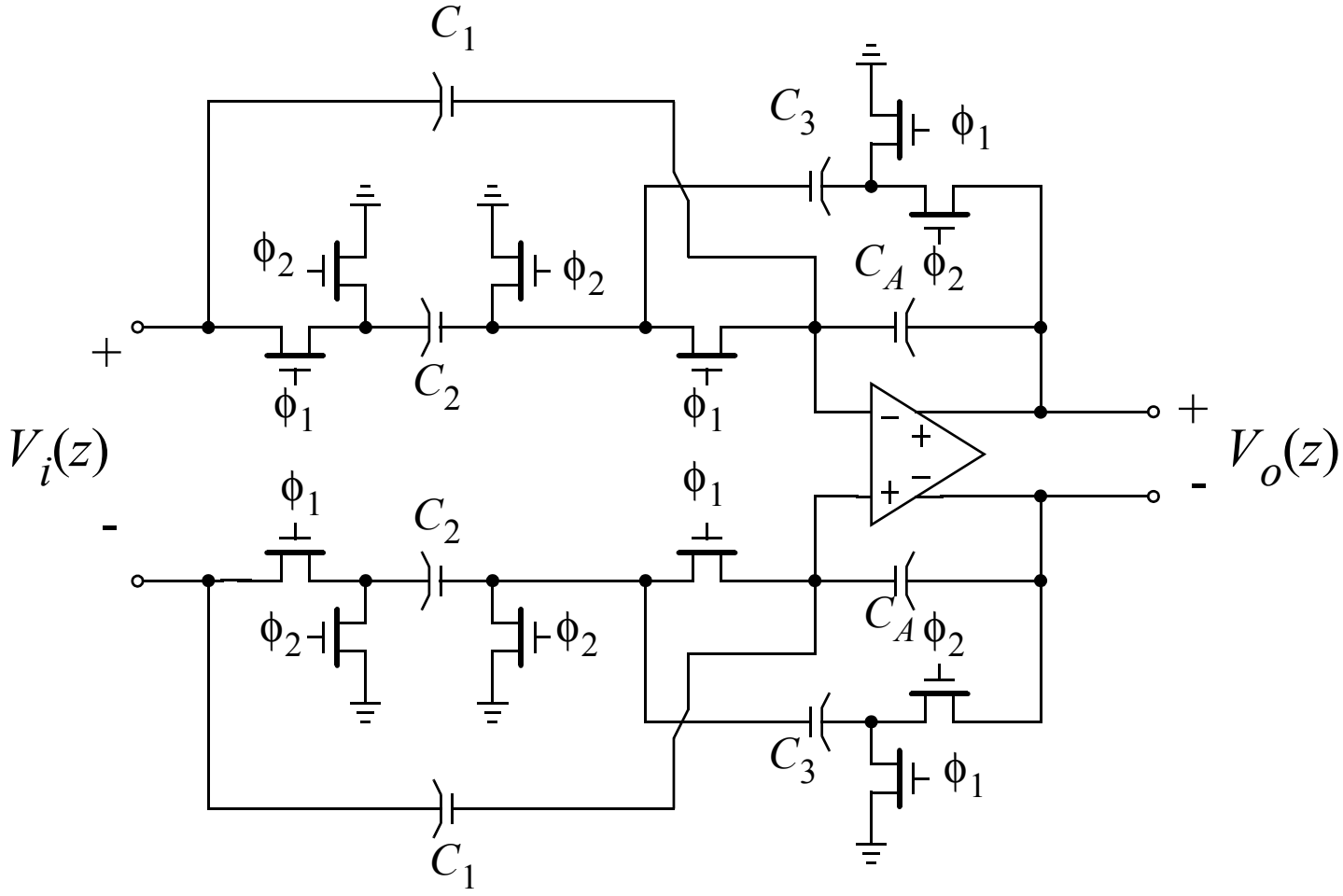
- Share switches that are always connected to the same potentials.

Fully-Differential Filters

- Most modern SC filters are fully-differential
- Difference between two voltages represents signal (also balanced around a common-mode voltage).
- Common-mode noise is rejected.
- Even order distortion terms cancel

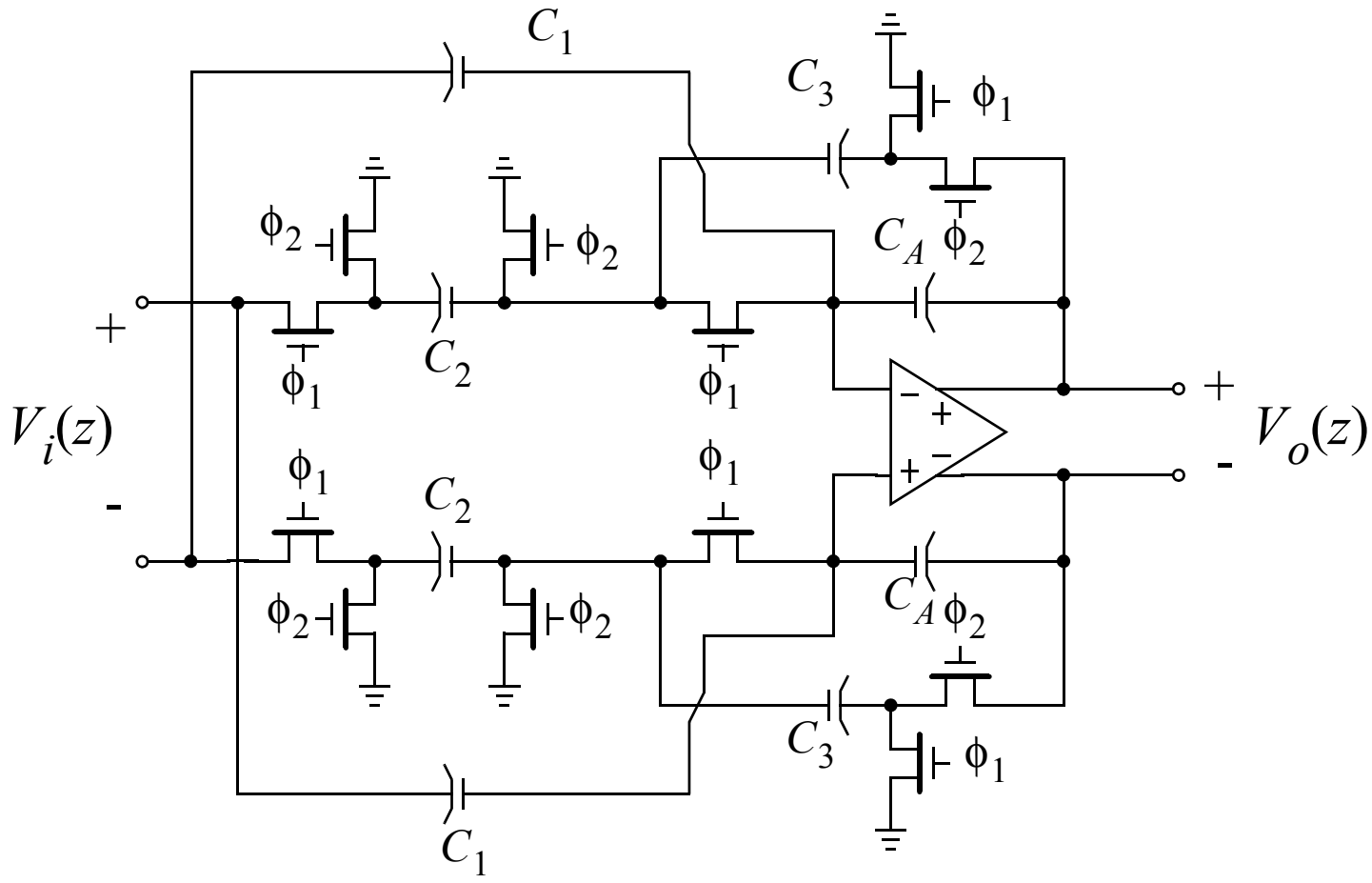


Fully-Differential Filters



Fully-Differential Filters

- Negative continuous-time input
  — equivalent to a negative C_1

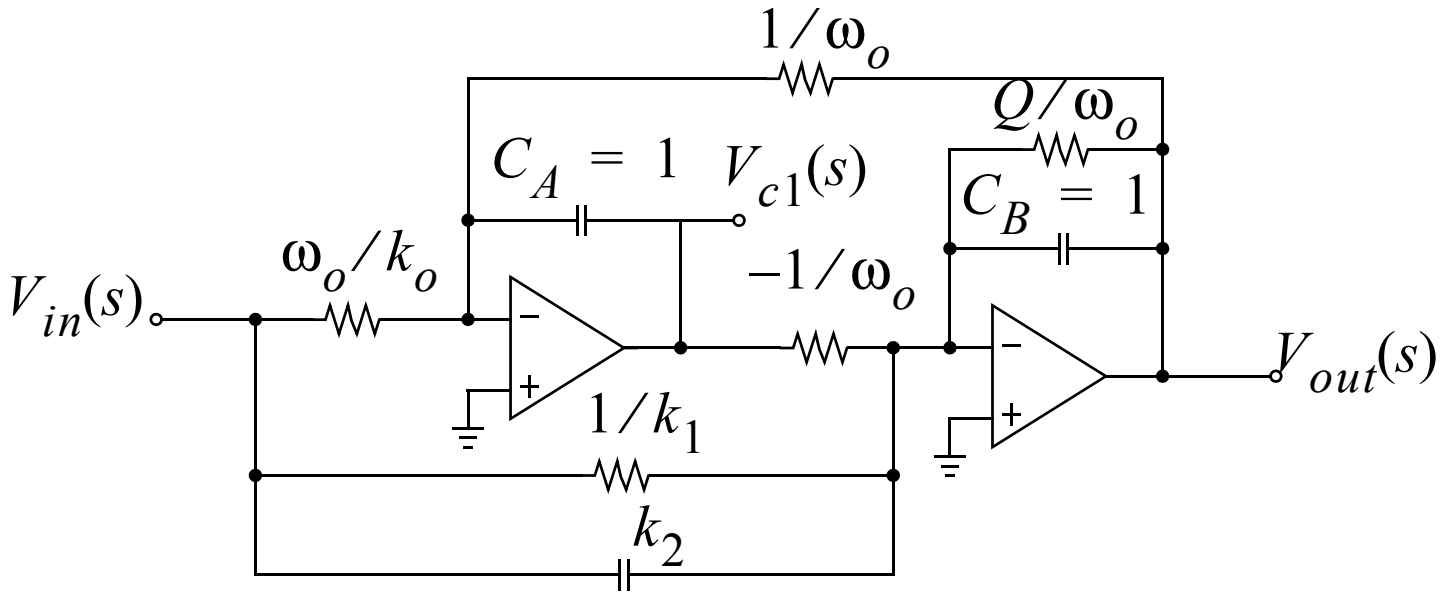


Fully-Differential Filters

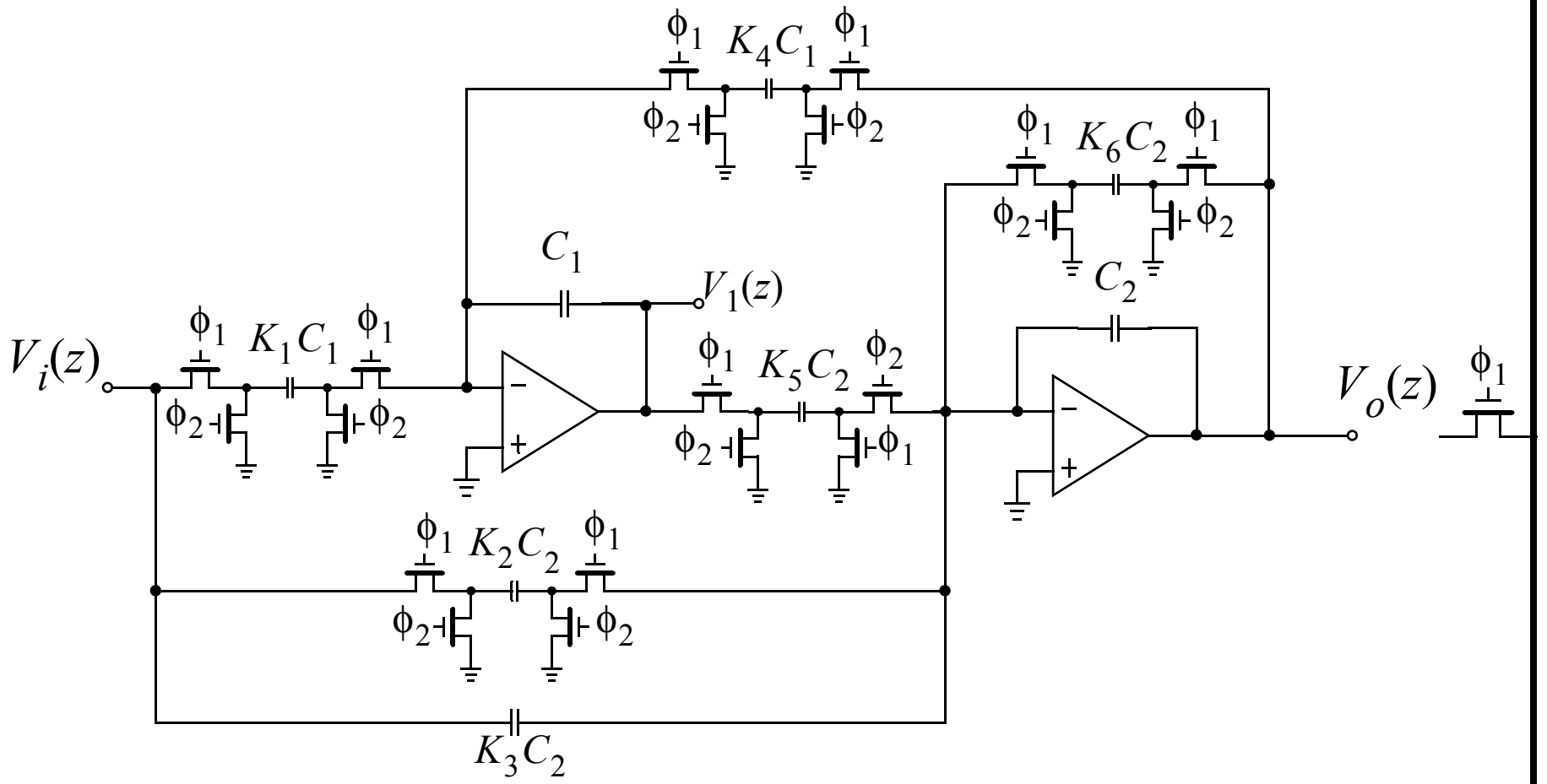
- Note that fully-differential version is essentially two copies of single-ended version, however ... area penalty not twice.
- Only one opamp needed (though common-mode circuit also needed)
- Input and output signal swings have been doubled so that same dynamic range can be achieved with half capacitor sizes (from kT/C analysis)
- Switches can be reduced in size since small caps used.
- However, there is more wiring in fully-differ version but better noise and distortion performance.

Low-Q Biquad Filter

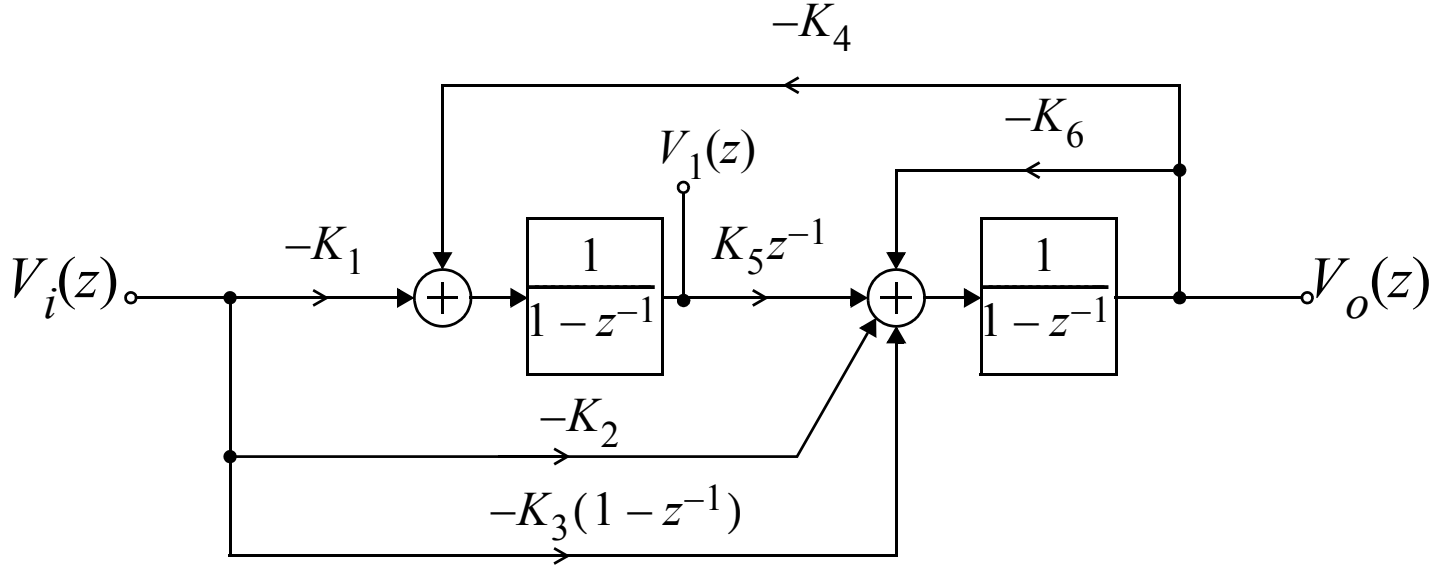
$$H_a(s) \equiv \frac{V_{out}(s)}{V_{in}(s)} = -\frac{k_2 s^2 + k_1 s + k_o}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \tag{38}$$



Low-Q Biquad Filter



Low-Q Biquad Filter



$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{(K_2+K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1+K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1} \qquad (39)$$

Low-Q Biquad Filter Design

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + 1} \tag{40}$$

- we can equate the individual coefficients of "z" in (39) and (40), resulting in:

$$K_3 = a_0 \tag{41}$$

$$K_2 = a_2 - a_0 \tag{42}$$

$$K_1 K_5 = a_0 + a_1 + a_2 \tag{43}$$

$$K_6 = b_2 - 1 \tag{44}$$

$$K_4 K_5 = b_1 + b_2 + 1 \tag{45}$$

- A degree of freedom is available here in setting internal $V_1(z)$ output

Low-Q Biquad Filter Design

- Can do proper dynamic range scaling
- Or let the time-constants of 2 integrators be equal by

$$K_4 = K_5 = \sqrt{b_1 + b_2 + 1} \tag{46}$$

Low-Q Biquad Capacitance Ratio

- Comparing resistor circuit to SC circuit, we have

$$K_4 \approx K_5 \approx \omega_o T \tag{47}$$

$$K_6 \approx \frac{\omega_o T}{Q} \tag{48}$$

- However, the sampling-rate, $1/T$, is typically much larger that the approximated pole-frequency, ω_o,

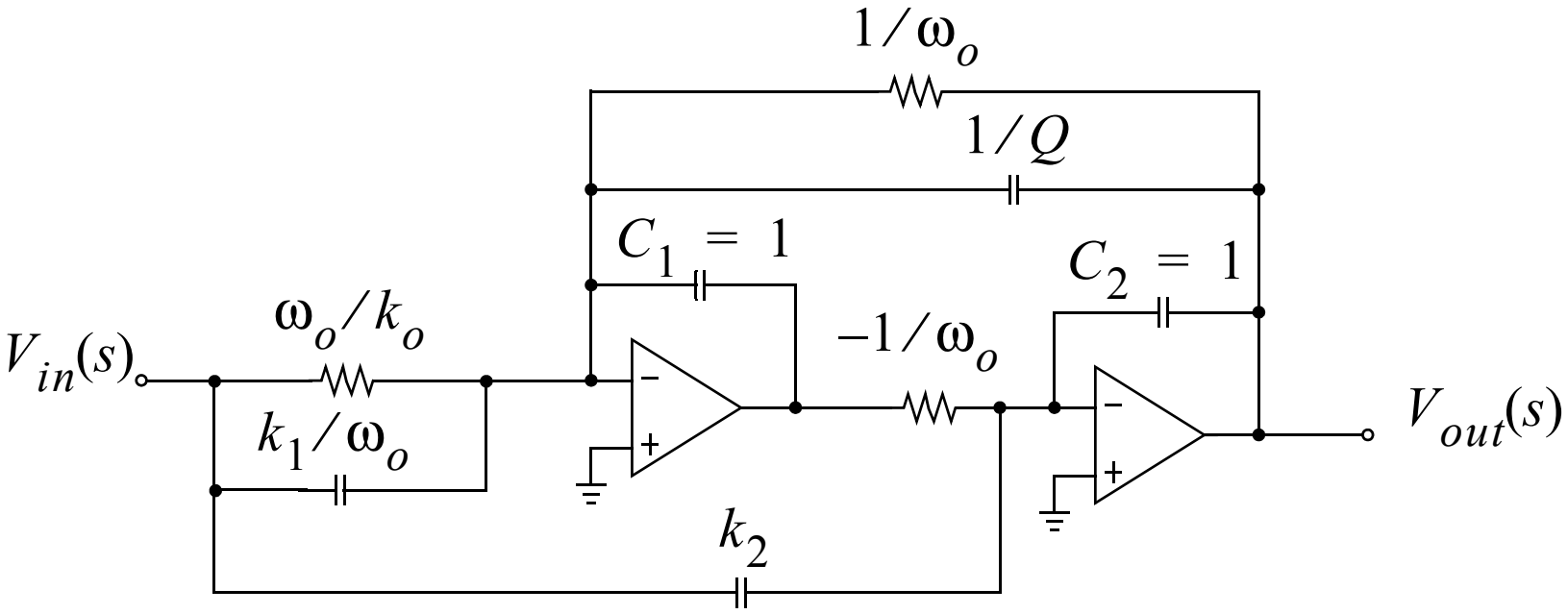
$$\omega_o T \ll 1 \tag{49}$$

Low-Q Biquad Capacitance Ratio

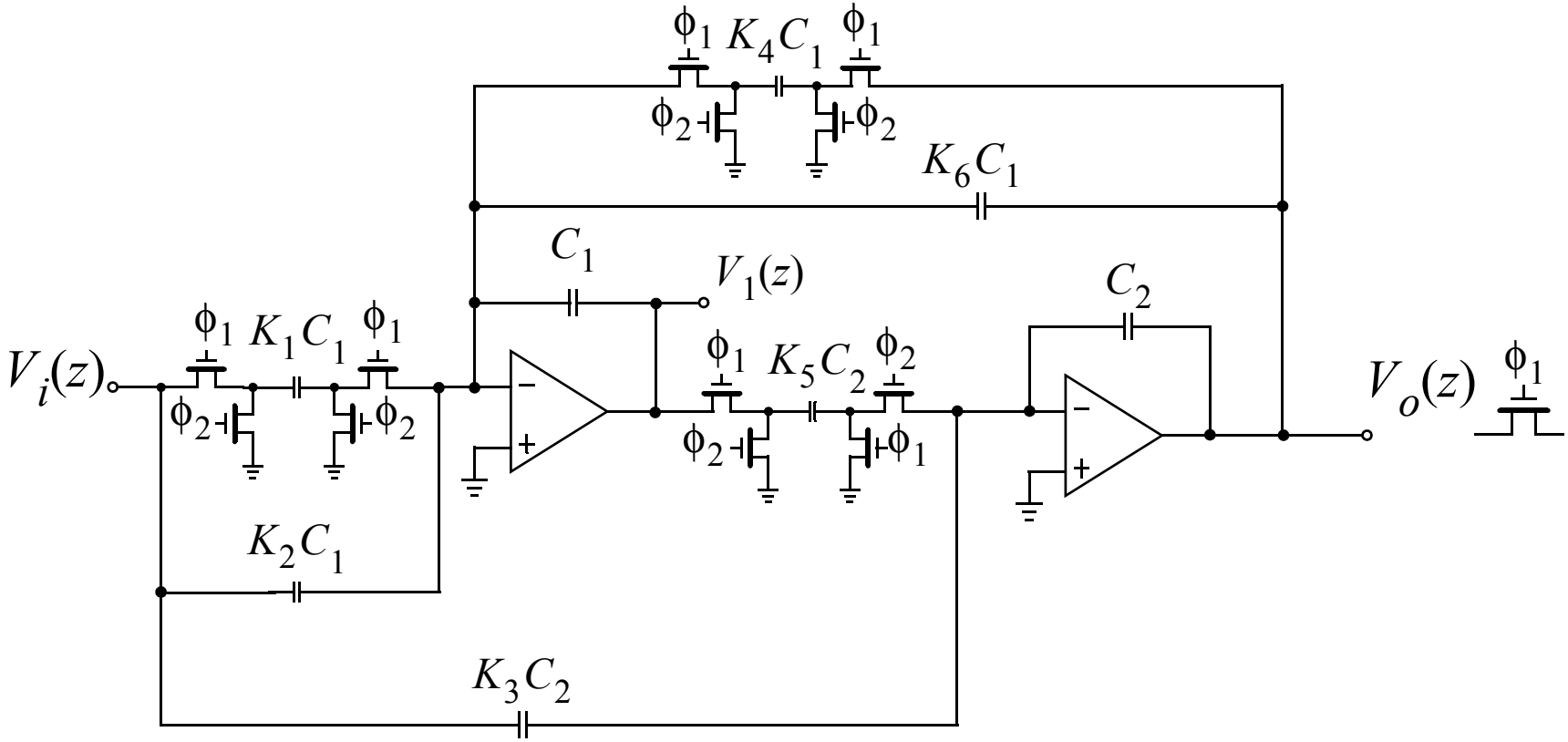
- Thus, the largest capacitors determining pole positions are the integrating capacitors, C_1 and C_2.
- If $Q < 1$, the smallest capacitors are $K_4 C_1$ and $K_5 C_2$ resulting in an approximate capacitance spread of $1/(\omega_o T)$.
- If $Q > 1$, then from (48) the smallest capacitor would be $K_6 C_2$ resulting in an approximate capacitance spread of $Q/(\omega_o T)$ — can be quite large for $Q \gg 1$

High-Q Biquad Filter

- Use a high-Q biquad filter circuit when $Q \gg 1$
- Q-damping done with a cap around both integrators
- Active-RC prototype filter



High-Q Biquad Filter



- Q-damping now performed by K_6C_1

High-Q Biquad Filter

- Input $K_1 C_1$: major path for lowpass
- Input $K_2 C_1$: major path for band-pass filters
- Input $K_3 C_2$: major path for high-pass filters
- General transfer-function is:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_3 z^2 + (K_1 K_5 + K_2 K_5 - 2K_3)z + (K_3 - K_2 K_5)}{z^2 + (K_4 K_5 + K_5 K_6 - 2)z + (1 - K_5 K_6)} \quad (50)$$

- If matched to the following general form

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0} \quad (51)$$

High-Q Biquad Filter

$$K_1 K_5 = a_0 + a_1 + a_2 \tag{52}$$

$$K_2 K_5 = a_2 - a_0 \tag{53}$$

$$K_3 = a_2 \tag{54}$$

$$K_4 K_5 = 1 + b_0 + b_1 \tag{55}$$

$$K_5 K_6 = 1 - b_0 \tag{56}$$

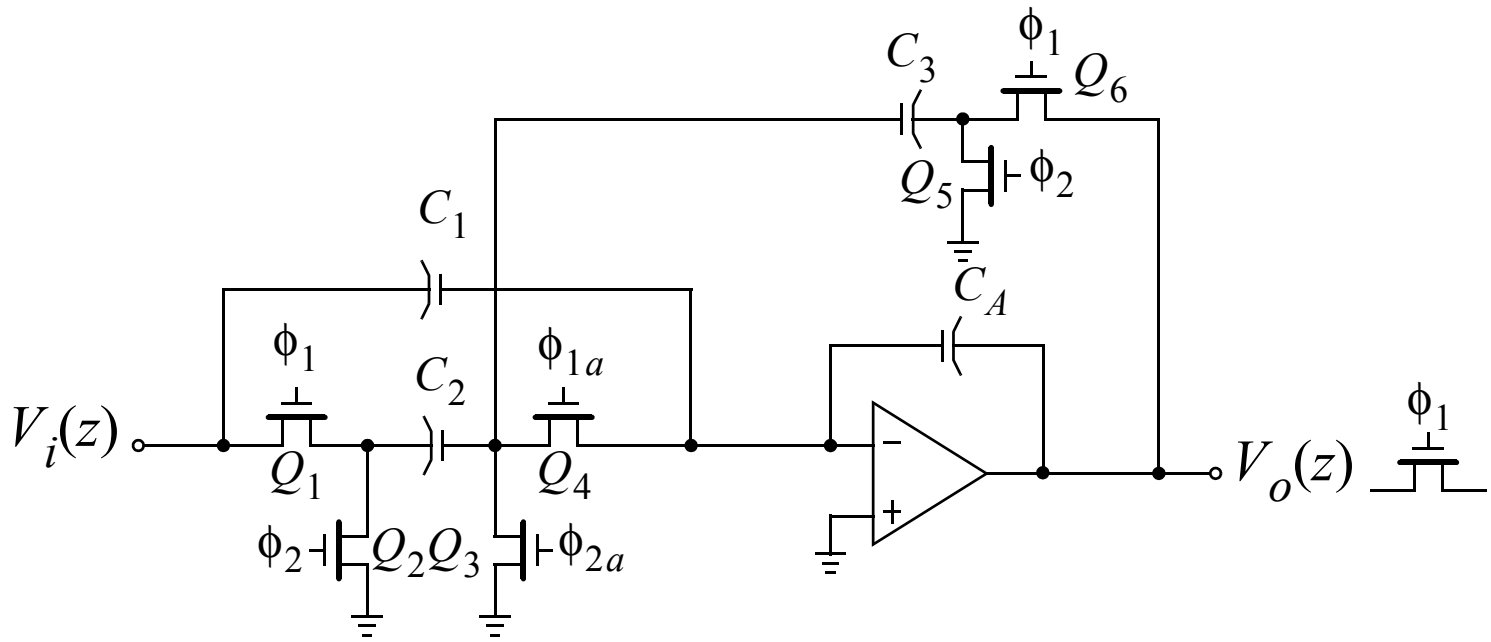
- And, as in lowpass case, can set

$$K_4 = K_5 = \sqrt{1 + b_0 + b_1} \tag{57}$$

- As before, K_4 and K_5 approx $\omega_o T \ll 1$ but $K_6 \cong 1/Q$

Charge Injection

- To reduce charge injection (thereby improving distortion) , turn off certain switches first.



- Advance ϕ_{1a} and ϕ_{2a} so that only their charge injection affect circuit (result is a dc offset)

Charge Injection

- Note: ϕ_{2a} connected to ground while ϕ_{1a} connected to virtual ground, therefore ...

  — can use single n-channel transistors

  — charge injection NOT signal dependent

$$Q_{CH} = -WLC_{ox}V_{eff} = -WLC_{ox}(V_{GS} - V_t) \qquad (58)$$

- Charge related to V_{GS} and V_t and V_t related to substrate-source voltage.
- Source of Q_3 and Q_4 remains at 0 volts — ***amount of charge injected by Q_3, Q_4 is not signal dependent and can be considered as a dc offset***.

Charge Injection Example

- Estimate dc offset due to channel-charge injection when $C_1 = 0$ and $C_2 = C_A = 10C_3 = 10pF$.
- Assume switches Q_3, Q_4 have $V_{tn} = 0.8V$, $W = 30\mu m$, $L = 0.8\mu m$, $C_{ox} = 1.9 \times 10^{-3}\ pF/\mu m^2$, and power supplies are $\pm 2.5V$.
- Channel-charge of Q_3, Q_4 (when on) is

$$Q_{CH3} = Q_{CH4} = -(30)(0.8)(0.0019)(2.5 - 0.8) \qquad (59)$$
$$= -77.5 \times 10^{-3}\ pC$$

- dc feedback keeps virtual opamp input at zero volts.

Charge Injection Example

- Charge transfer into C_3 given by

$$Q_{C_3} = -C_3 v_{out} \tag{60}$$

- We estimate half channel-charges of Q_3, Q_4 are injected to the virtual ground leading to

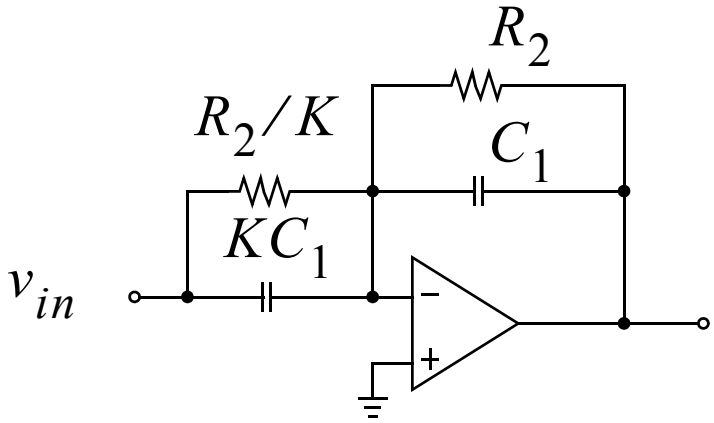
$$\frac{1}{2}(Q_{CH3} + Q_{CH4}) = Q_{C_3} \tag{61}$$

which leads to

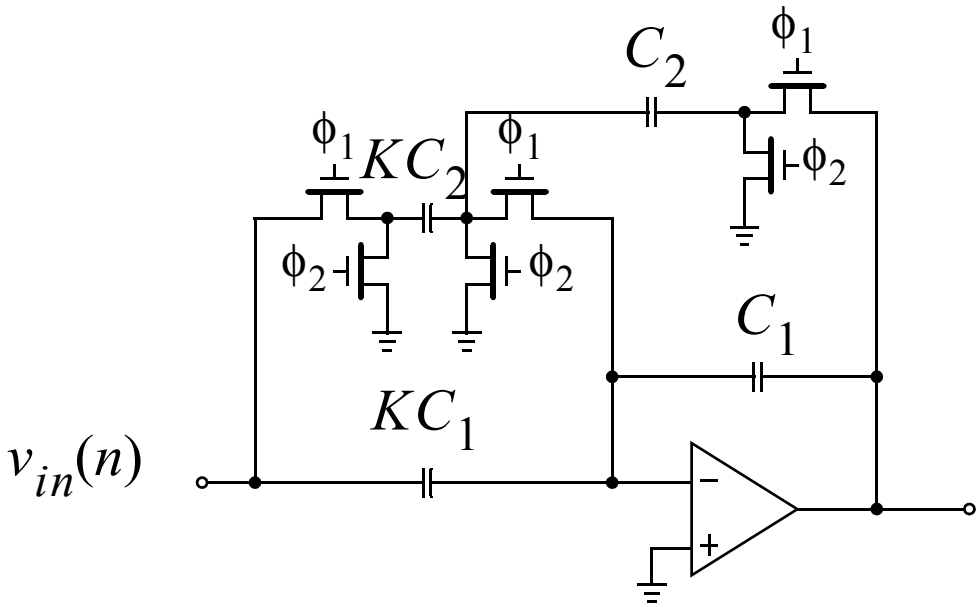
$$v_{out} = \frac{77.5 \times 10^{-3}\ pC}{1pF} = 78\ \text{mV} \tag{62}$$

- dc offset affected by the capacitor sizes, switch sizes and power supply voltage.

SC Gain Circuits — Parallel RC

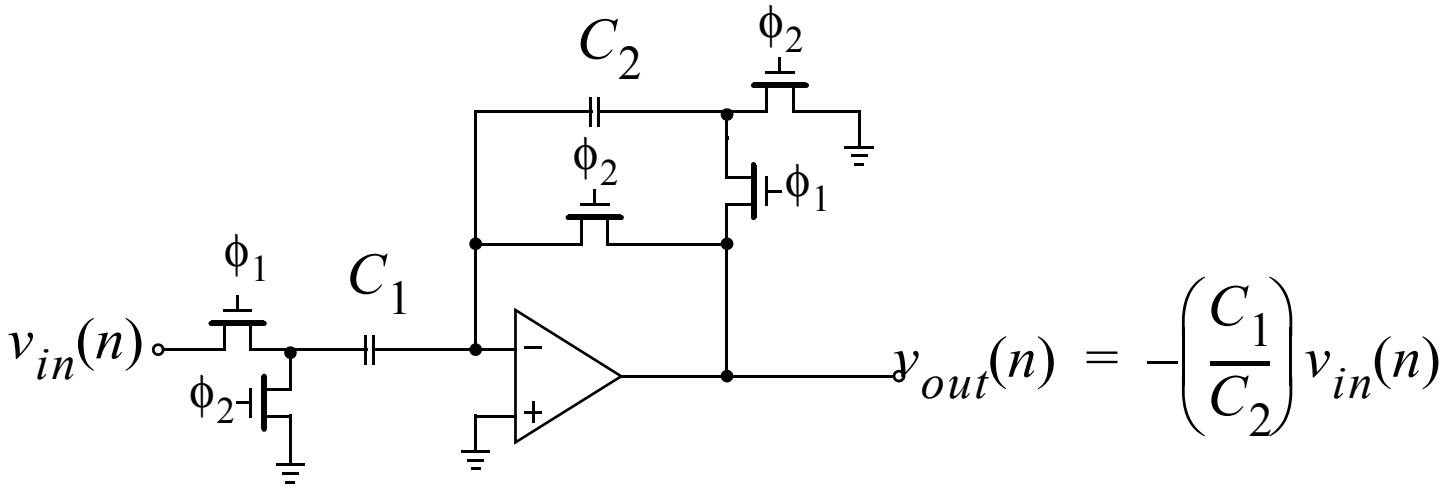


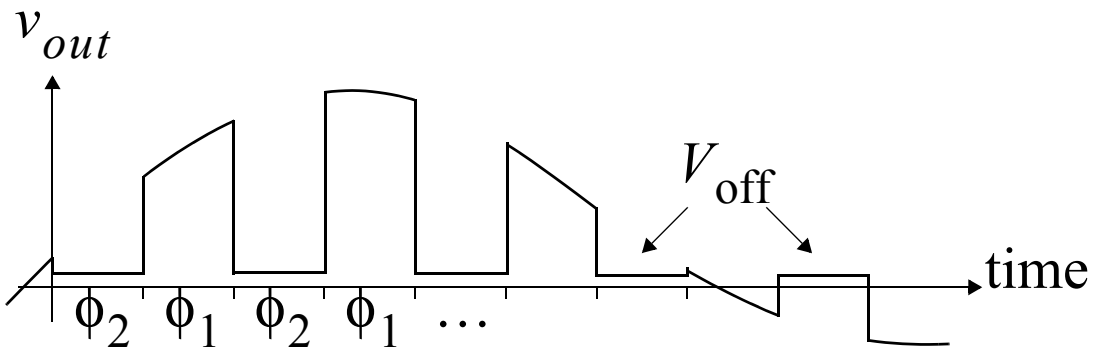
$$v_{out}(t) = -Kv_{in}(t)$$



$$v_{out}(n) = -Kv_{in}(n)$$

SC Gain Circuits — Resettable Gain





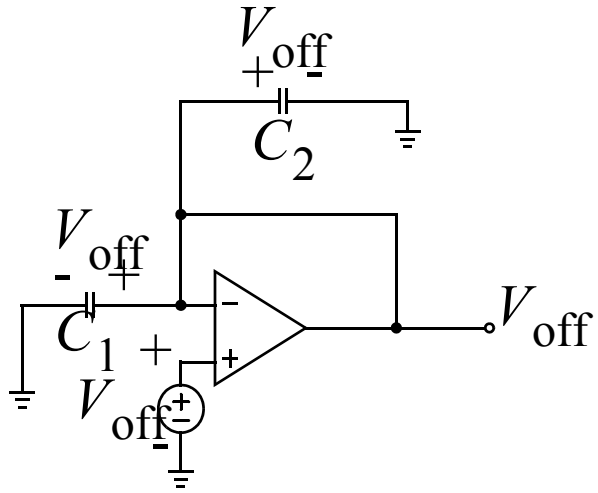
SC Gain Circuits

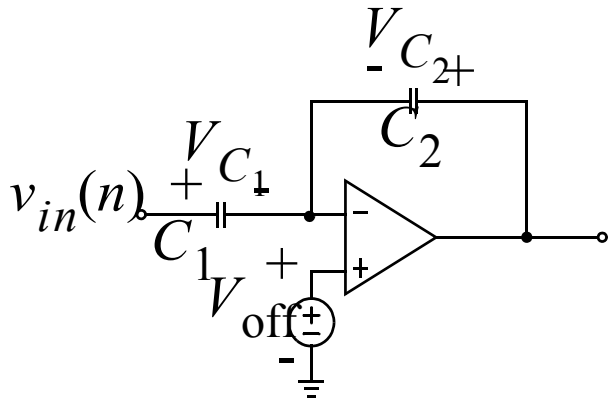
Parallel RC Gain Circuit

- circuit amplifies 1/f noise as well as opamp offset voltage

Resettable Gain Circuit

- performs offset cancellation
- also highpass filters 1/f noise of opamp
- However, requires a high slew-rate from opamp

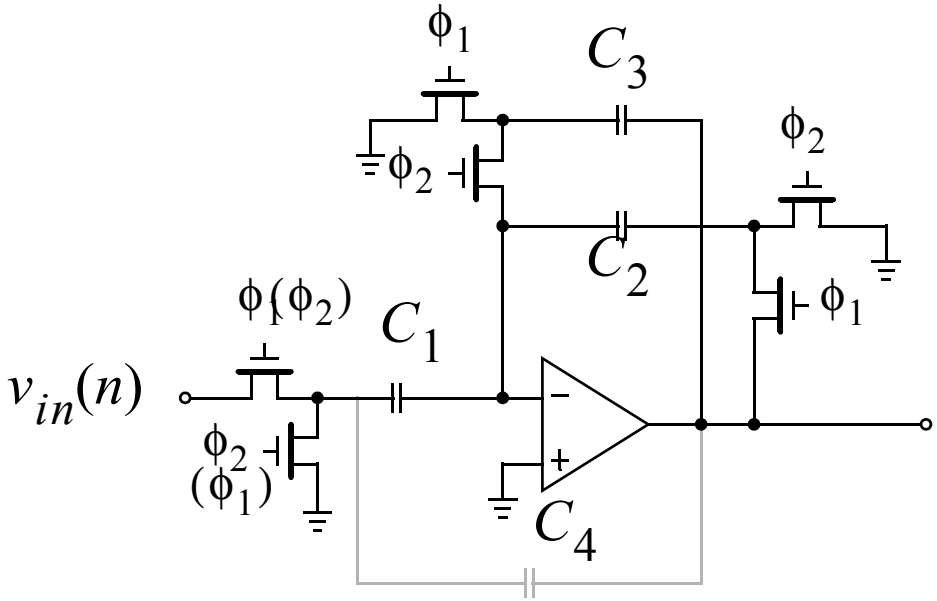




$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$

SC Gain Circuits — Capacitive-Reset

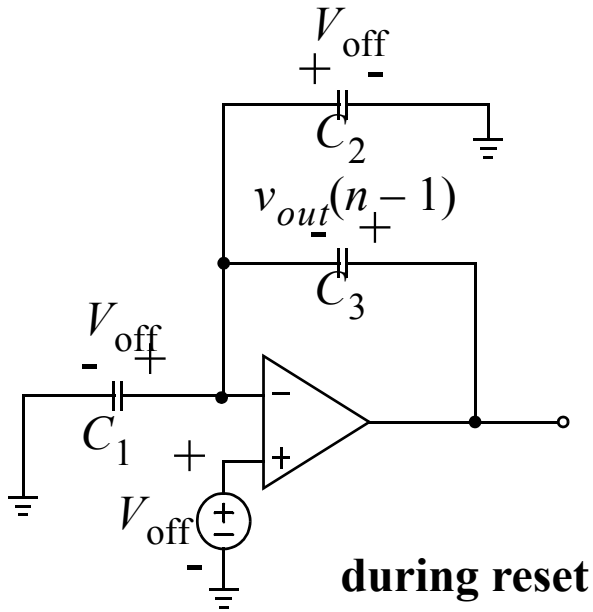
- Eliminate slew problem and still cancel offset by coupling opamp's output to invertering input



$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$

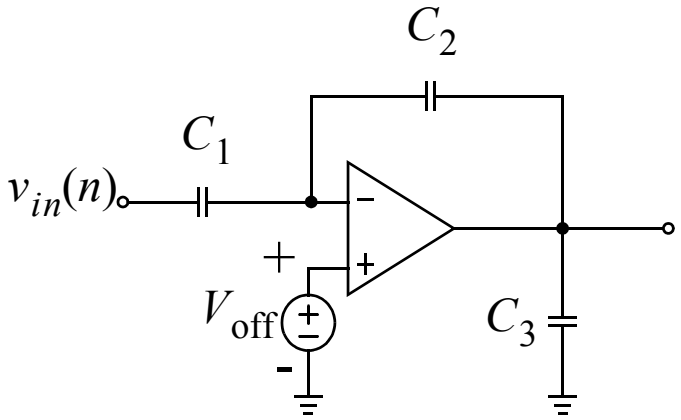
- C_4 is optional de-glitching capacitor

SC Gain Circuits — Capacitive-Reset



$$v_{out}(n-1) + V_{off}$$

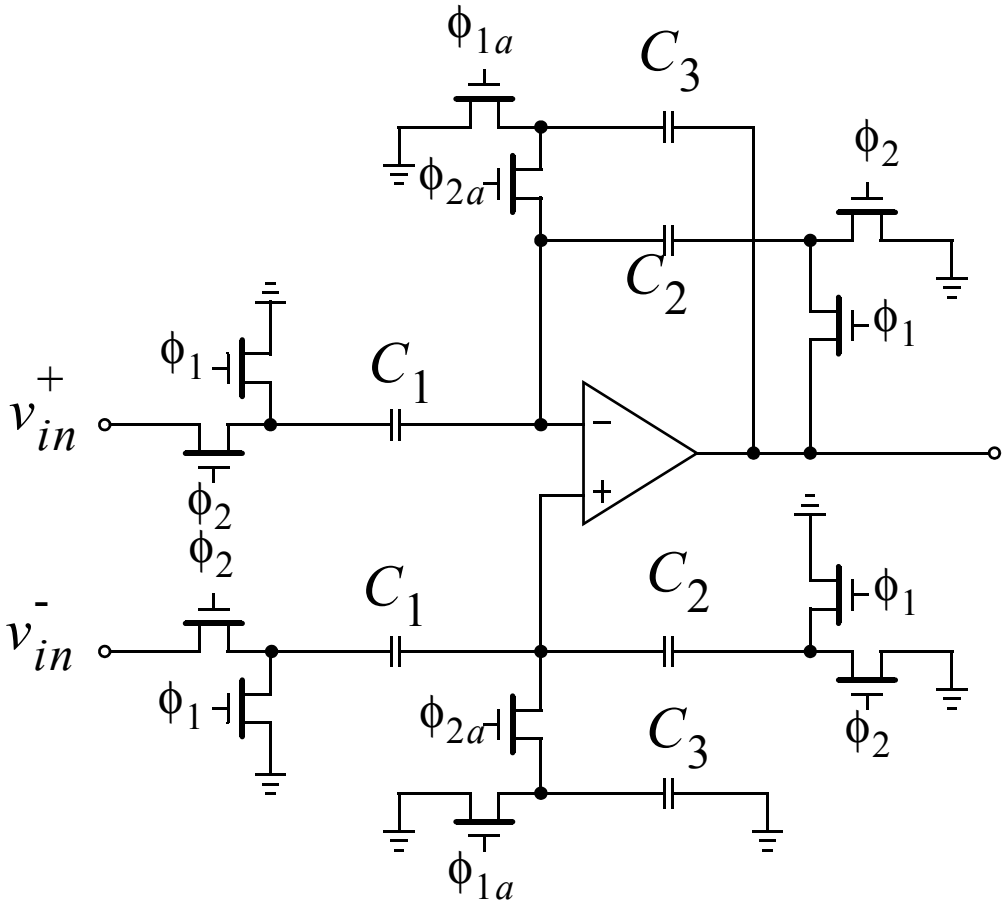
during reset



during valid output

$$v_{out}(n) = -\left(\frac{C_1}{C_2}\right) v_{in}(n)$$

SC Gain Circuits — Differential Cap-Reset



$$v_{out} = \left(\frac{C_1}{C_2}\right)(v_{in}^+ - v_{in}^-)$$

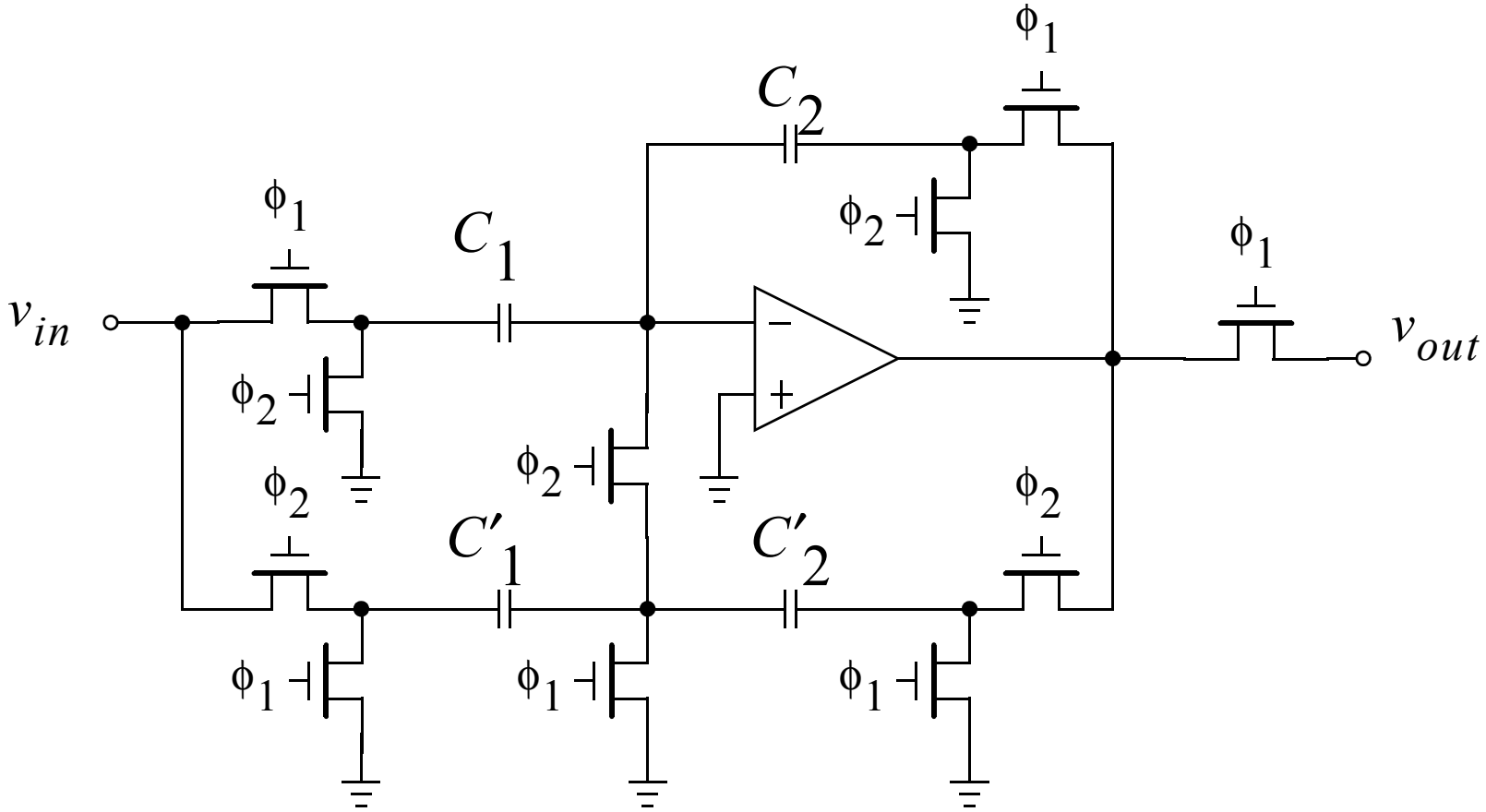
- Accepts differential inputs and partially cancels switch clock-feedthrough

Correlated Double-Sampling (CDS)

- Preceeding SC gain amp is an example of CDS
- Minimizes errors due to opamp offset and 1/f noise
- When CDS used, opamps should have low thermal noise (often use n-channel input transistors)
- Often use CDS in only a few stages
  — input stage for oversampling converter
  — some stages in a filter (where low-freq gain high)

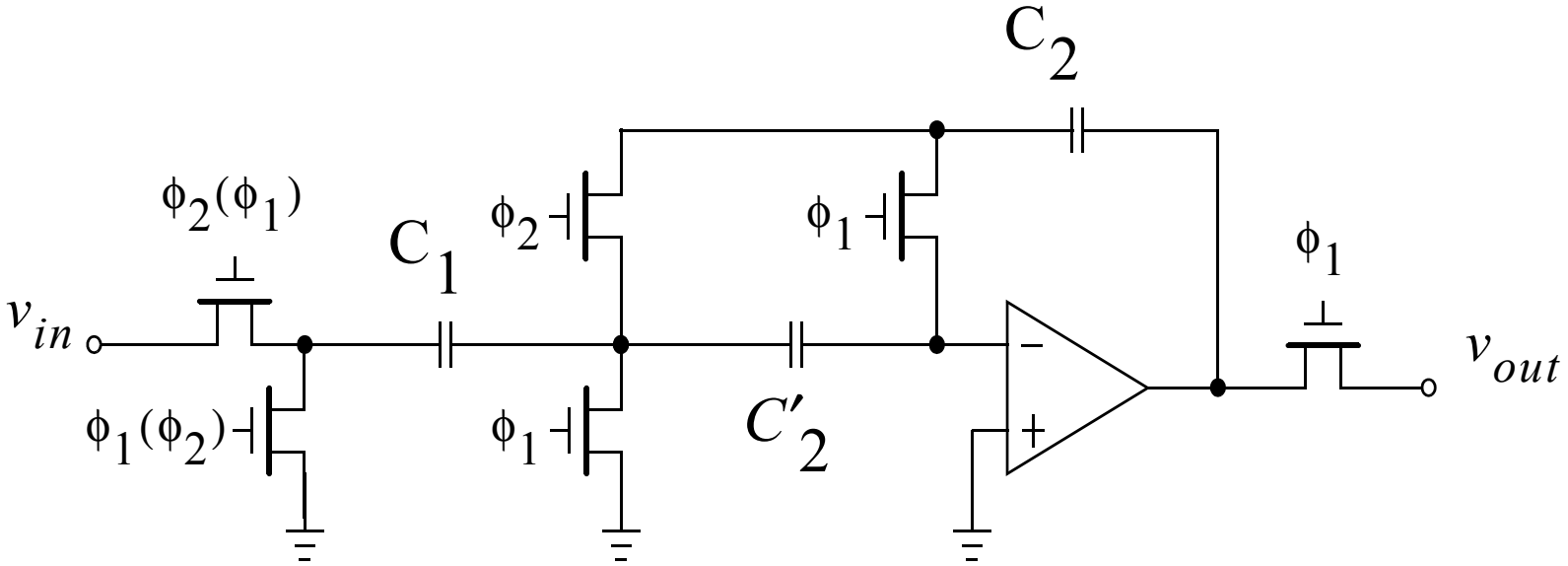
- Basic approach:
  — Calibration phase: store input offset voltage
  — Operation phase: error subtracted from signal

Better High-Freq CDS Amplifier



- ϕ_2 — C_1', C_2' used but include errors
- ϕ_1 — C_1, C_2 used but here no offset errors

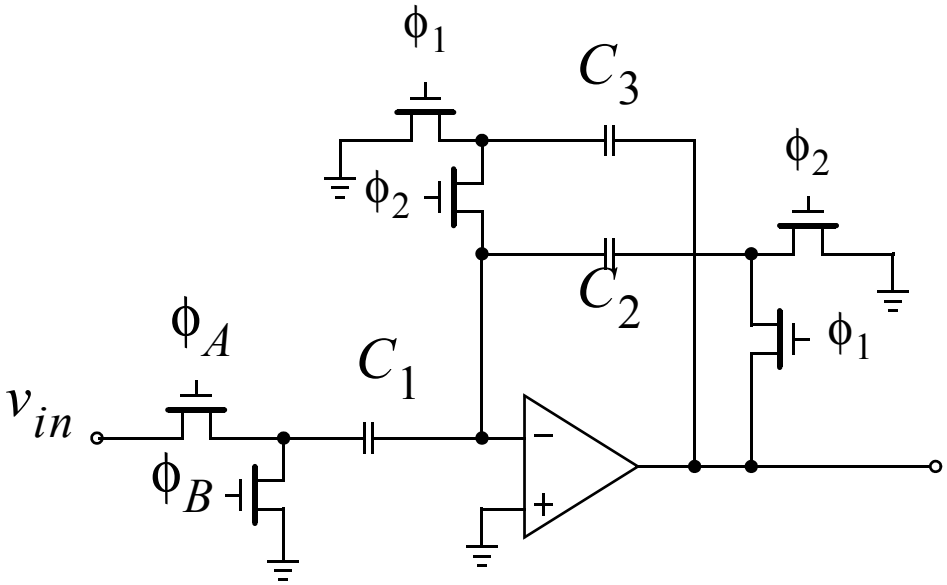
CDS Integrator

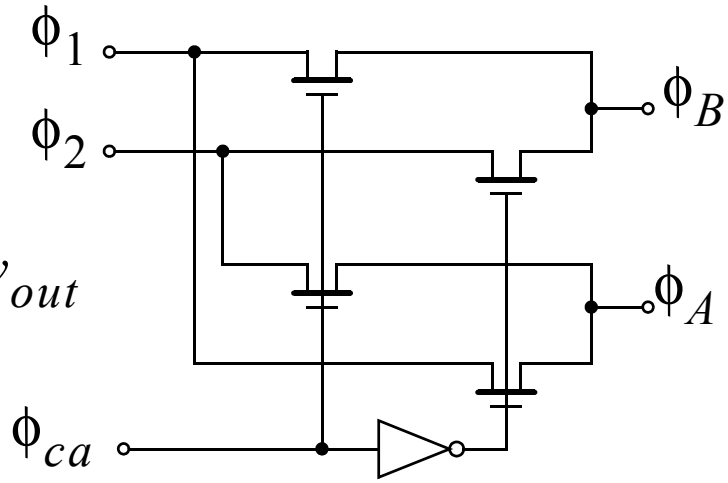


- ϕ_1 — sample opamp offset on C_2'
- ϕ_2 — C_2' placed in series with opamp to reduce error
- Offset errors reduced by opamp gain
- Can also apply this technique to gain amps

SC Amplitude Modulator

- Square wave modulate by ±1 (i.e. $V_{out} = \pm V_{in}$)

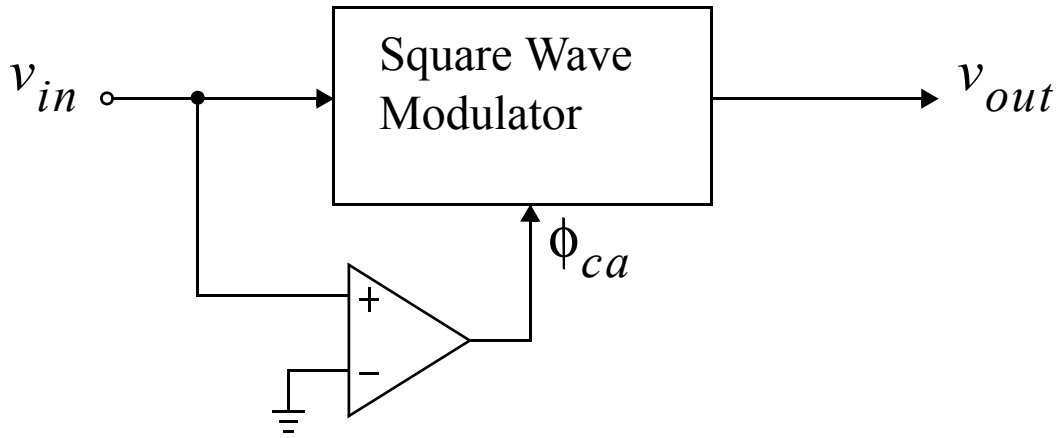




$$\phi_A = (\phi_2 \cdot \phi_{ca}) + (\overline{\phi_1} \cdot \phi_{ca})$$
$$\phi_B = (\phi_1 \cdot \phi_{ca}) + (\overline{\phi_2} \cdot \phi_{ca})$$

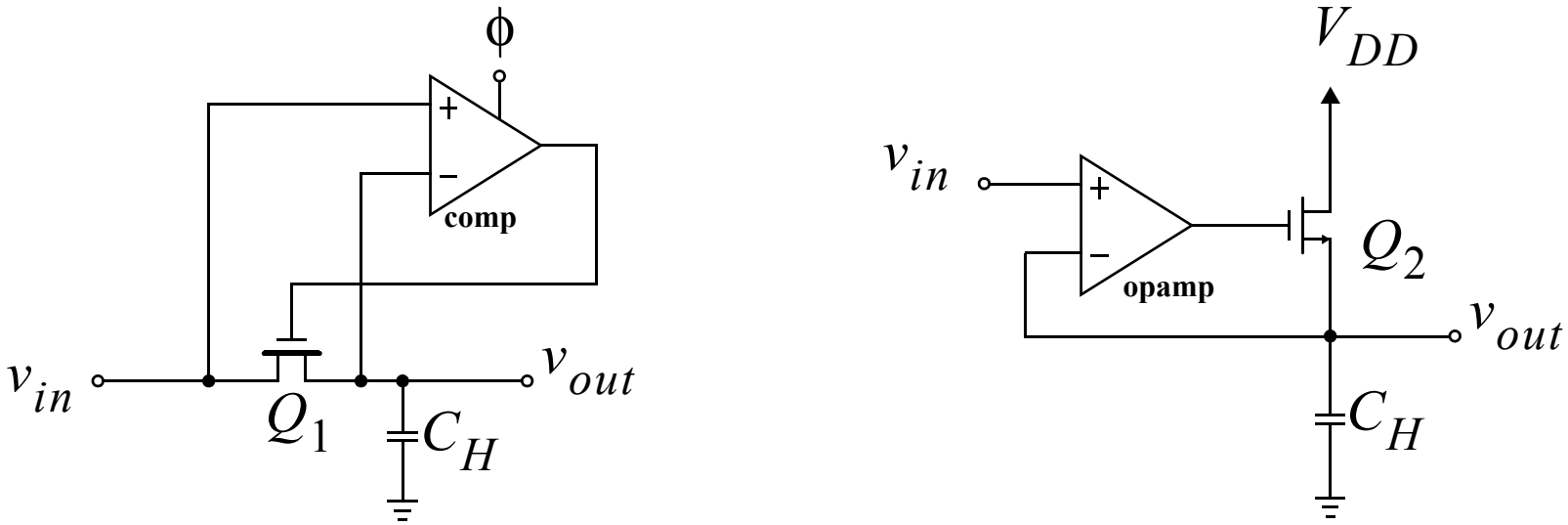
- Makes use of cap-reset gain circuit.
- ϕ_{ca} is the modulating signal

SC Full-Wave Rectifier



- Use square wave modulator and comparator to make
- For proper operation, comparator output should changes synchronously with the sampling instances.

SC Peak Detector



- Left circuit can be fast but less accurate
- Right circuit is more accurate due to feedback but slower due to need for compensation (circuit might also slew so opamp's output should be clamped)