Basic Opamp Design and Compensation

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Transistor Model Summary

General Constants

Transistor charge — $q = 1.602 \times 10^{-19}$ C

Boltzman constant — $k = 1.38 \times 10^{-23}$ JK^{-1}

Intrinsic silicon carrier concentration (300 K)— $n_i = 1.1 \times 10^{16}$ carriers/m^3

Relative permittivity of oxide — $K_{ox} \cong 3.9$

Relative permittivity of silicon — $K_s \cong 11.8$

MOS Transistor Parameters

Electron mobility (typical) — $\mu_n = 0.05$ m^2/V $\cdot$ s

Hole mobility (typical) — $\mu_p = 0.02$ m^2/V $\cdot$ s

Oxide thickness (typical) — $t_{ox} = 0.02$ μm

Transistor Model Summary

Gate capacitance per unit area — $C_{ox} = \dfrac{K_{ox}\varepsilon_o}{t_{ox}} \approx 1.9 \times 10^{-3}\ \text{pF/}(\mu\text{m})^2$

Device parameters (typ) — $\mu_n C_{ox} = 90\ \mu\text{A/V}^2, \mu_p C_{ox} = 30\ \mu\text{A/V}^2$

Threshold voltages (typical) — $V_{tn} = 0.8\ \text{V}, V_{tp} = -0.9\ \text{V}$

Threshold voltage adjustment — $V_{tn} = V_{tn\text{-}0} + \gamma(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F})$

Body effect parameter (typical) — $\gamma = 0.5\ \text{V}^{1/2}$

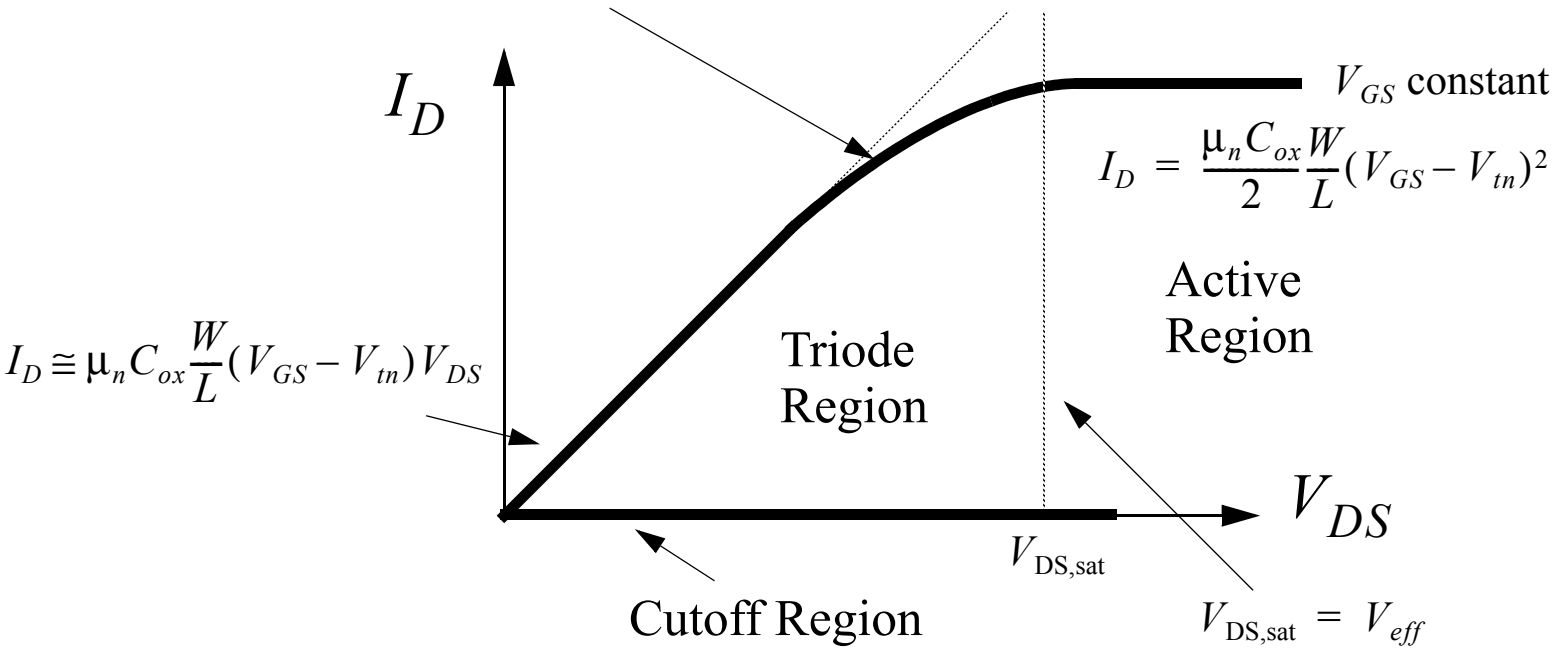
Fermi potential difference (typical) — $\phi_F = 0.35\ \text{V}$

Effective Gate-Source Voltage, V_{eff}

Effective gate-source voltage — $V_{eff} \equiv V_{GS} - V_{tn}$

Triode and Active Regions

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^2}{2}\right]$$



- Cutoff Region: $V_{GS} < V_{tn}$
- Triode Region: $V_{GS} > V_{tn}$, $V_{DS} \leq V_{eff}$
- Active Region: $V_{GS} > V_{tn}$, $V_{DS} \geq V_{eff}$

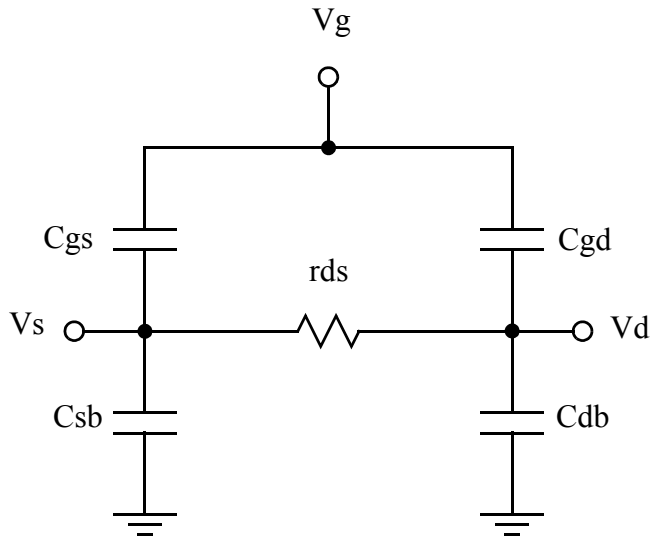
MOS Triode Equations

Region of operation — $V_{GS} > V_{tn}$, $V_{DS} \le V_{eff}$

Drain current — $$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{tn})V_{DS} - 1.7\frac{V_{DS}^2}{2}\right]$$

1.7 typical term is due to body effect along channel

Small-Signal Model in Triode Region (for $V_{DS} << V_{eff}$)



$$r_{ds} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)V_{eff}}$$

MOS Active (or Pinch-Off) Equations

Region of operation — $V_{GS} > V_{tn}$, $V_{DS} \geq V_{eff}$

Drain current — $$I_D = \left(\frac{\mu_n C_{ox}}{2}\right)\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2[1 + \lambda(V_{DS} - V_{eff})]$$

Output impedance constant — $$\lambda \propto \frac{1}{L\sqrt{V_{DG} + V_{tn} + 0.9}}$$

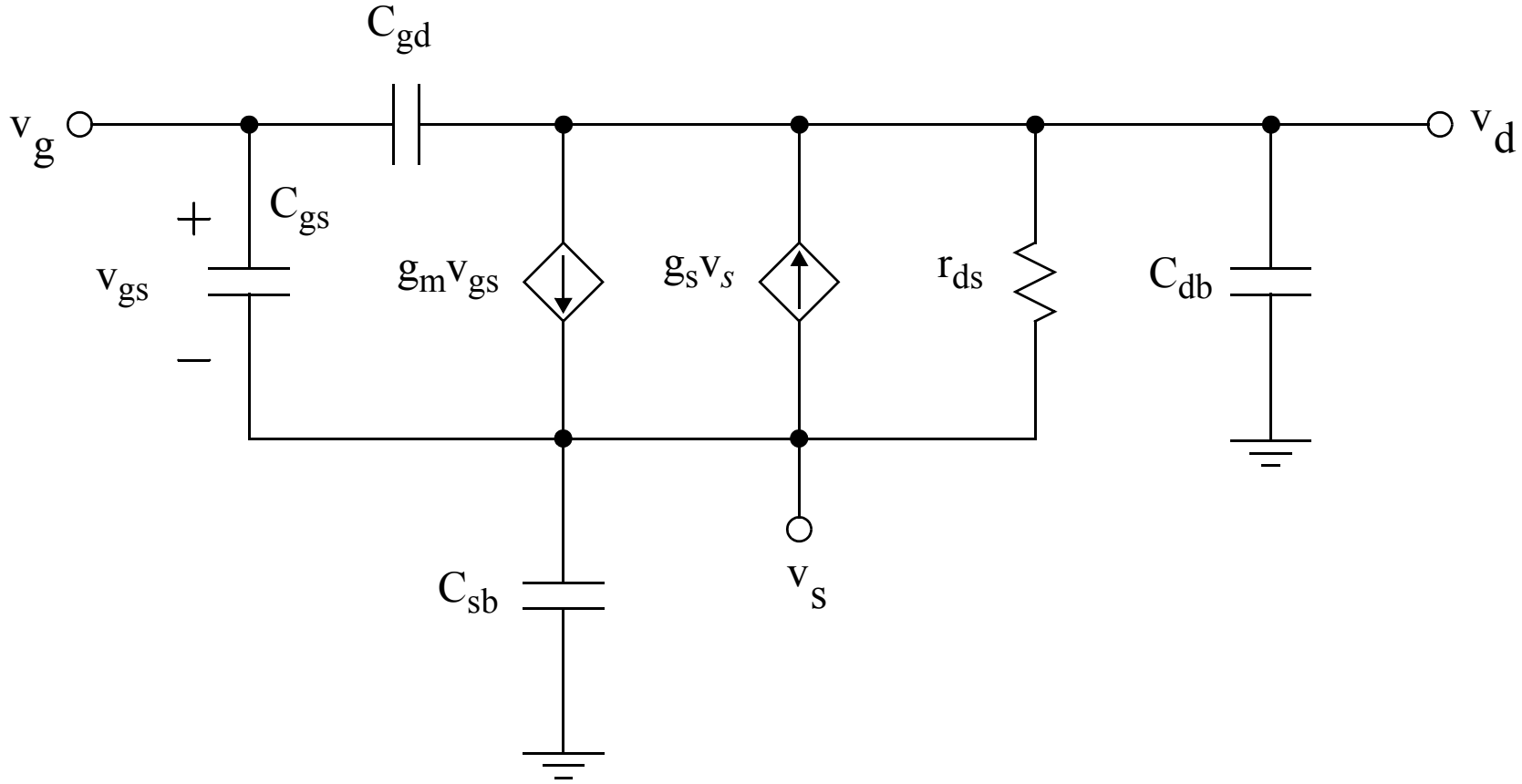
0.9 term is due to built-in junction potential

Effective gate-source voltage — $$V_{eff} = V_{GS} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

(ignoring output impedance)

MOS Active Equations

Small-Signal Model (Active Region)



MOS Active Equations

Transconductance — $g_m = \mu_n C_{ox}\left(\frac{W}{L}\right) V_{eff}$

Transconductance — $g_m = \sqrt{2\mu_n C_{ox}(W/L) I_D}$

Transconductance — $g_m = \frac{2I_D}{V_{eff}}$

Body effect transconductance — $g_s = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$

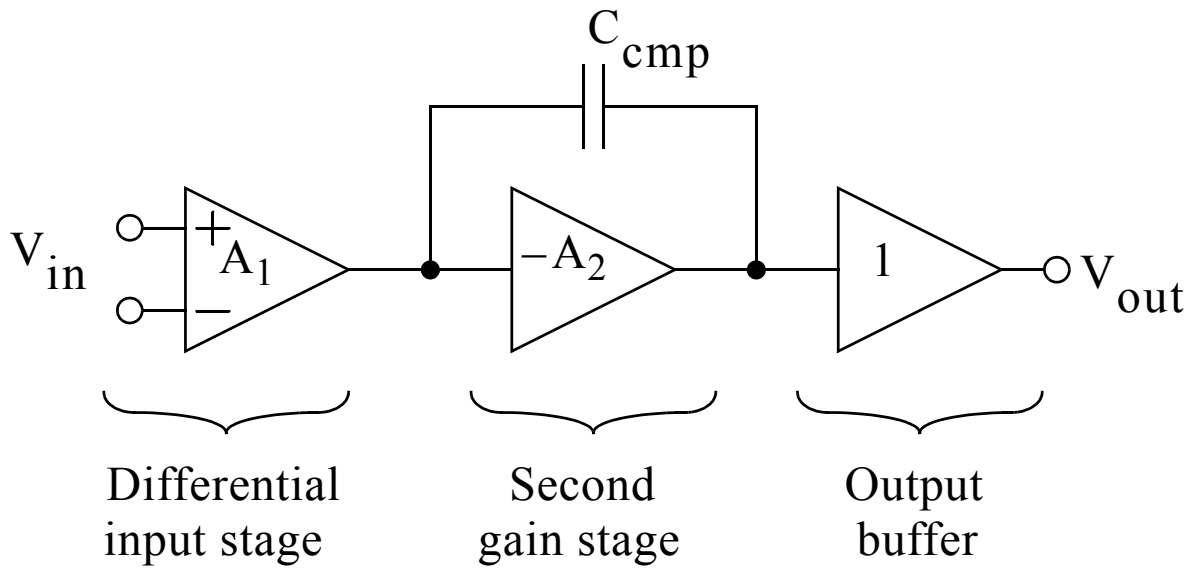
Body effect transconductance (typical) — $g_s \cong 0.2 g_m$

Output impedance — $r_{ds} = \frac{1}{\lambda I_D}$

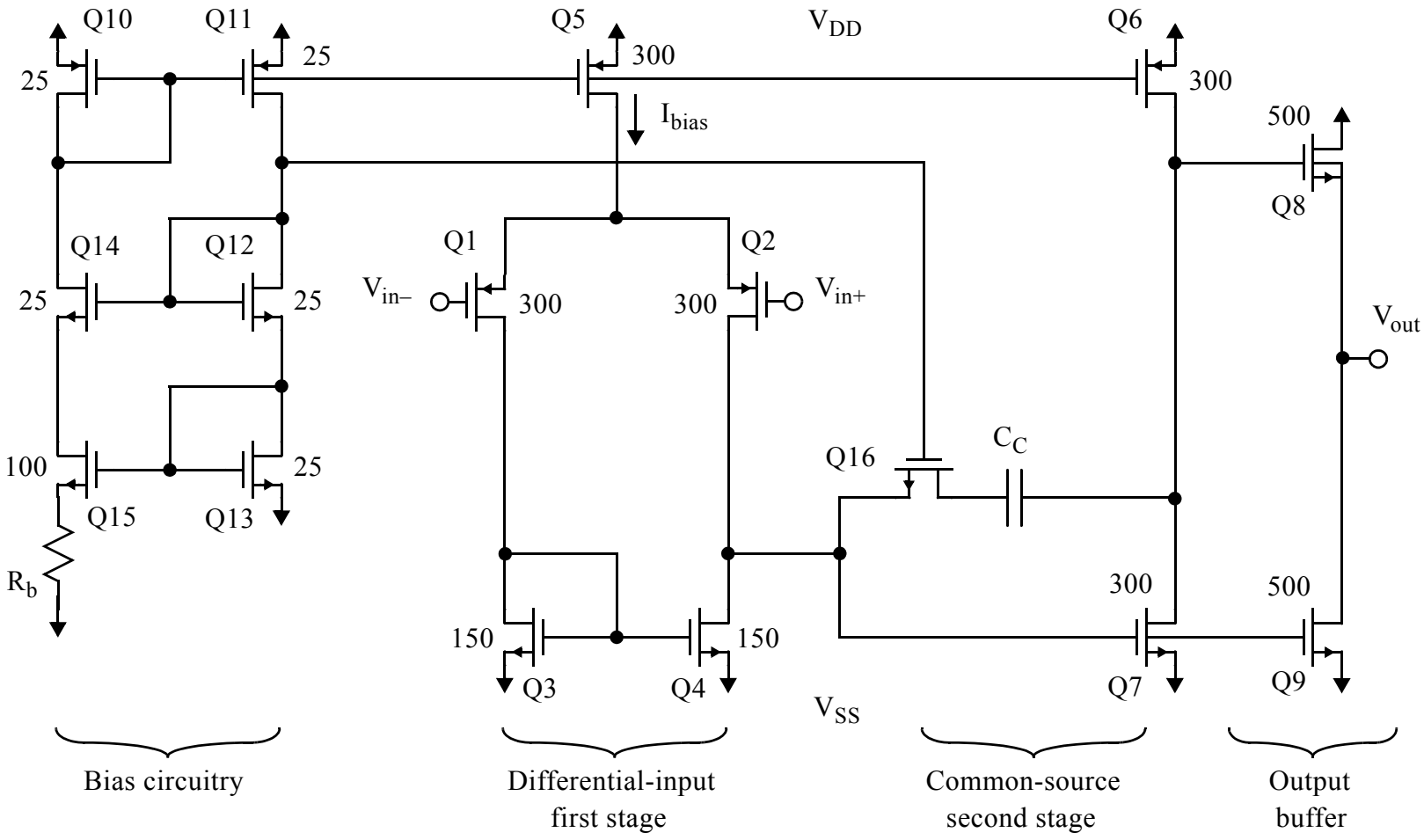
Output impedance — $r_{ds} \approx \alpha \frac{L}{I_D}\sqrt{V_{DG} + V_{tn}}$ where $\alpha = 5 \times 10^6 \sqrt{\text{V}}/\text{m}$

Two-Stage CMOS Opamp

- Useful for describing many opamp design concepts
- Still used for low voltage applications



Two-Stage CMOS Opamp



all transistor lengths = 1.6 um

Opamp Gain

- 3rd stage NOT included if driving capacitive loads
- Typical gains of 50-100 for each of stage 1 and 2

First Stage

- Differential to single-ended

$$A_{v1} = g_{m1}(r_{ds2} \parallel r_{ds4}) \tag{1}$$

$$g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 \frac{I_{bias}}{2}} \tag{2}$$

Second Stage

- Common-source gain

$$A_{v2} = -g_{m7}(r_{ds6} \parallel r_{ds7}) \tag{3}$$

Opamp Gain

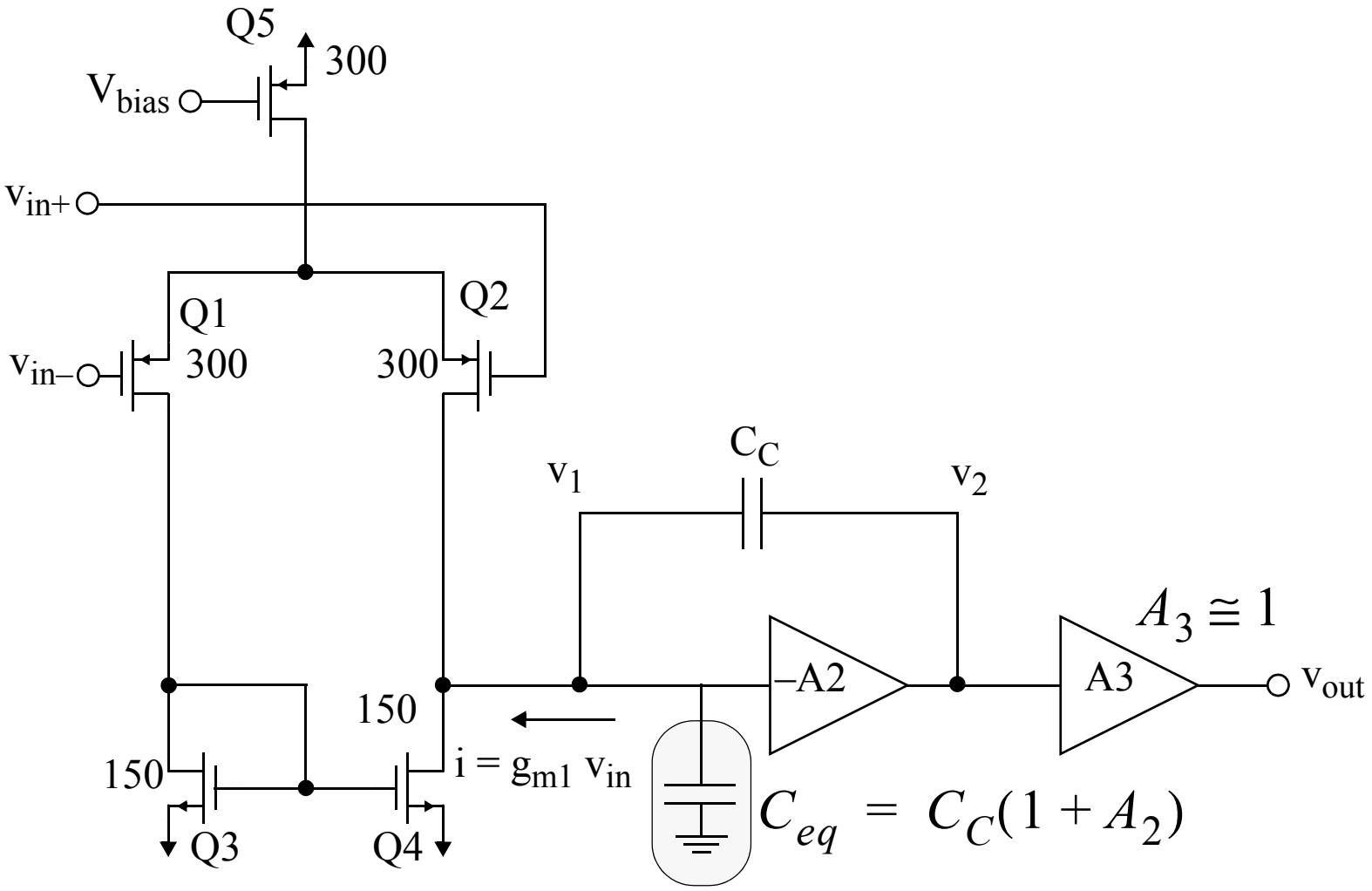
Third Stage

- Source follower
- Typical gain — slightly less than 1 (say 0.9)
- Note — $g_{ds} = 1/r_{ds}$ and $G_L = 1/R_L$

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{s8} + g_{ds8} + g_{ds9}} \tag{4}$$

- g_s is body-effect conductance and equals zero if source tied to substrate
- G_L is the load conductance at output

Frequency Response



Frequency Response

- C_C dominates at all freq except unity-gain freq
- Ignore Q_{16} for now (used for lead compensation)
- Miller effect results in

$$(C_{eq} = C_C(1 + A_2)) \cong C_C A_2 \tag{5}$$

- At midband freq

$$A_1 = g_{m1} Z_{out} = g_{m1} / (sC_C A_2) \tag{6}$$

- Overall gain (assuming $A_3 \cong 1$)

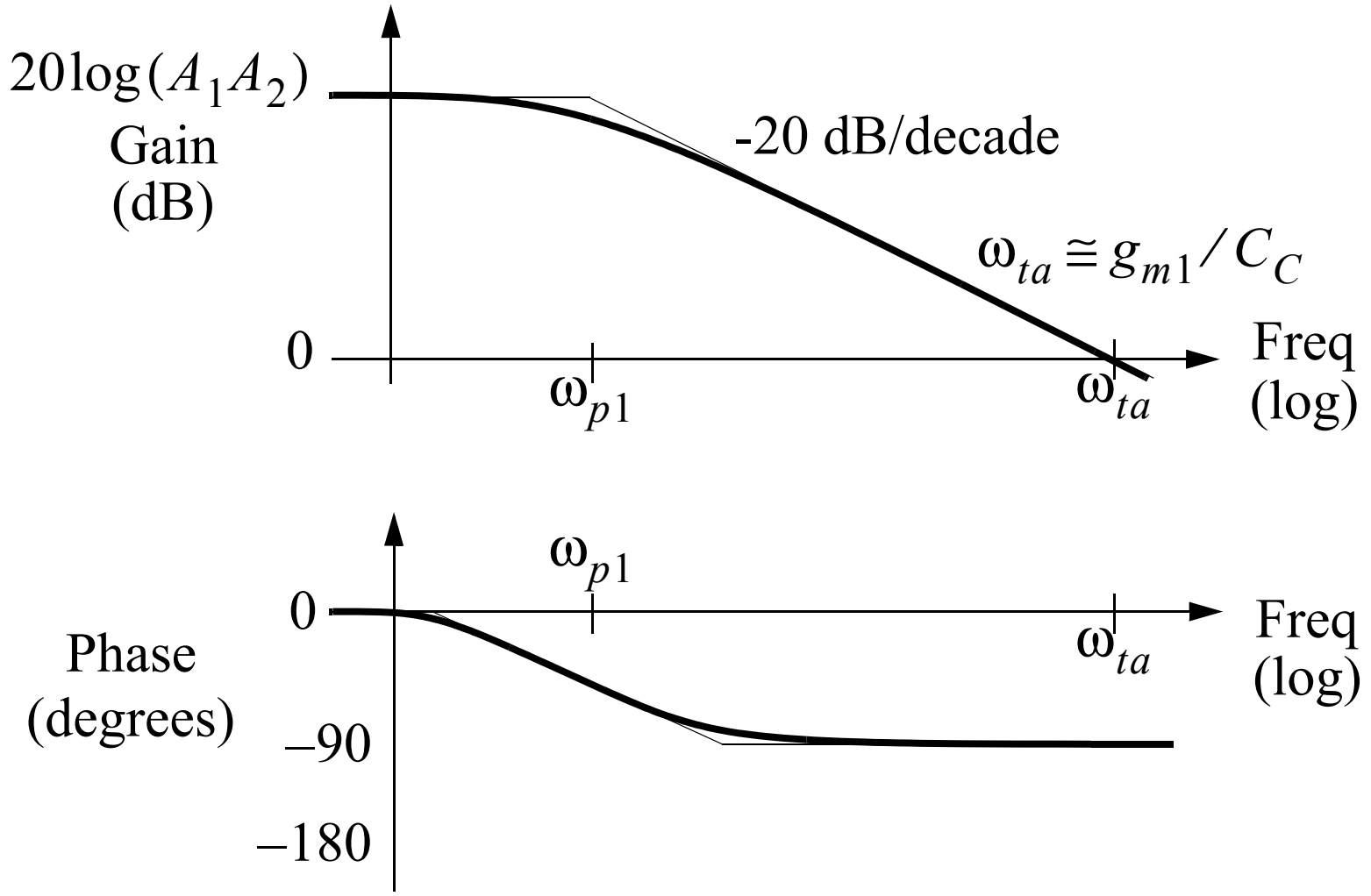
$$A_v(s) = A_2 A_1 = g_{m1} / (sC_C) \tag{7}$$

resulting in a unity-gain frequency of

$$\omega_{ta} = g_{m1} / C_C \tag{8}$$

Freq Response

- First-order model



Slew Rate

- Max rate output changes when input signal large
- All Q5 bias current goes into Q1 or Q2

$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{\max} = \frac{I_{C_C}|_{\max}}{C_C} = \frac{I_{D5}}{C_C} = \frac{2I_{D1}}{C_C} \tag{9}$$

I_{D1} is nominal bias current of input transistors

- Using $C_C = g_{m1}/\omega_{ta}$ and $g_{m1} = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_1 I_{D1}}$

Slew Rate

$$SR = \frac{2I_{D1}}{\sqrt{2\mu_p C_{ox}(W/L)_1 I_{D1}}}\omega_{ta} = V_{eff1}\omega_{ta} \qquad (10)$$

where $V_{eff1} = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}}$

- Normally, little control over ω_{ta} for a given power diss
- Increase slew-rate by increasing V_{eff1}
- This is one of main reasons for using p-channel input stage — higher slew-rate

Systematic Offset Voltage

- To ensure inherent offset voltage does not exist, design should satisfy

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5} \tag{11}$$

- Ensures nominal current through Q7 equals Q6
- Found by noting

$$I_{D5} = 2I_{D3} = 2I_{D4} \tag{12}$$

and

$$V_{GS7} = V_{DS3} = V_{GS4} \tag{13}$$

then setting $I_{D7} = I_{D6}$

N-Channel or P-Channel Input Stage

- Can also build complement opamp with an n-channel input diff pair and second-stage p-channel stage

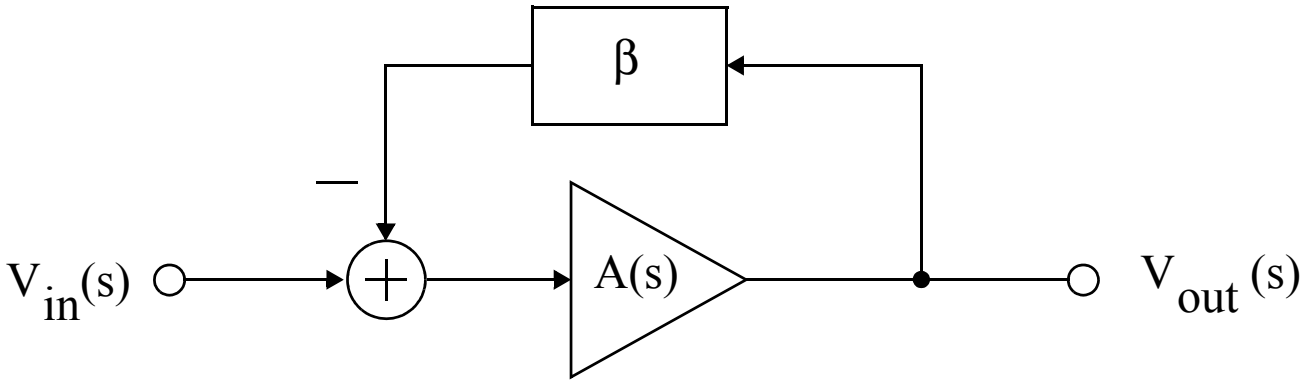
P-channel Advantages

- Higher slew-rate — For fixed bias current, V_{eff} is larger (assuming similar widths used for max gain)
- Higher unity-gain freq — higher transconductance of second stage which is proportional to unity-gain freq
- Lower 1/f noise — holes less likely to be trapped — p-channel transistors have lower 1/f noise

N-channel Advantage

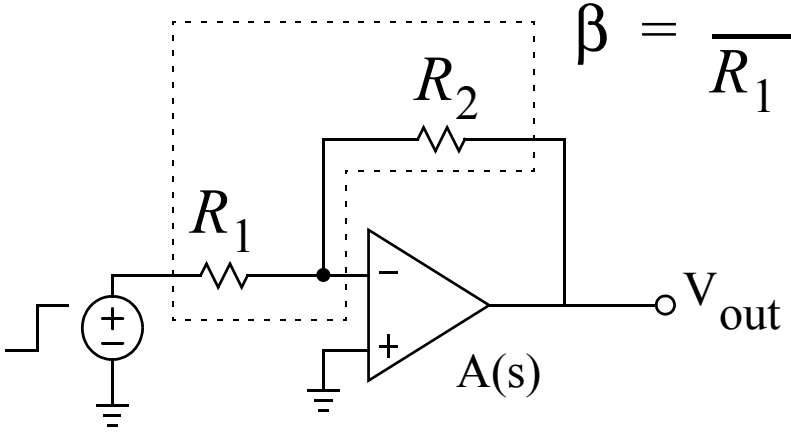
- Lower thermal noise — thermal noise is lowered by high transconductance of first stage

Opamp Compensation

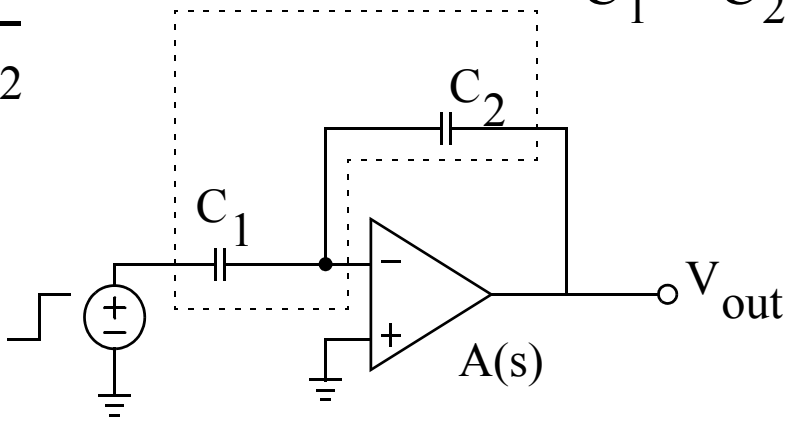


- Feedback circuit β assumed to be freq independent

$$\beta = \frac{R_1}{R_1 + R_2}$$



$$\beta = \frac{C_2}{C_1 + C_2}$$



General Opamp Compensation

- Model A(s) by

$$A(s) = \frac{A_0}{(1 + s/\omega_{p1})(1 + s/\omega_{eq})} \tag{14}$$

- ω_{p1} — first dominant-pole frequency
- ω_{eq} — pole frequency modelling higher-freq poles.
- ω_{eq} found from simulation — frequency with –135° phase shift (–90° due to ω_{p1} and another –45° due to higher-frequency poles and zeros)
- Closed loop gain given by

$$A_{CL}(s) = \frac{A(s)}{1 + \beta A(s)} \tag{15}$$

General Opamp Compensation

$$A_{CL}(s) = \frac{A_{CL0}}{1 + \frac{s(1/\omega_{p1} + 1/\omega_{eq})}{1+\beta A_0} + \frac{s^2}{(1+\beta A_0)(\omega_{p1}\omega_{eq})}} \qquad (16)$$

where $A_{CL0} = A_0/(1+\beta A_0) \cong 1/\beta$

- Compare to a general second-order equation

$$H_2(s) = \frac{K\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2} = \frac{K}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \qquad (17)$$

$$\% \text{ overshoot} = 100e^{\frac{-\pi}{\sqrt{4Q^2-1}}} \qquad (18)$$

General Opamp Compensation

- Equating 2 equations above results in

$$\omega_0 = \sqrt{(1+\beta A_0)(\omega_{p1}\omega_{eq})} \cong \sqrt{\beta A_0 \omega_{p1}\omega_{eq}} \tag{19}$$

$$Q = \frac{\sqrt{(1+\beta A_0)/\omega_{p1}\omega_{eq}}}{1/\omega_{p1}+1/\omega_{eq}} \cong \sqrt{\frac{\beta A_0 \omega_{p1}}{\omega_{eq}}} \tag{20}$$

- To find relationship between Q and phase-margin we look at the loop gain, $LG(s)$

$$LG(s) = \beta A(s) = \frac{\beta A_0}{(1+s/\omega_{p1})(1+s/\omega_{eq})} \tag{21}$$

- To find a relationship for the loop-gain unity-gain freq

$$\left|LG(j\omega_t)\right| = 1 \tag{22}$$

General Opamp Compensation

- And rearrange and use approx that $\omega_t \gg \omega_{p1}$

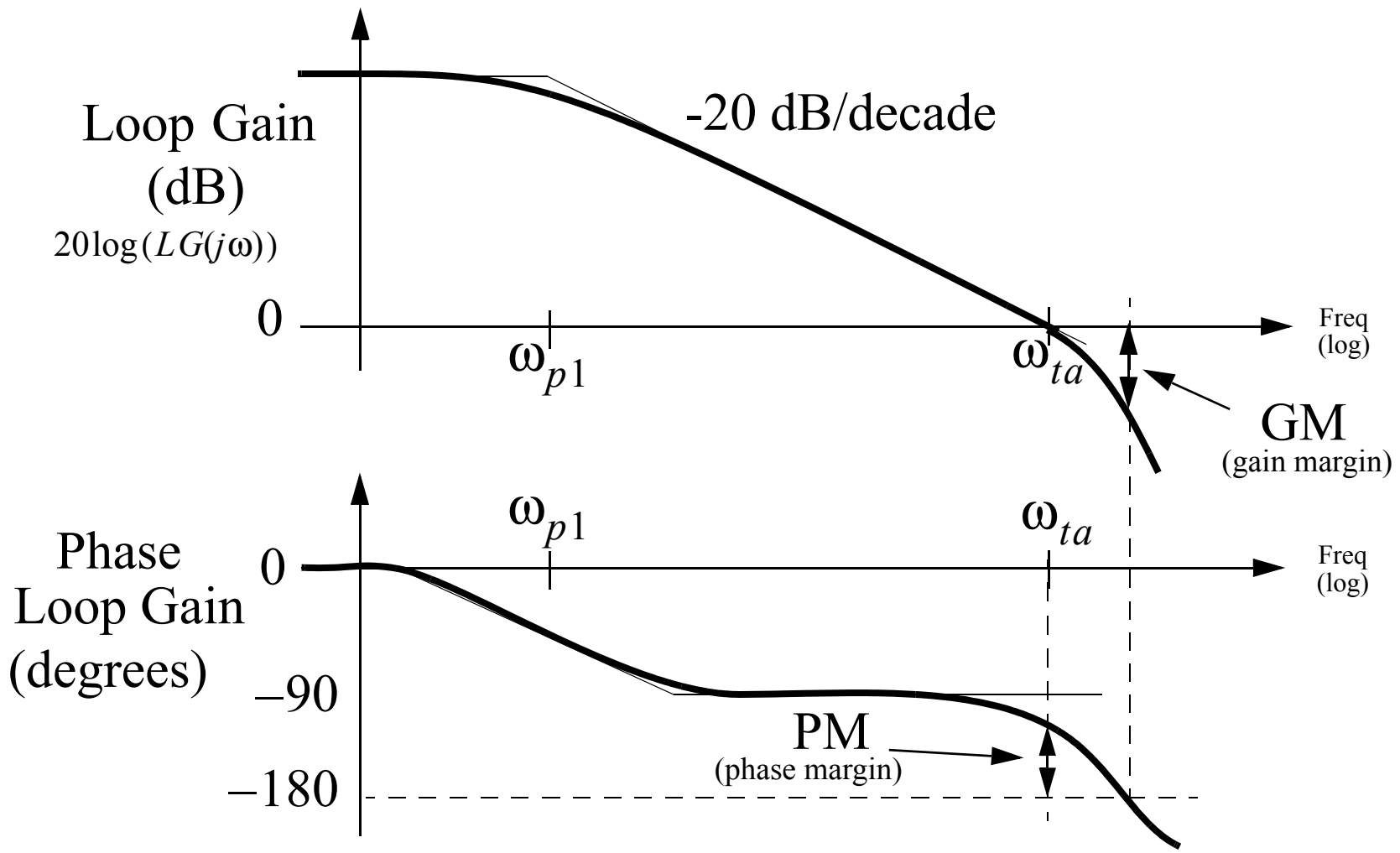
$$\frac{\beta A_0 \omega_{p1}}{\omega_{eq}} = \left(\frac{\omega_t}{\omega_{eq}}\right)\sqrt{1+\left(\frac{\omega_t}{\omega_{eq}}\right)^2} \tag{23}$$

so that

$$Q = \sqrt{\left(\frac{\omega_t}{\omega_{eq}}\right)\sqrt{1+\left(\frac{\omega_t}{\omega_{eq}}\right)^2}} \tag{24}$$

- Would also like to relate ***phase-margin*** with ω_t/ω_{eq} and Q factor

Phase-Margin



General Opamp Compensation

$$PM = \angle LG(j\omega_t) - (-180°) = 90° - \tan^{-1}(\omega_t/\omega_{eq}) \quad (25)$$

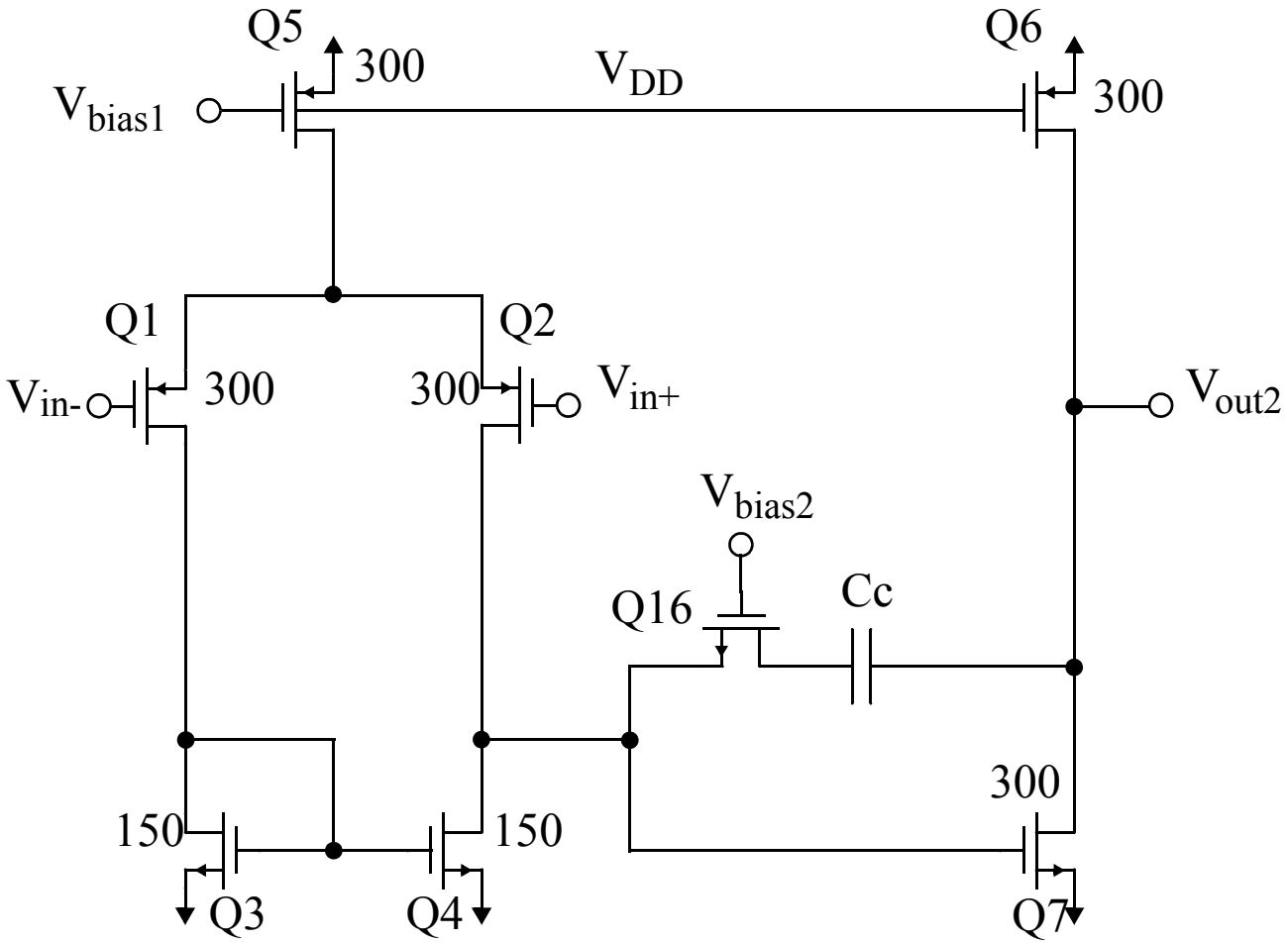
where ω_{p1} adds 90° phase shift

$$\omega_t/\omega_{eq} = \tan(90° - PM) \quad (26)$$

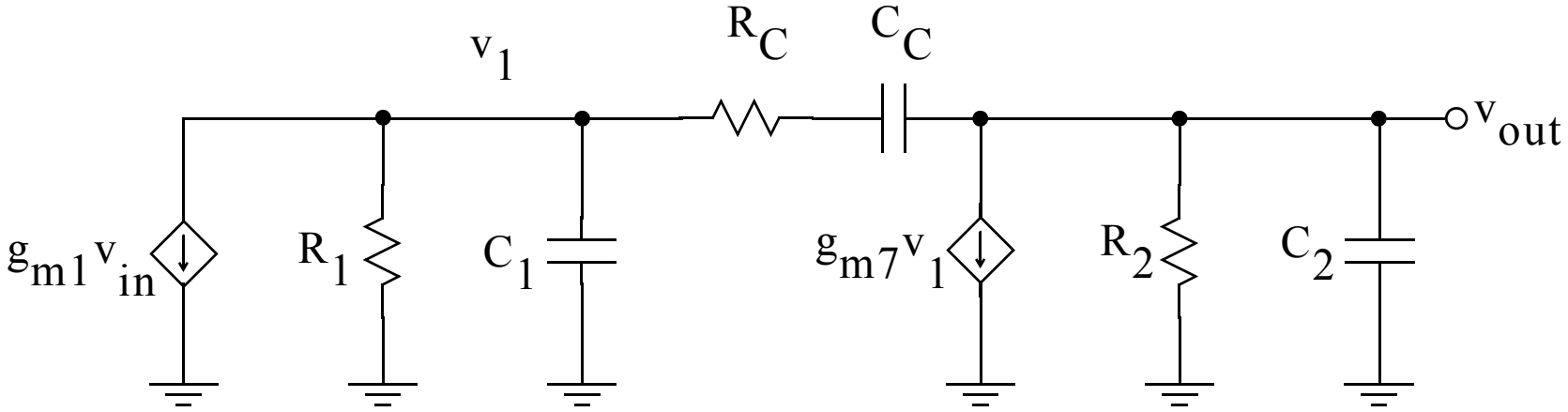
- If non-dominant poles remains unchanged, ω_t independent of β for optimally compensated circuit!

PM (Phase margin)	ω_t/ω_{eq}	Q factor	Percentage overshoot for a step input
55°	0.700	0.925	13.3%
60°	0.580	0.817	8.7%
65°	0.470	0.717	4.7%
70°	0.360	0.622	1.4%
75°	0.270	0.527	0.008%

Compensating the 2-Stage Opamp



Compensating the 2-Stage Opamp



- Q_{16} has $V_{DS16} = 0$ and is hard in the triode region.

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff16}} \tag{27}$$

- Small signal analysis — without R_C present, right-half plane zero occurs and worsens phase-margin

Compensating the 2-Stage Opamp

- Including R_C (through Q16) places zero at

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)} \tag{28}$$

- Zero moved to left-half plane to aid compensation
- Good practical choice is

$$\omega_z = 1.2\omega_t \tag{29}$$

satisfied by letting

$$R_C \cong \frac{1}{1.2g_{m1}} \tag{30}$$

since $\omega_t \cong g_{m1}/C_C$ and $\omega_z \cong 1/(R_C C_C)$ if $R_C \gg 1/g_{m7}$

Design Procedure

1) Find C_C with R_c=0 for a 55^o phase margin

— Arbitrarily choose $C'_C \cong 5$ pF and set $R_C = 0$

— Using SPICE, find frequency ω_t where a –125° phase shift exists, define gain as A'

— Choose new C_C so ω_t becomes unity-gain frequency of the loop gain — results in a 55° phase margin.

— Achieved by setting $C_C = C'_C A'$

— Might need to iterate on C_C a couple of times using SPICE

Design Procedure

2) Choose R_C according to

$$R_C = \frac{1}{1.2\omega_t C_C} \tag{31}$$

— Increases ω_t by about 20 percent, leaving zero near final ω_t

— Check that gain continues to decrease at frequencies above the new ω_t

3) If phase margin not adequate, increase C_C while leaving R_C constant

Design Procedure

4) Replace R_C by a transistor

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff16}} \tag{32}$$

— SPICE can be used again to fine-tune the device dimensions to optimize phase margin

Process and Temperature Independence

- Can show non-dominant pole roughly given by

$$\omega_{p2} \cong \frac{g_{m7}}{C_1 + C_2} \tag{33}$$

- Recall zero given by

$$\omega_z = \frac{-1}{C_C(1/g_{m7} - R_C)} \tag{34}$$

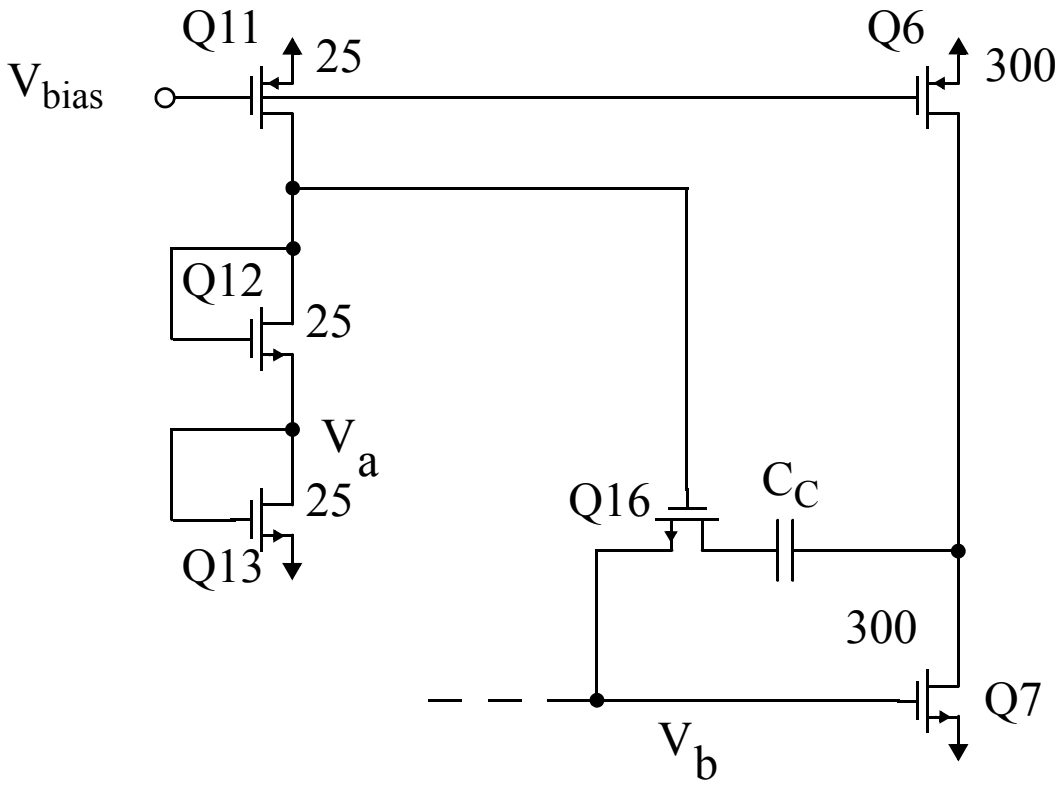
- If R_C tracks inverse of g_{m7} then zero will track ω_{p2}

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}(W/L)_{16} V_{eff16}} \tag{35}$$

$$g_{m7} = \mu_n C_{ox}(W/L)_7 V_{eff7} \tag{36}$$

Process and Temperature Independence

- Need to ensure V_{eff16}/V_{eff7} independent of process and temperature variations



- First set $V_{eff13} = V_{eff7}$ which makes $V_a = V_b$

Process and Temperature Independence

$$\sqrt{\frac{2I_{D7}}{\mu_n C_{ox}(W/L)_7}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} \tag{37}$$

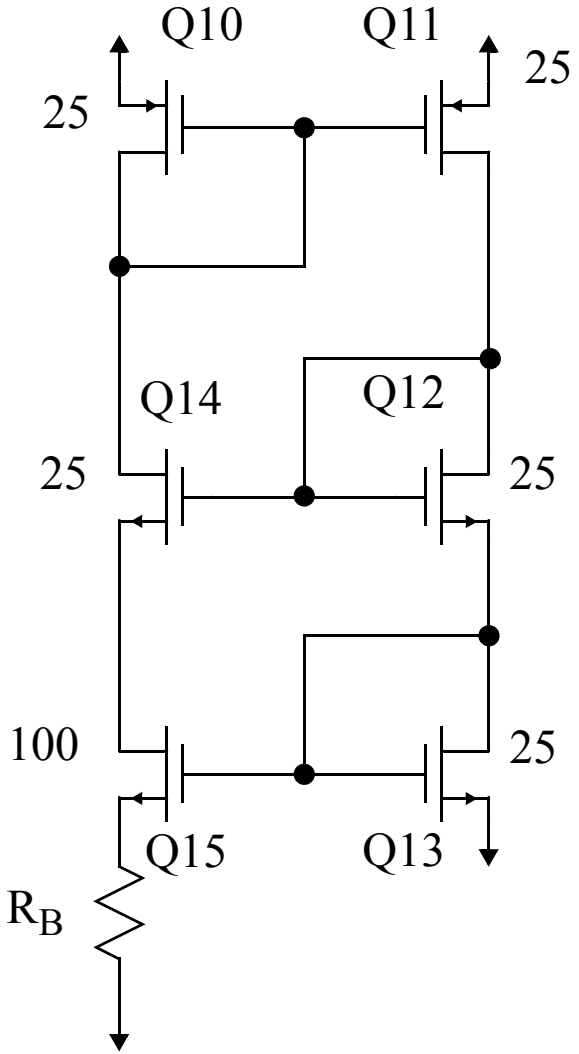
$$\frac{I_{D7}}{I_{D13}} = \frac{(W/L)_7}{(W/L)_{13}} \tag{38}$$

- Since $V_a = V_b$ and gates of Q12 and Q16 same

$$V_{\text{eff12}} = V_{\text{eff16}} \tag{39}$$

$$\frac{V_{eff7}}{V_{eff16}} = \frac{V_{eff13}}{V_{eff12}} = \frac{\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}}}{\sqrt{\frac{2I_{D12}}{\mu_n C_{ox}(W/L)_{12}}}} = \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} \tag{40}$$

Stable Transconductance Biasing



- Can bias on-chip g_m to a resistor

$$V_{GS13} = V_{GS15} + I_{D15}R_B \tag{41}$$

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D15}R_B \tag{42}$$

- But $I_{D13} = I_{D15}$ and rearrange

$$\frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}}\left[1 - \sqrt{\frac{W/L_{13}}{W/L_{15}}}\right] = R_B \tag{43}$$

- Recall $g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}$

$$g_{m13} = 2\left[1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right]/R_B \tag{44}$$

Stable Transconductance Biasing

- Transconductance of Q_{13} determined by geometric ratios only
- Independent of power-supply voltages, process parameters, temperature, etc.
- For special case $(W/L)_{15} = 4(W/L)_{13}$

$$g_{m13} = \frac{1}{R_B} \tag{45}$$

- Note that high-temp will decrease mobility and hence increase effective gate-source voltages
- Roughly 25% increase for 100 degree increase
- Requires a start-up circuit (might have all 0 currents)