Processing and Layout

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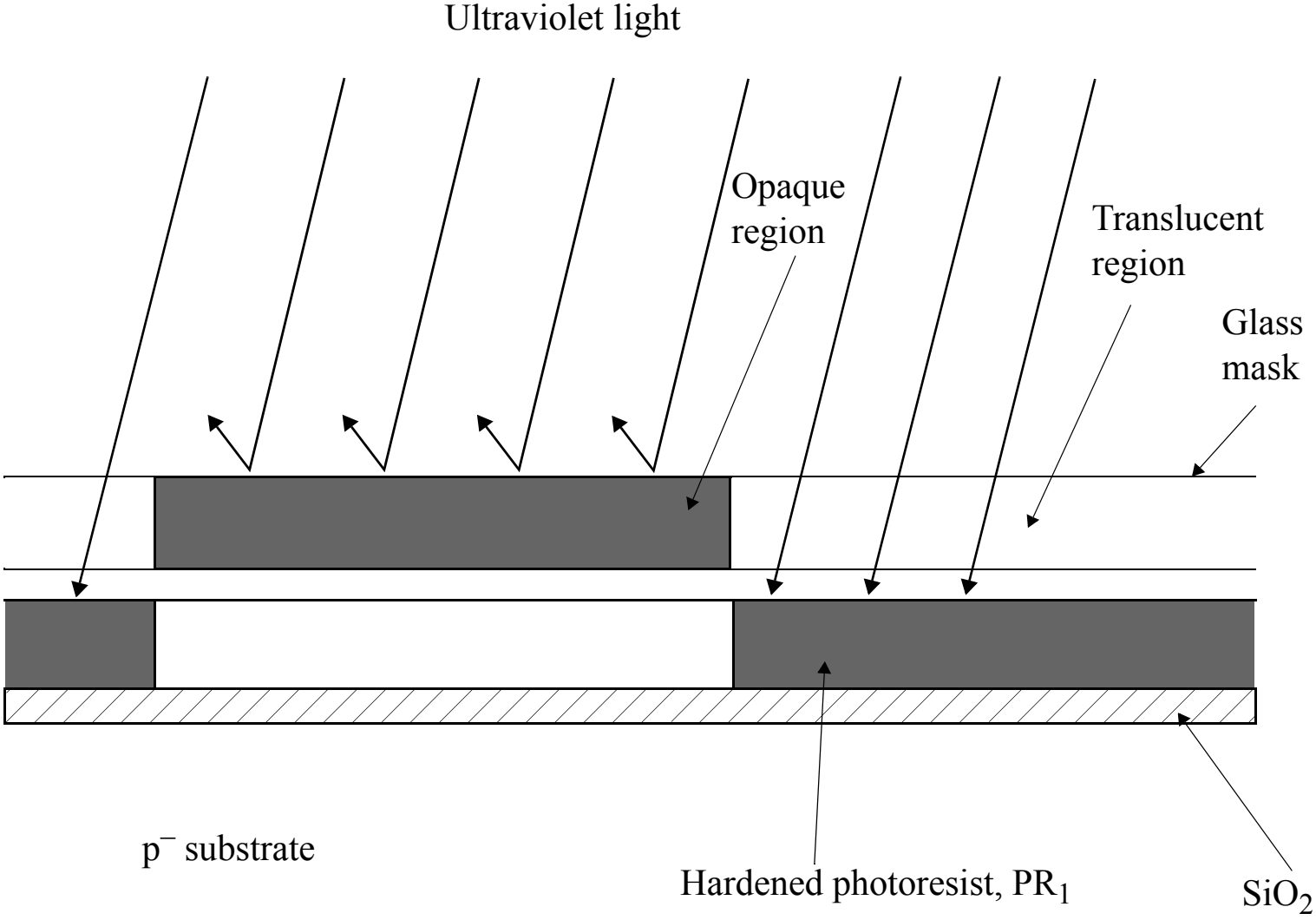
Silicon Wafer

- Create 8” diameter cylinder (1m long) of single-crystaline silicon with light doping (usually p-)
- Ingot cut into wafers about 1mm thick

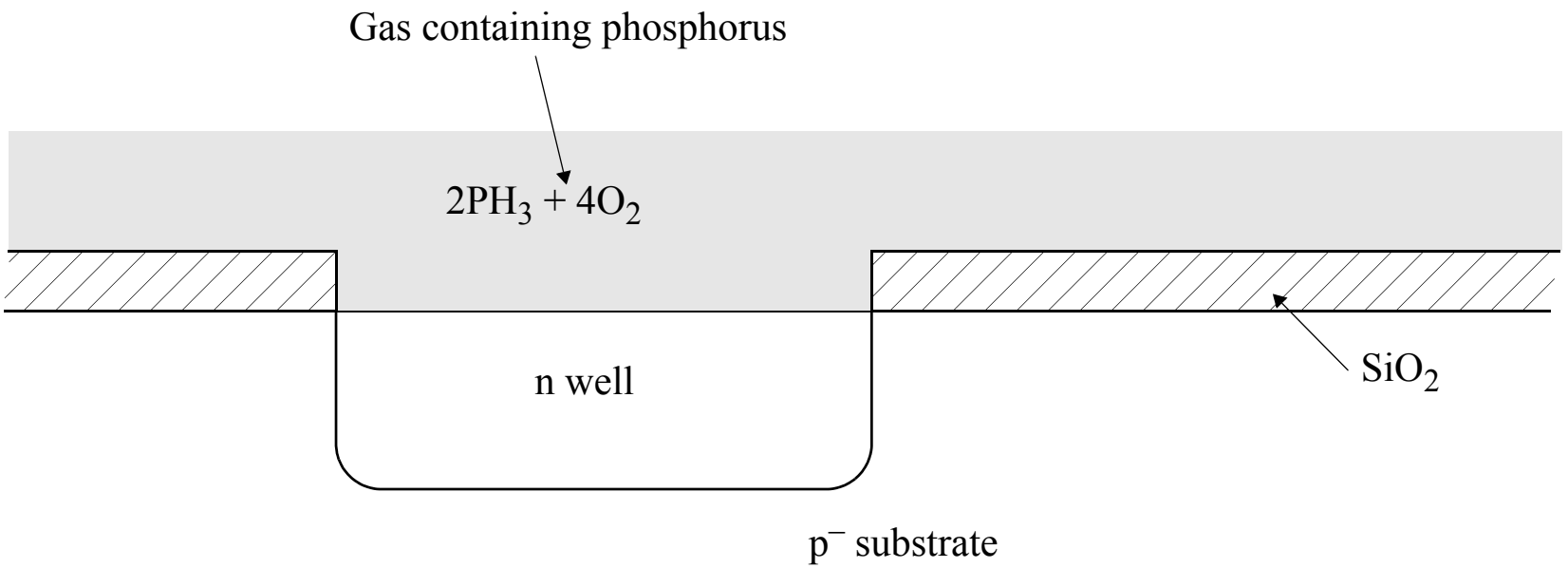
Photolithography

- Portions of silicon wafer are ***masked out*** so processing can be applied to remaining areas
- First create glass mask with dark areas using e-beam (cost of mask set often >$50k)
- Thermally grow SiO_2 on wafer, apply negative photoresist, align glass mask and expose to UV light
- Photoresist hardens (after baking) where exposed to light, remaining region removed (including SiO_2)
- Negative since SiO_2 removed where mask is light

Photolithography

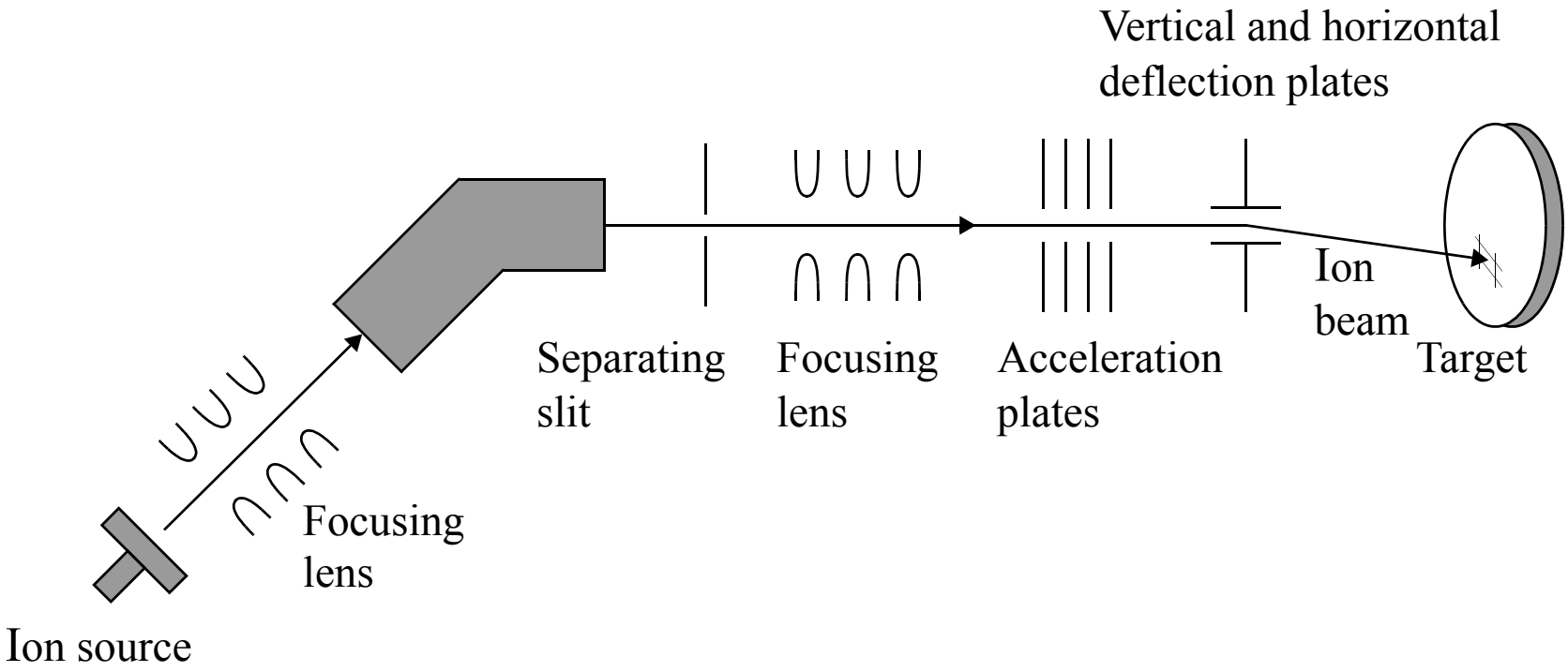


Diffusion



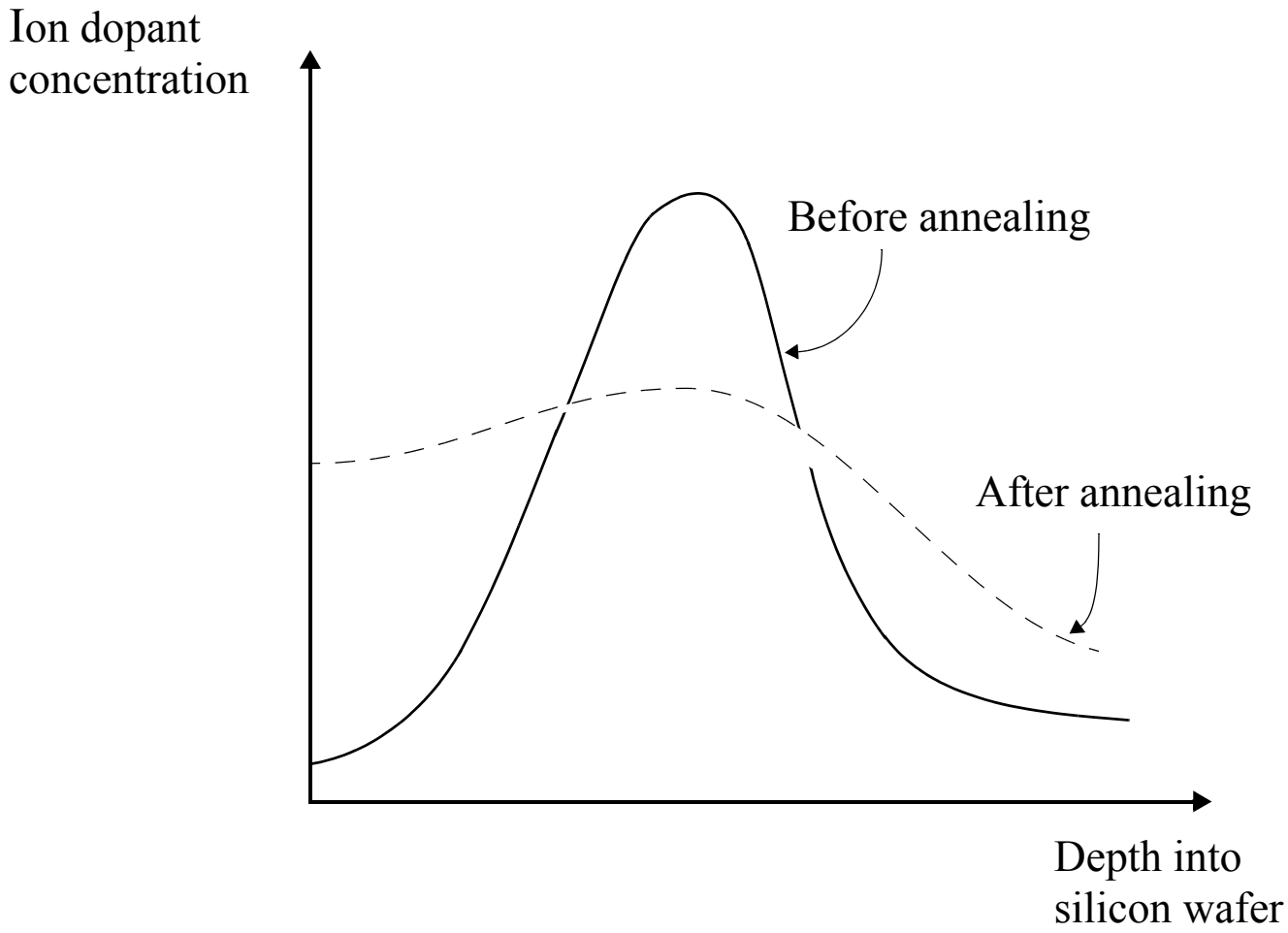
- Introduce dopants where well will be located
- Phosphorus gas used in furnace (1000 °C)

Ion Implantation



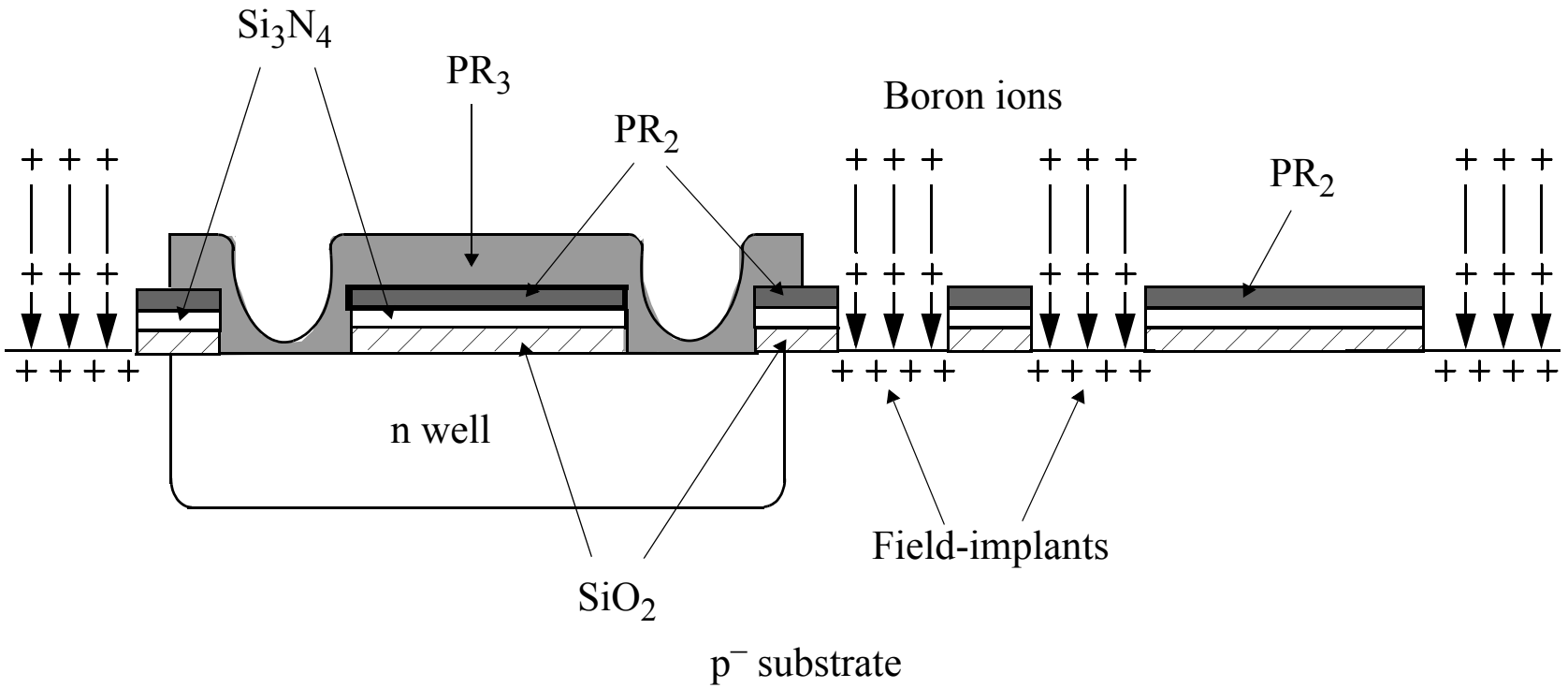
- More control as can set concentration and thickness
- Acceleration sets depth, current and time set dosage
- However, lattice damage and narrow doping profile — requires annealing

Annealing



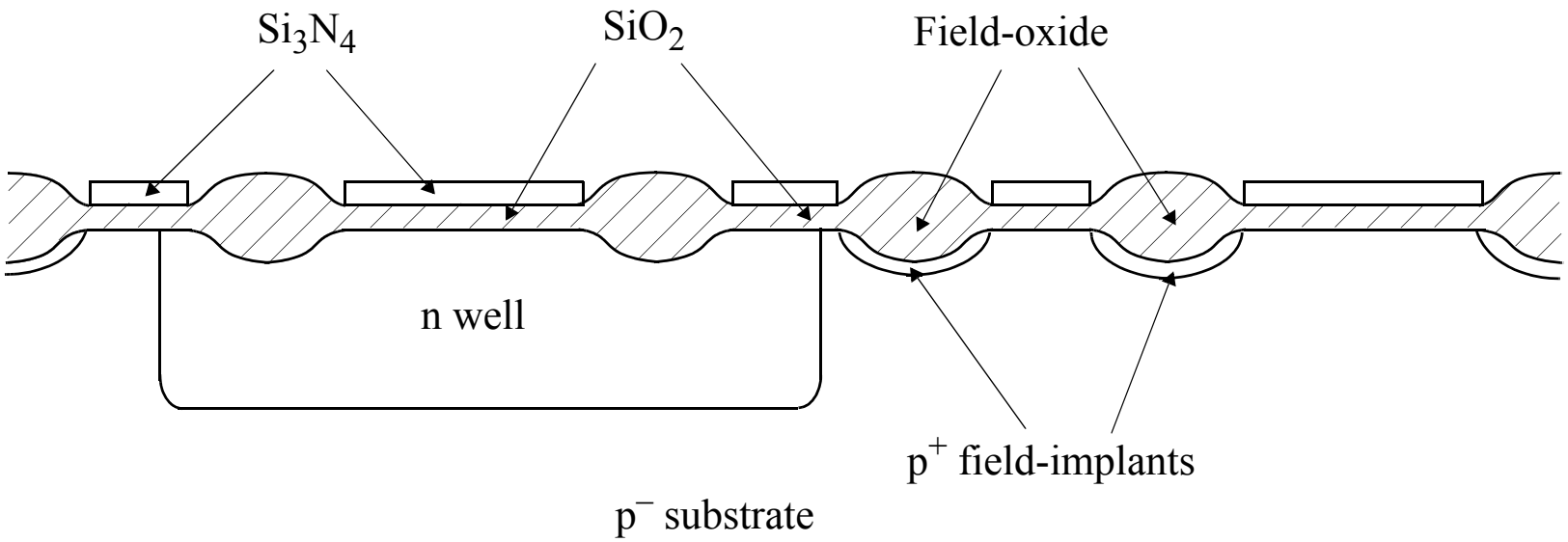
- Heat to 1000 °C then cool slowly

Field-implants



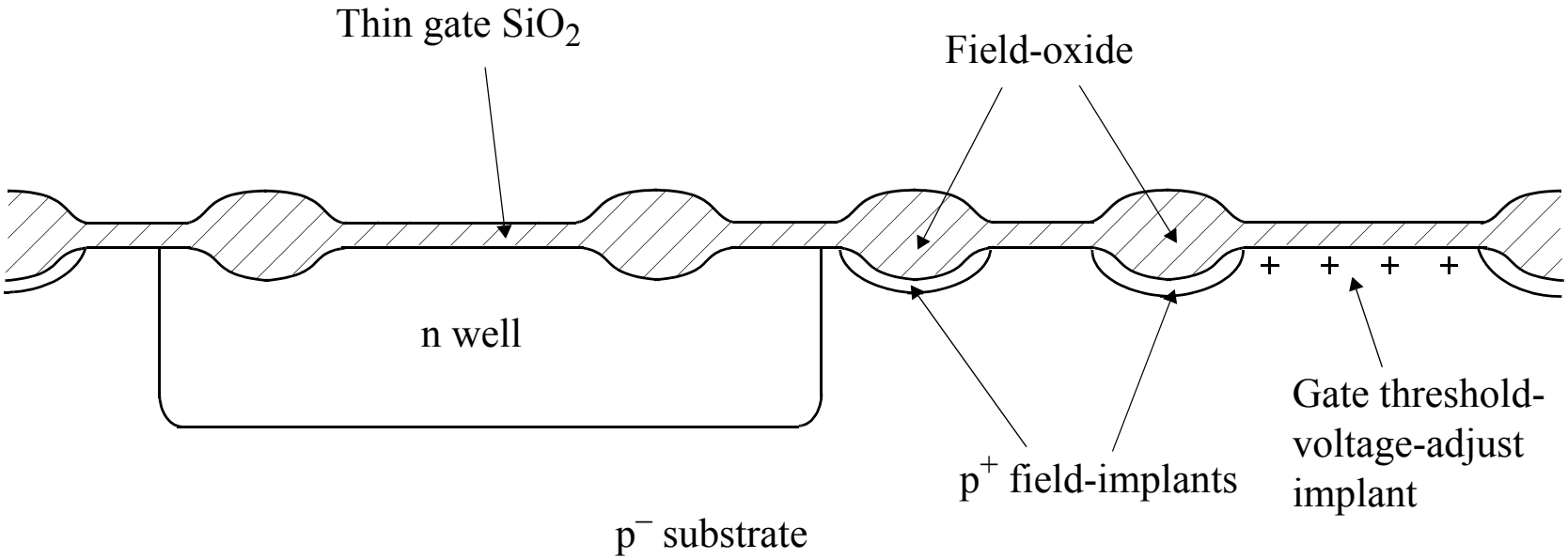
- Ensures silicon under field-oxide will not invert (will remain p-) although conductors above

Field-oxide



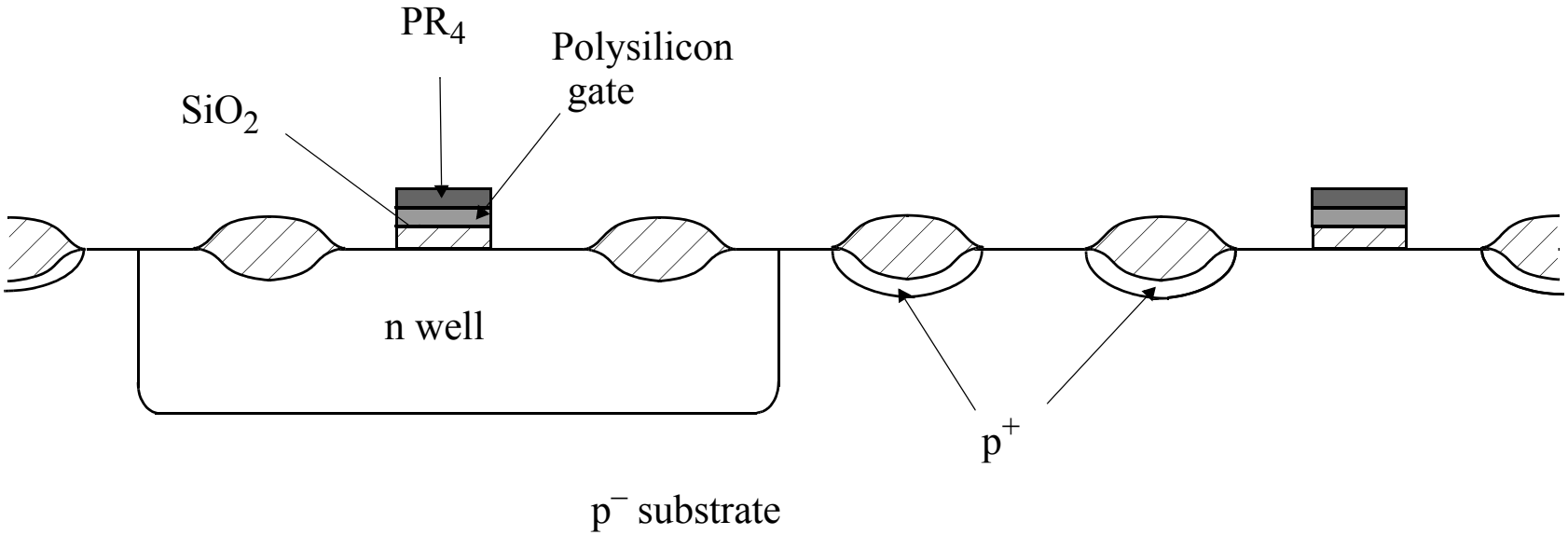
- Thick SiO_2 where no transistors
- Wet process (H_2O) — fast but more defects
- Dry process (O_2) — slower but denser and higher quality (high temp so called ***thermal oxide***)

Thin gate-oxide and threshold-adjust



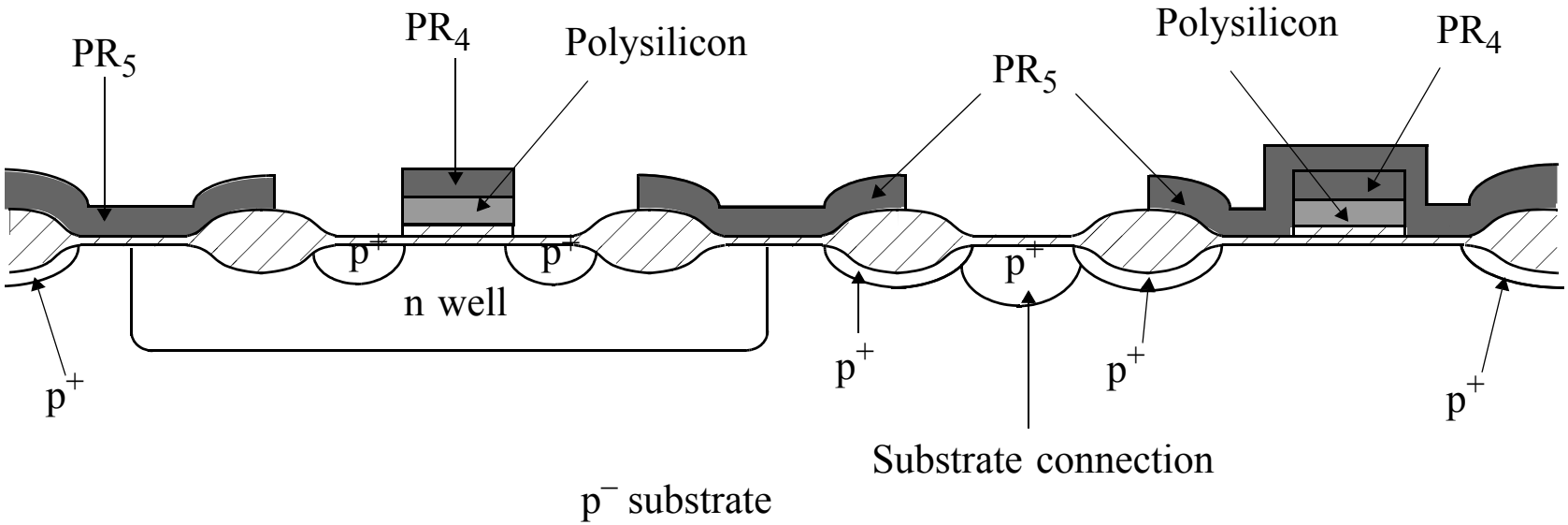
- Thin oxide grown using dry process (0.01 μm)
- If n-well more heavily doped then single boron implant will adjust
  V_{tn} from -0.1V to 0.8V and
  V_{tp} from -1.6V to -0.8V

Polysilicon Gates



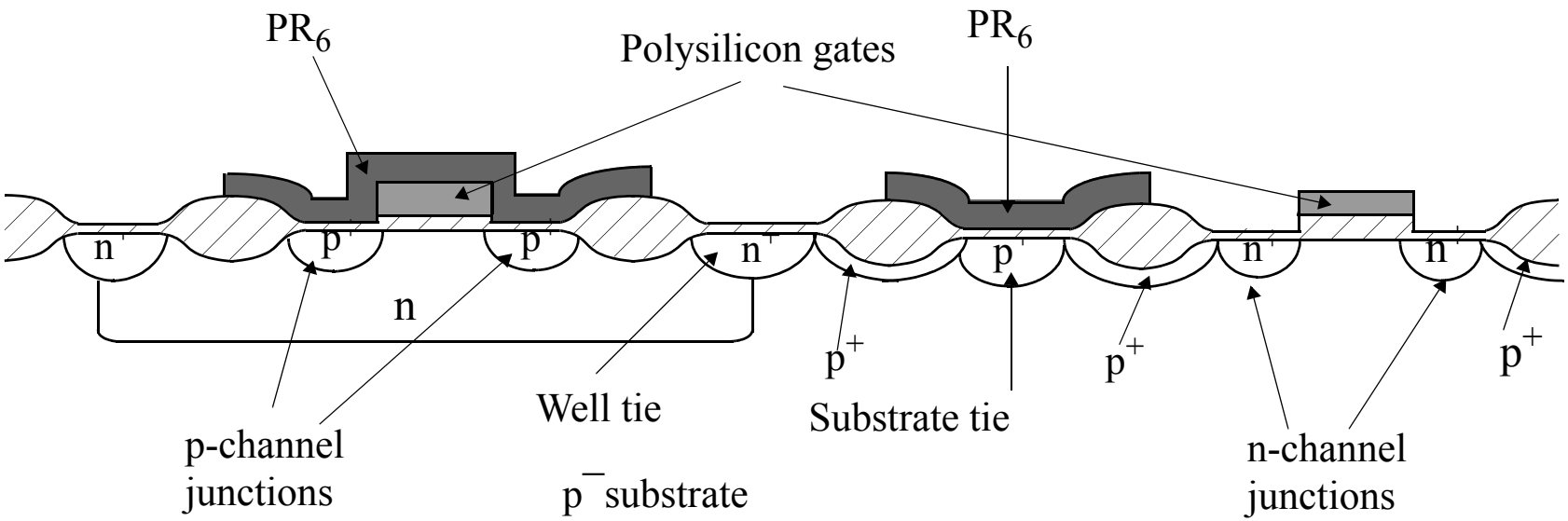
- Apply gate but only heat to 650 °C — polysilicon (rather than single crystal)
- 10 to 30 Ω/□ and thickness of 0.25 μm

P+ Junctions



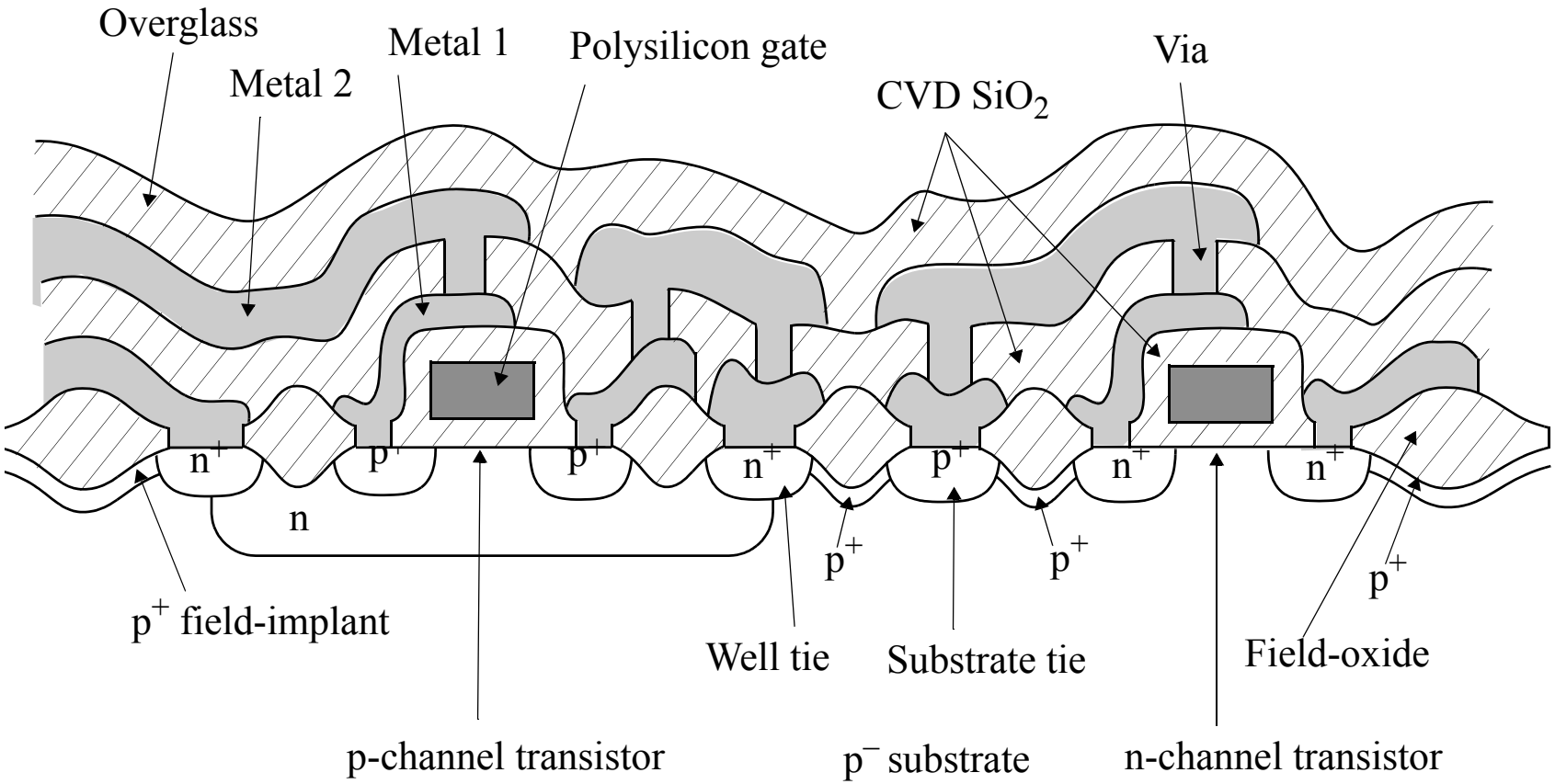
- Gates and drains formed for p-channel
- Use ion implantation
- Self-aligned as gate determines edges
- Substrate connection also shown

N+ Junctions

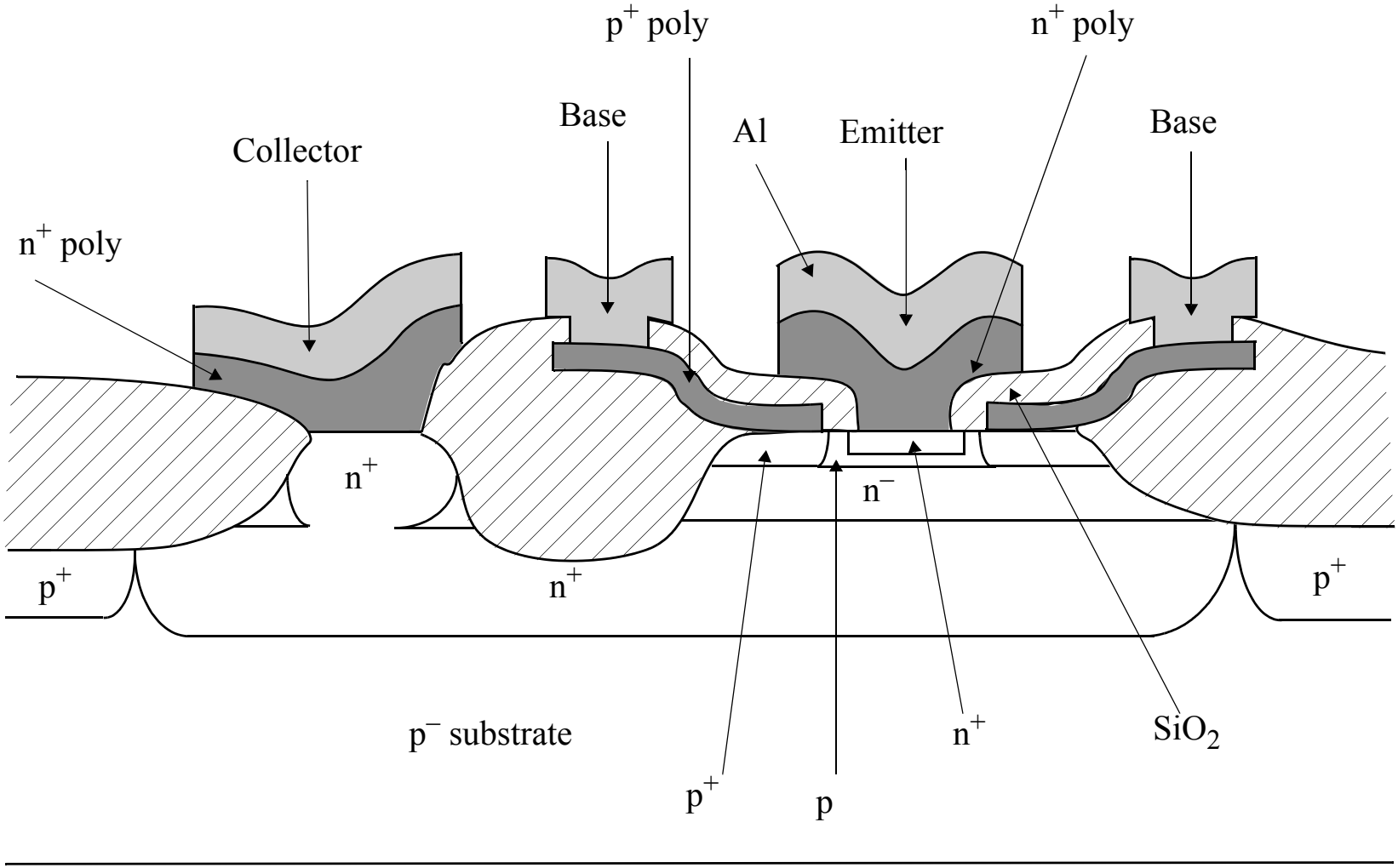


- p+ regions protected and n+ implanted
- Requires annealing after since ion implantation used
- Would melt gate if it were metal

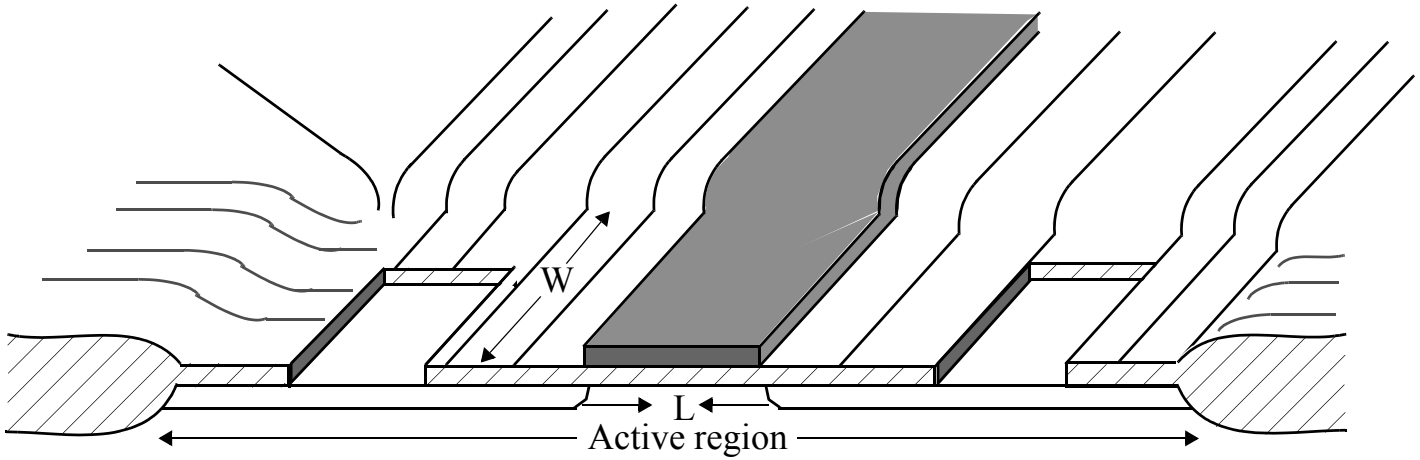
Final Cross Section

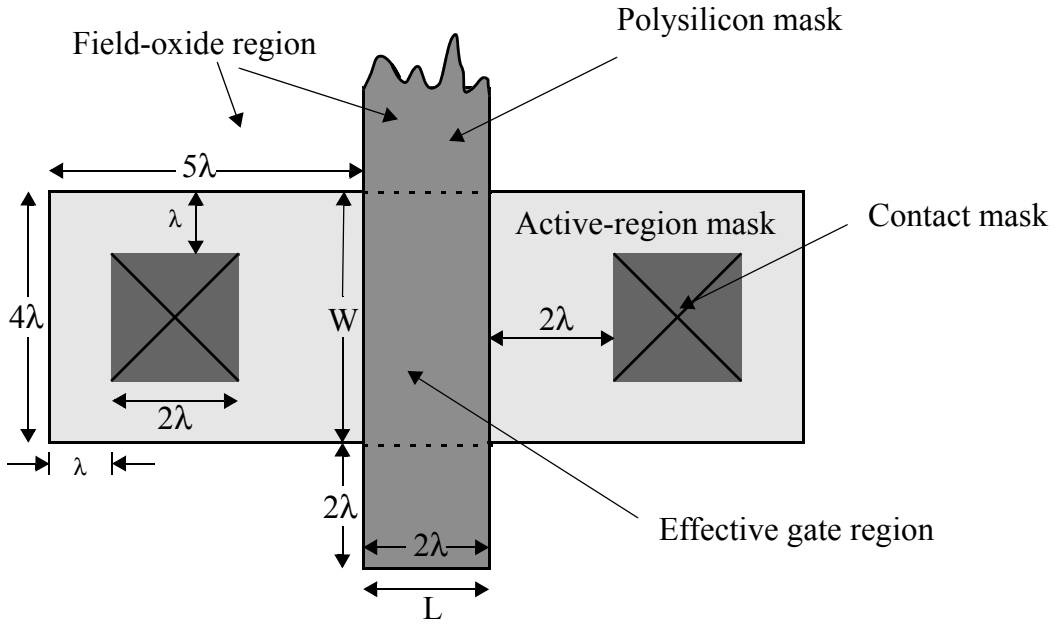


Bipolar Cross Section

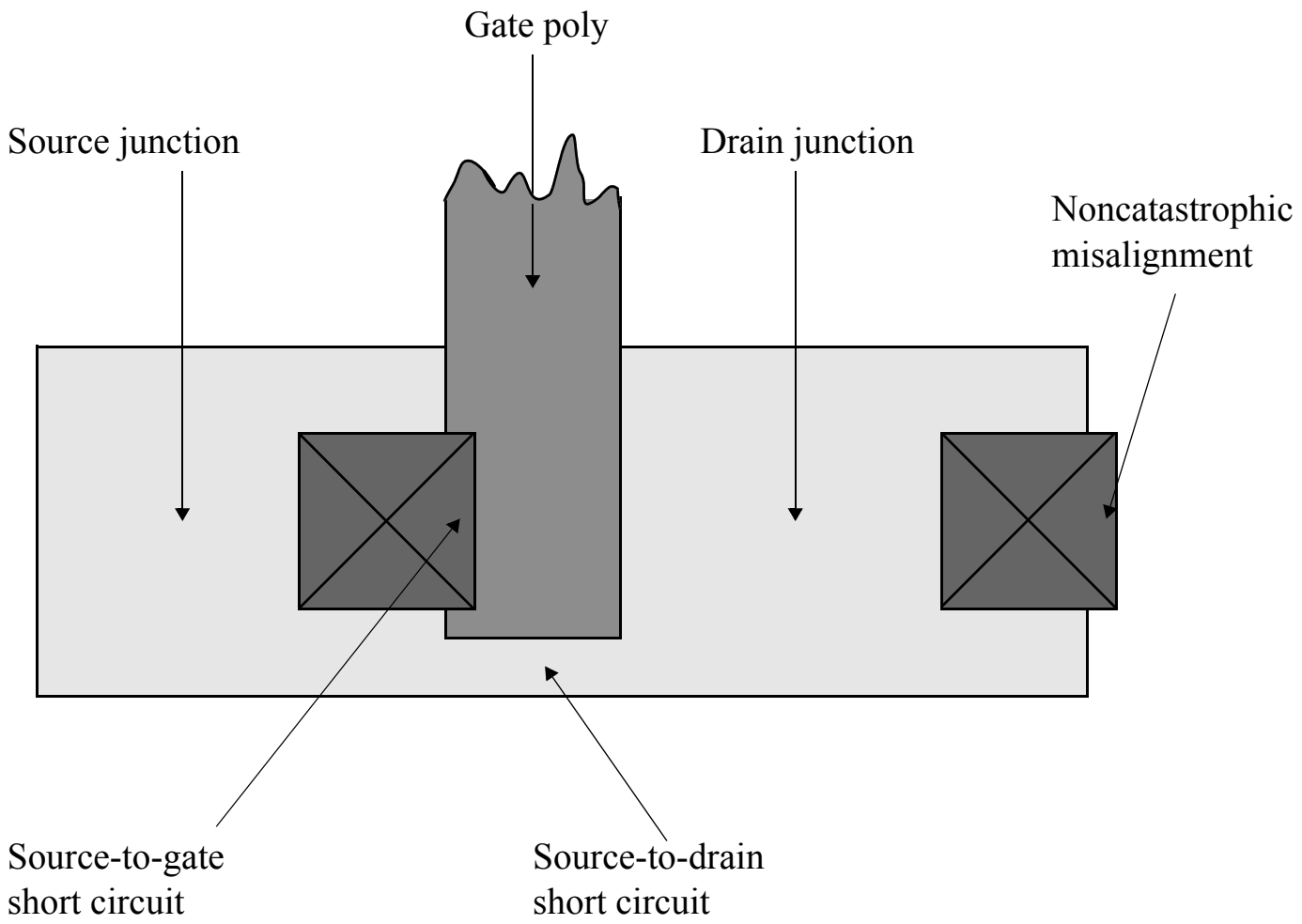


Transistor Layout

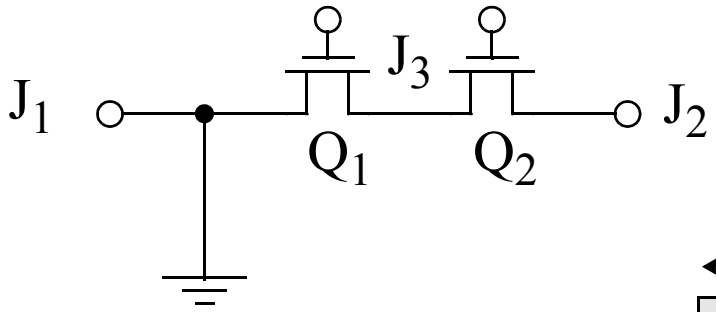




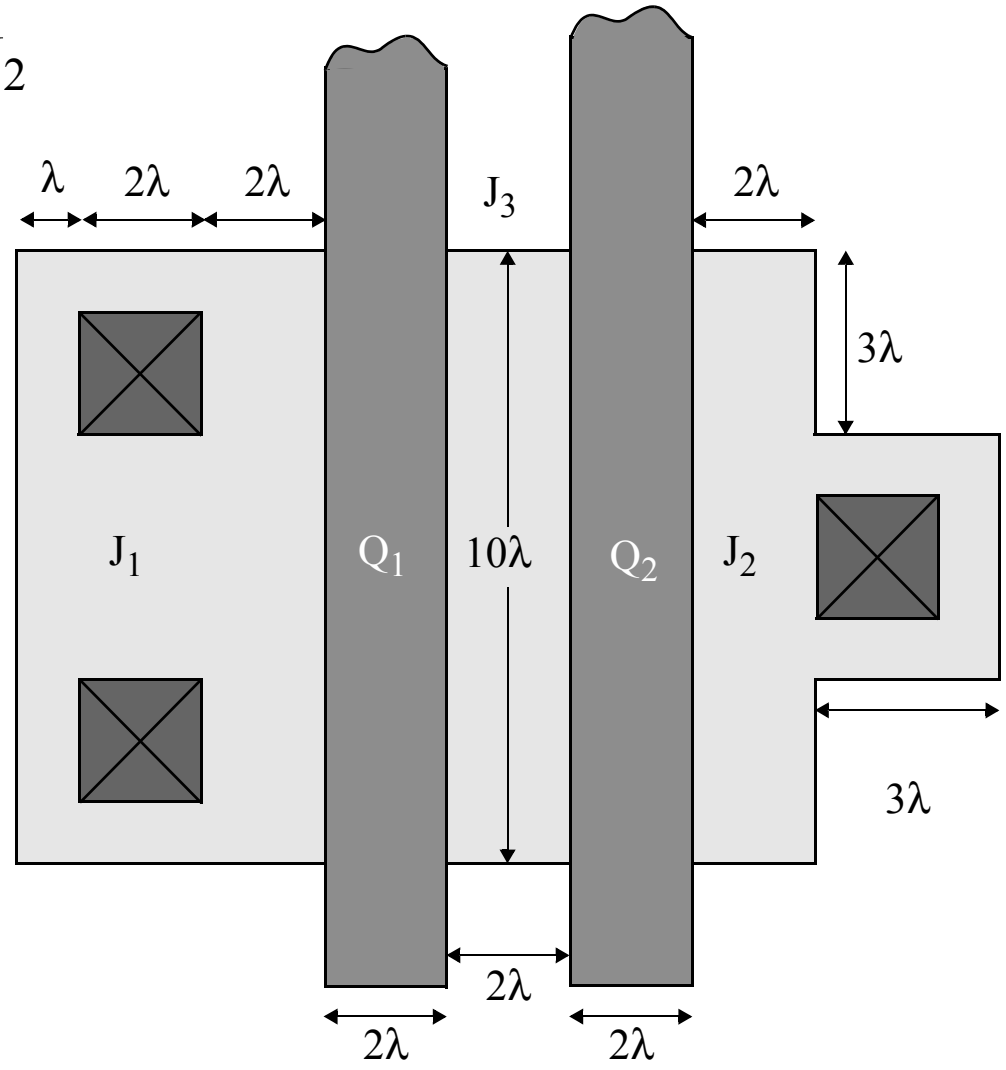
Mask misalignment



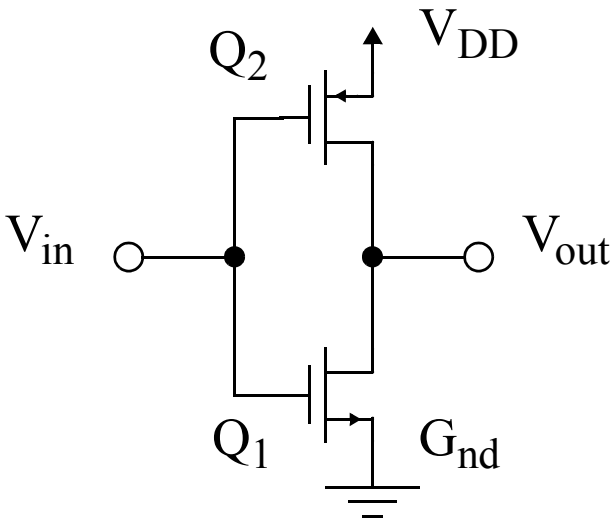
Series Transistor Layout

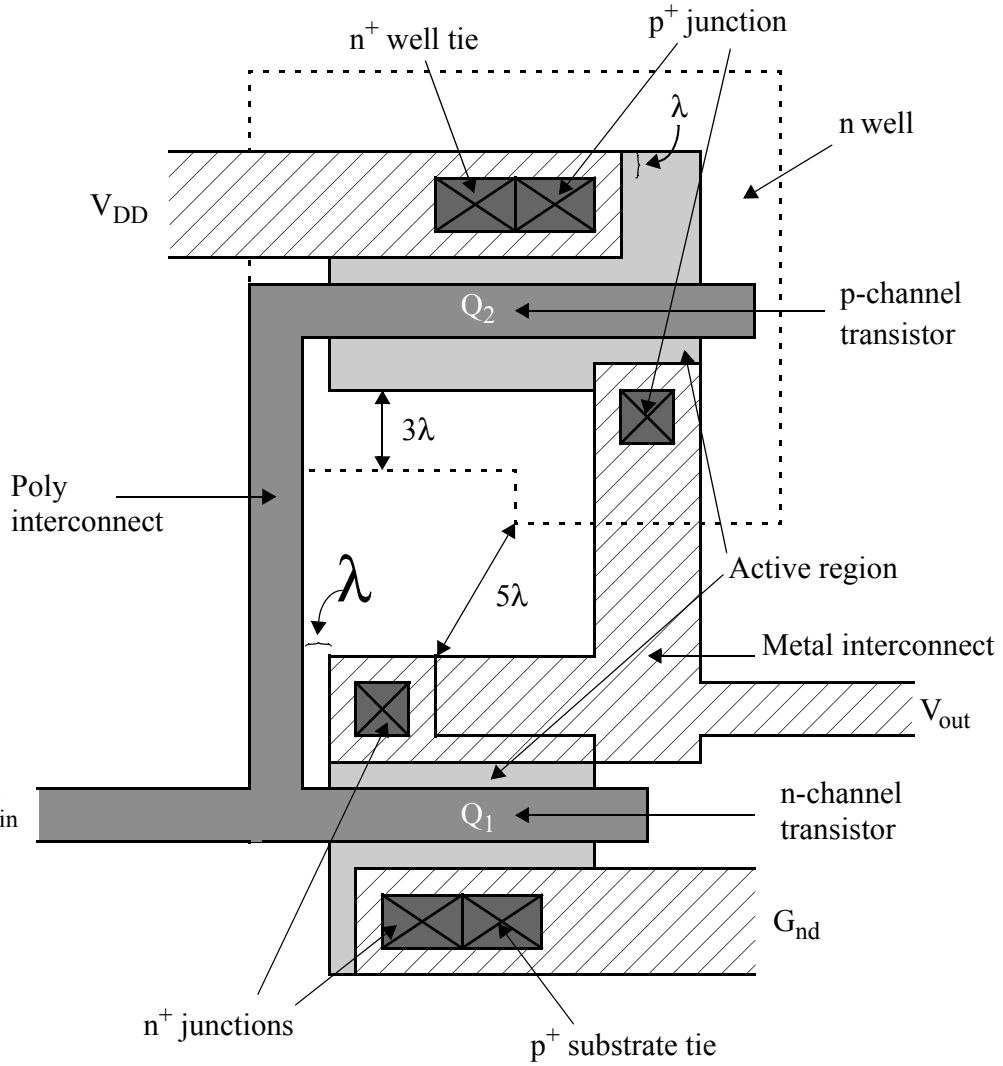


Less capacitance at node J_3 since less area AND not beside field implants

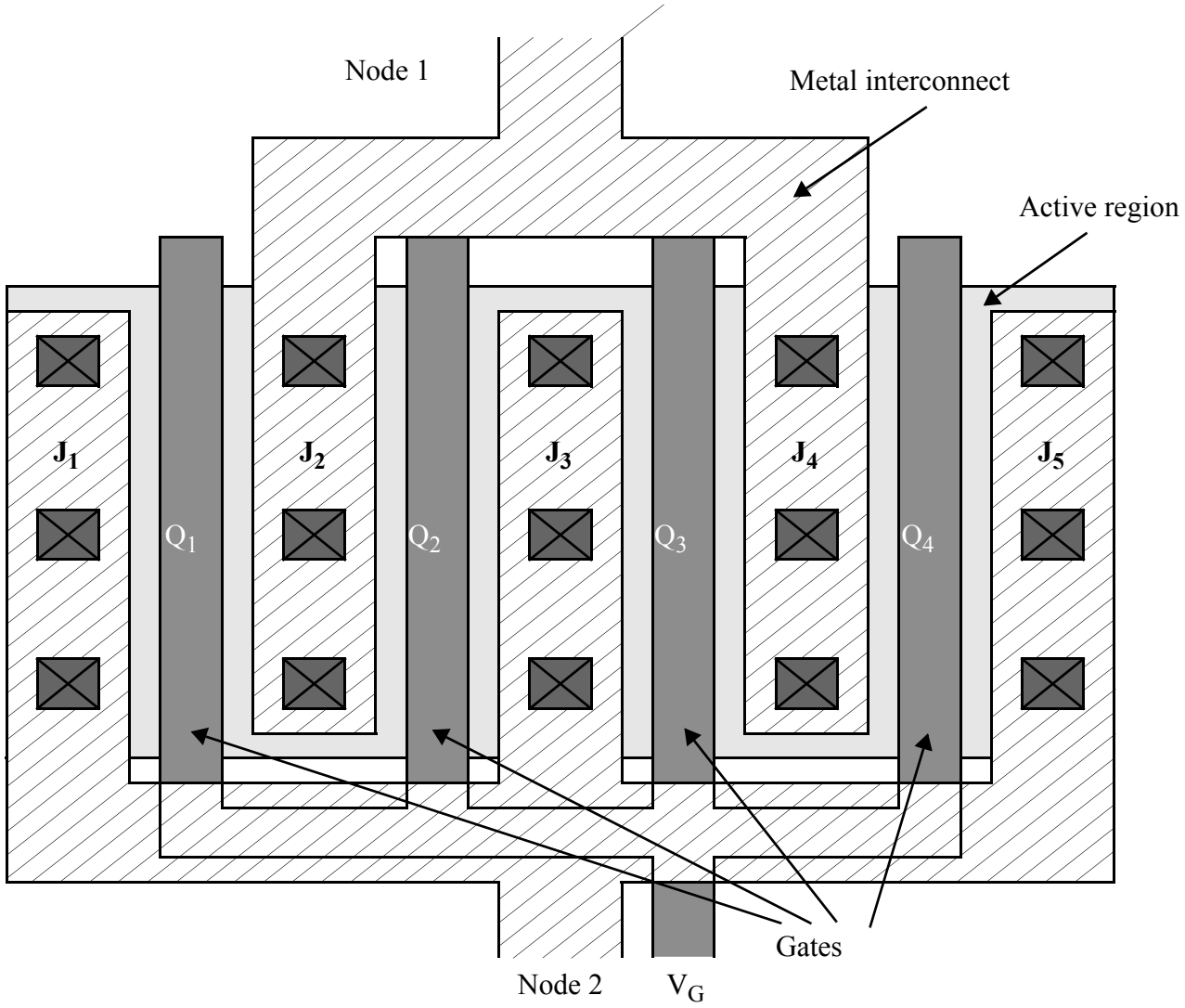


CMOS Inverter

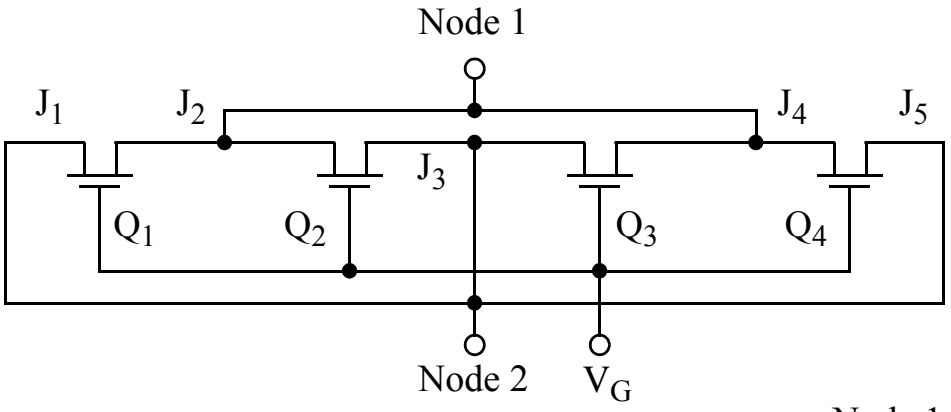


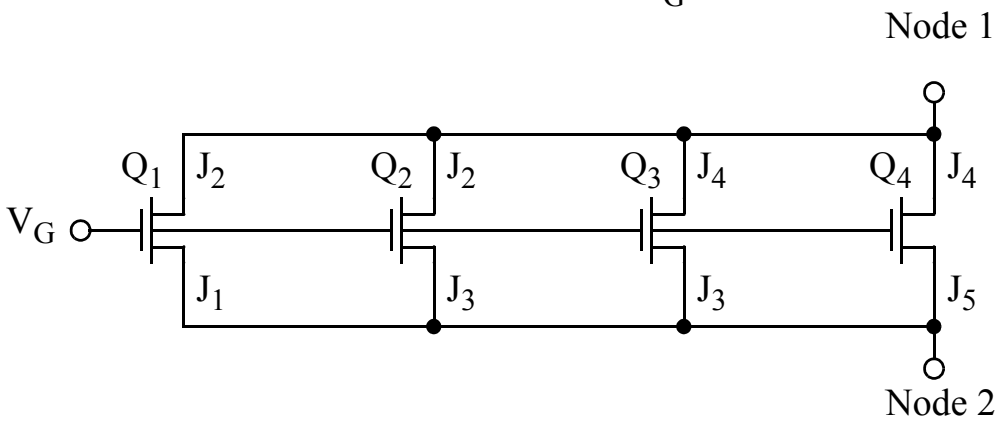


Single Large Transistor (4 in parallel)

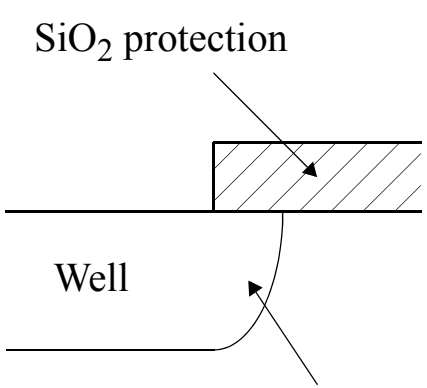


Schematic of Large Transistor

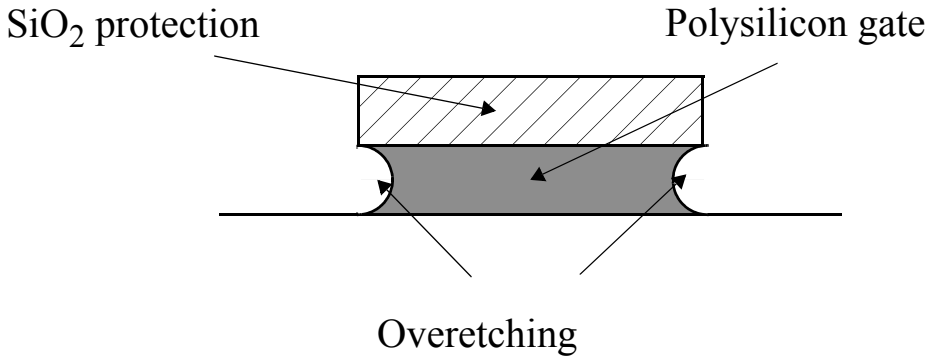


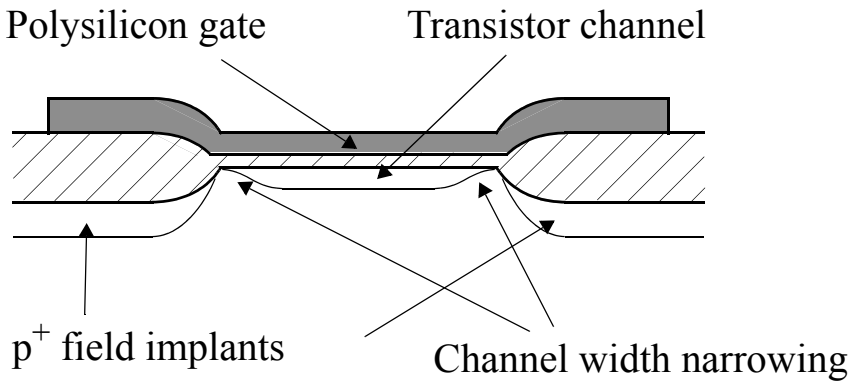


Actual sizes different from Masks

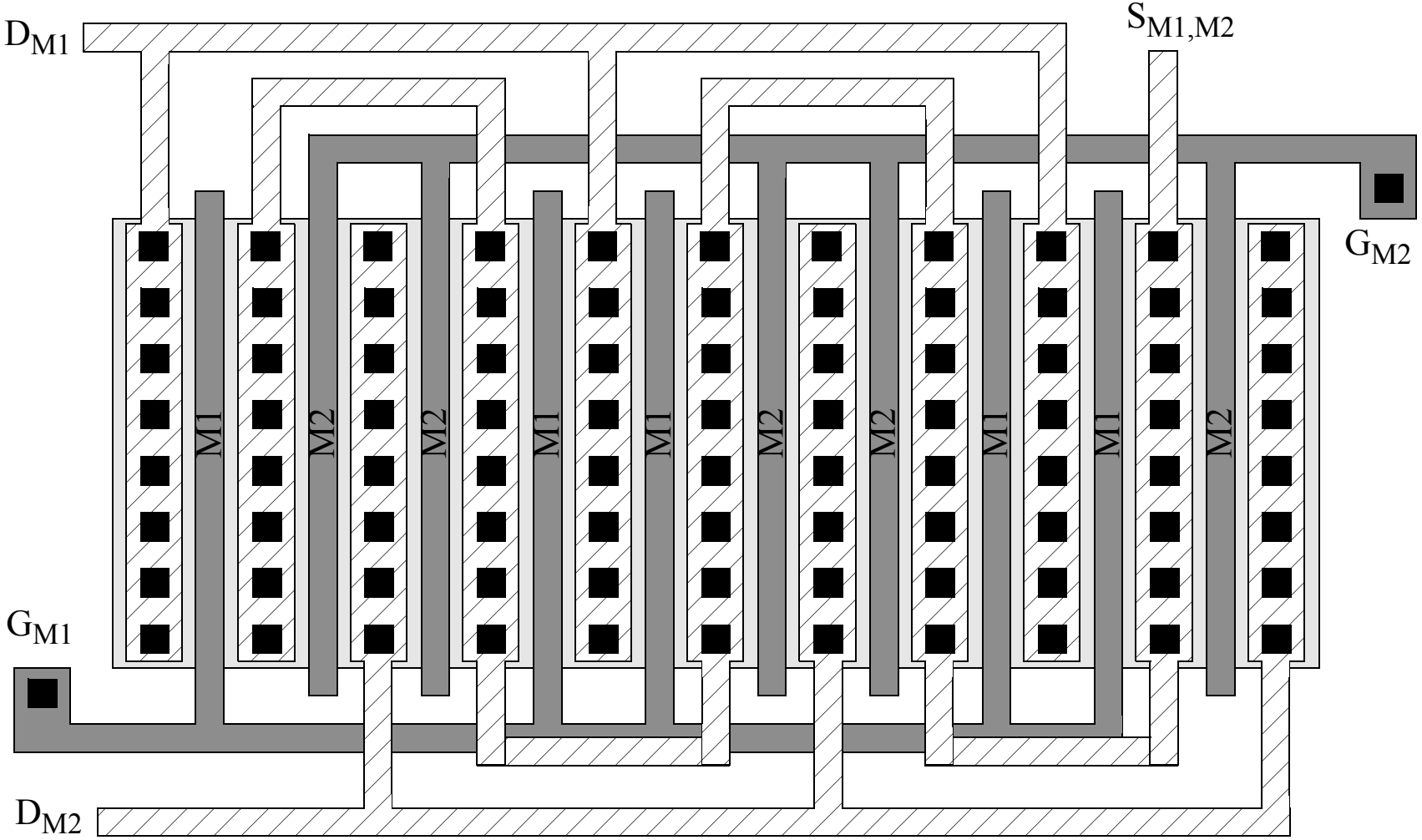


Lateral diffusion under SiO_2 mask

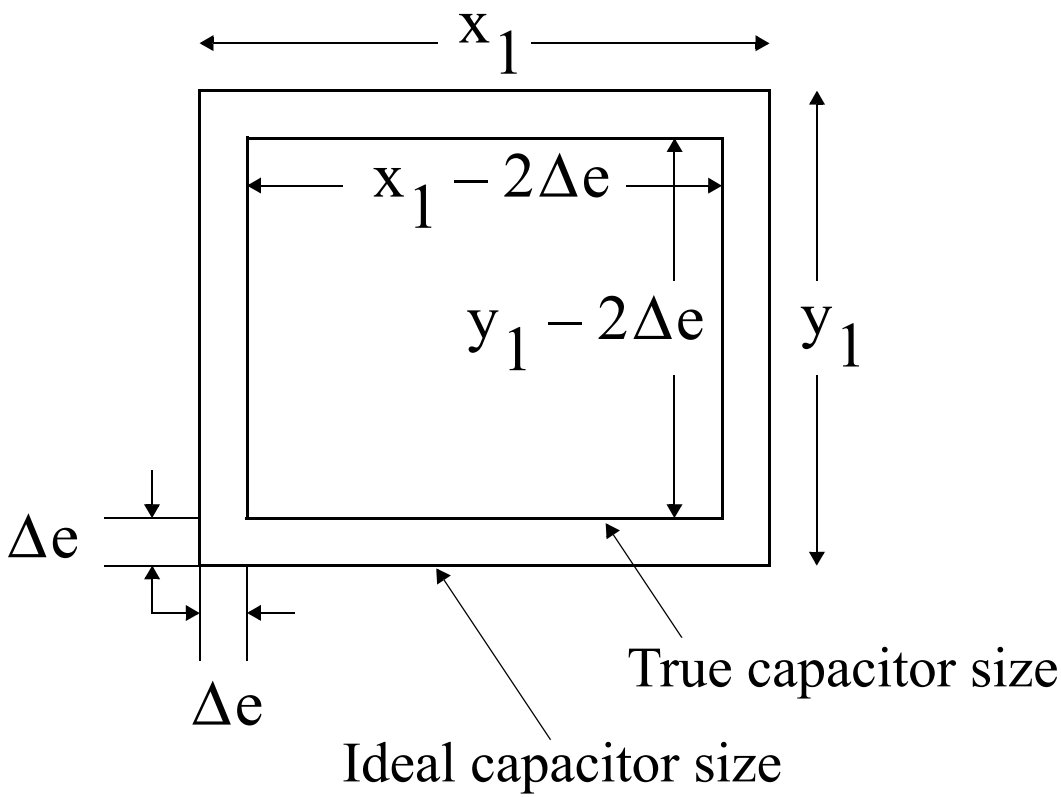




Common Centroid Layout for Diff Pair

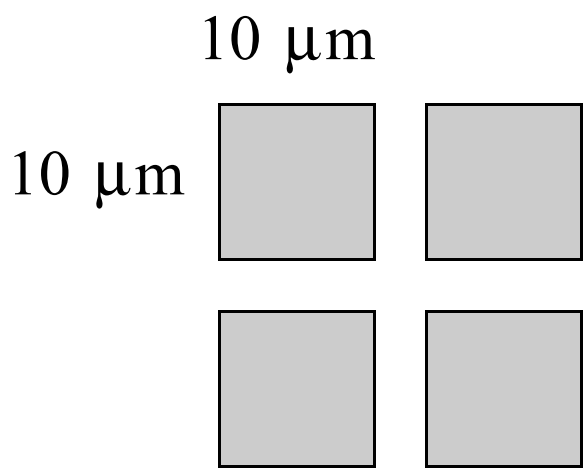


Capacitor Errors due to Overetching

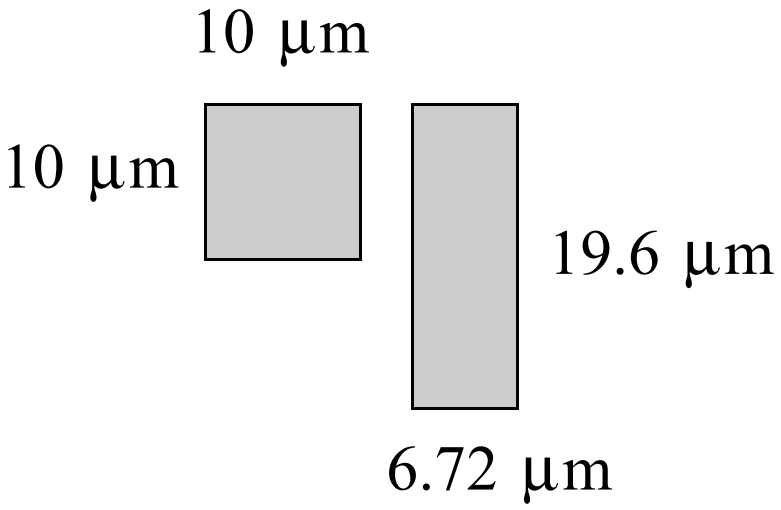


- Use unit sized capacitors as much as possible
- If not unit sized, keep the same perimeter-to-area ratio to minimize errors

Capacitor Layout



4 units



2.314 units

- Want to maintain ratio of 4 to 2.314
- Rectangular capacitor of size 1.314 units used
  — has same perimeter-to-area ratio as square
  — also has same number of corners

Capacitor Layout Equation

- Assume K is non-unit sized and between 1 and 2 — otherwise use another unit sized capacitor

$$K \equiv \frac{C_2}{C_1} = \frac{A_2}{A_1} = \frac{x_2 y_2}{x_1^2} \tag{1}$$

- Can show that

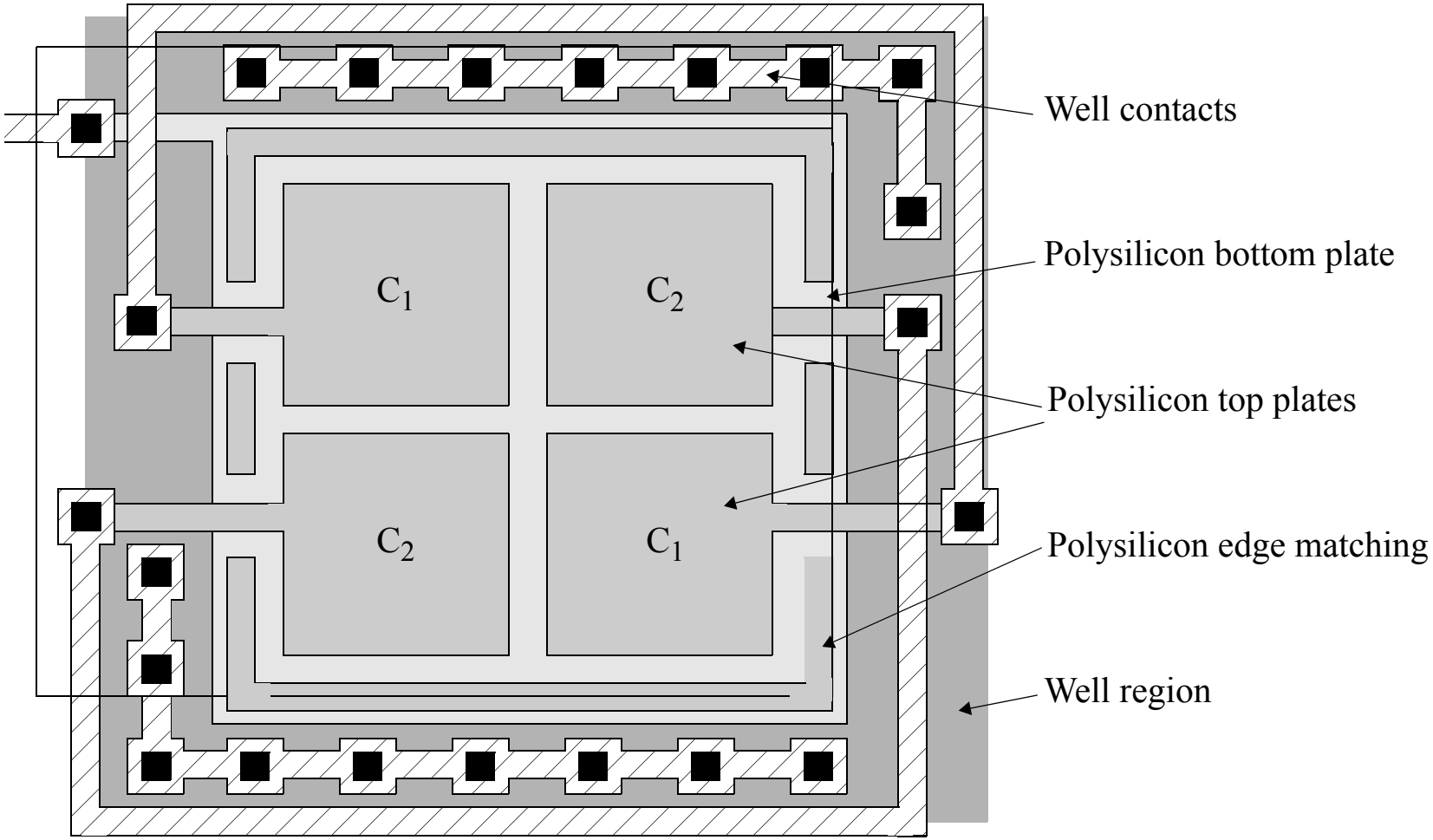
$$y_2 = x_1(K \pm \sqrt{K^2 - K}) \tag{2}$$

(+/- simply changes orientation of rectangle and sqrt is positive since K>1)

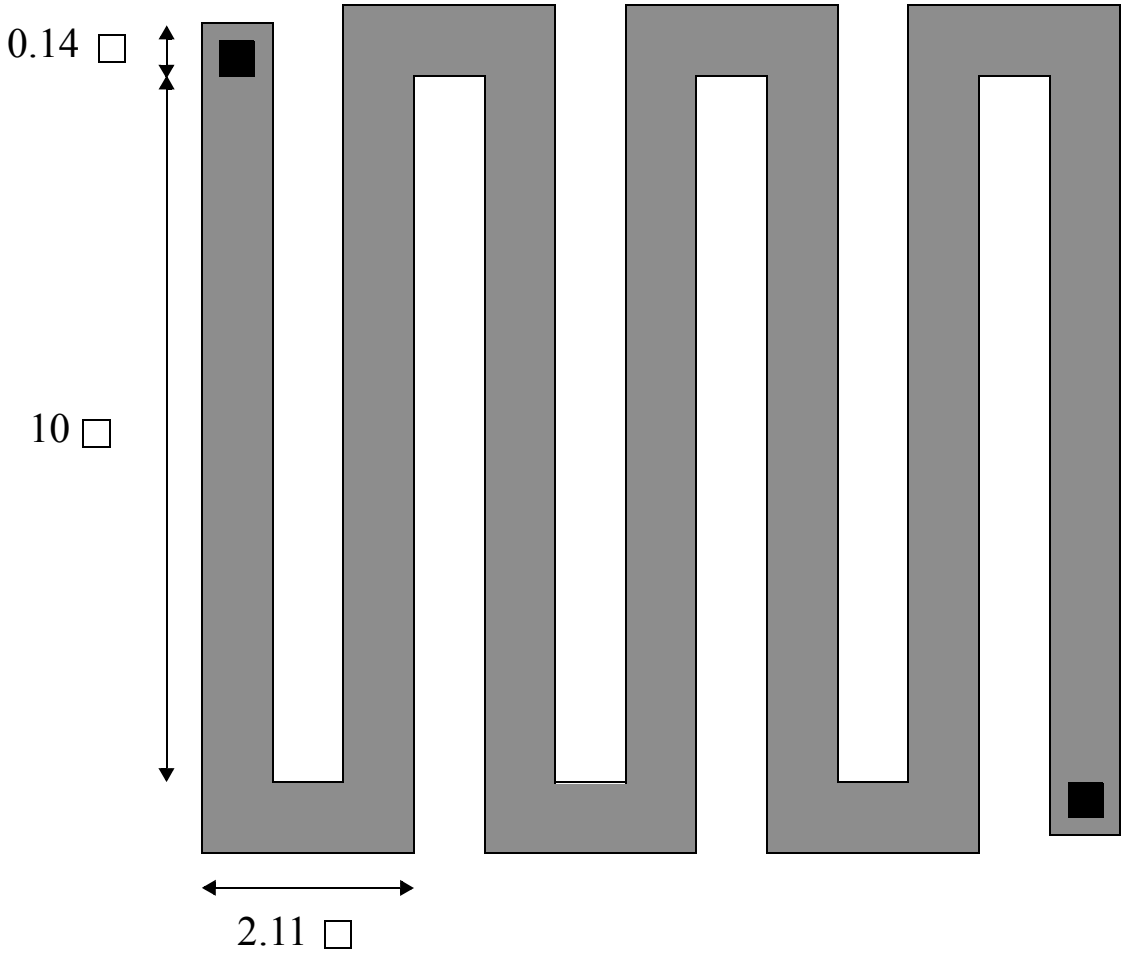
- Also

$$x_2 = \frac{K x_1^2}{y_2} \tag{3}$$

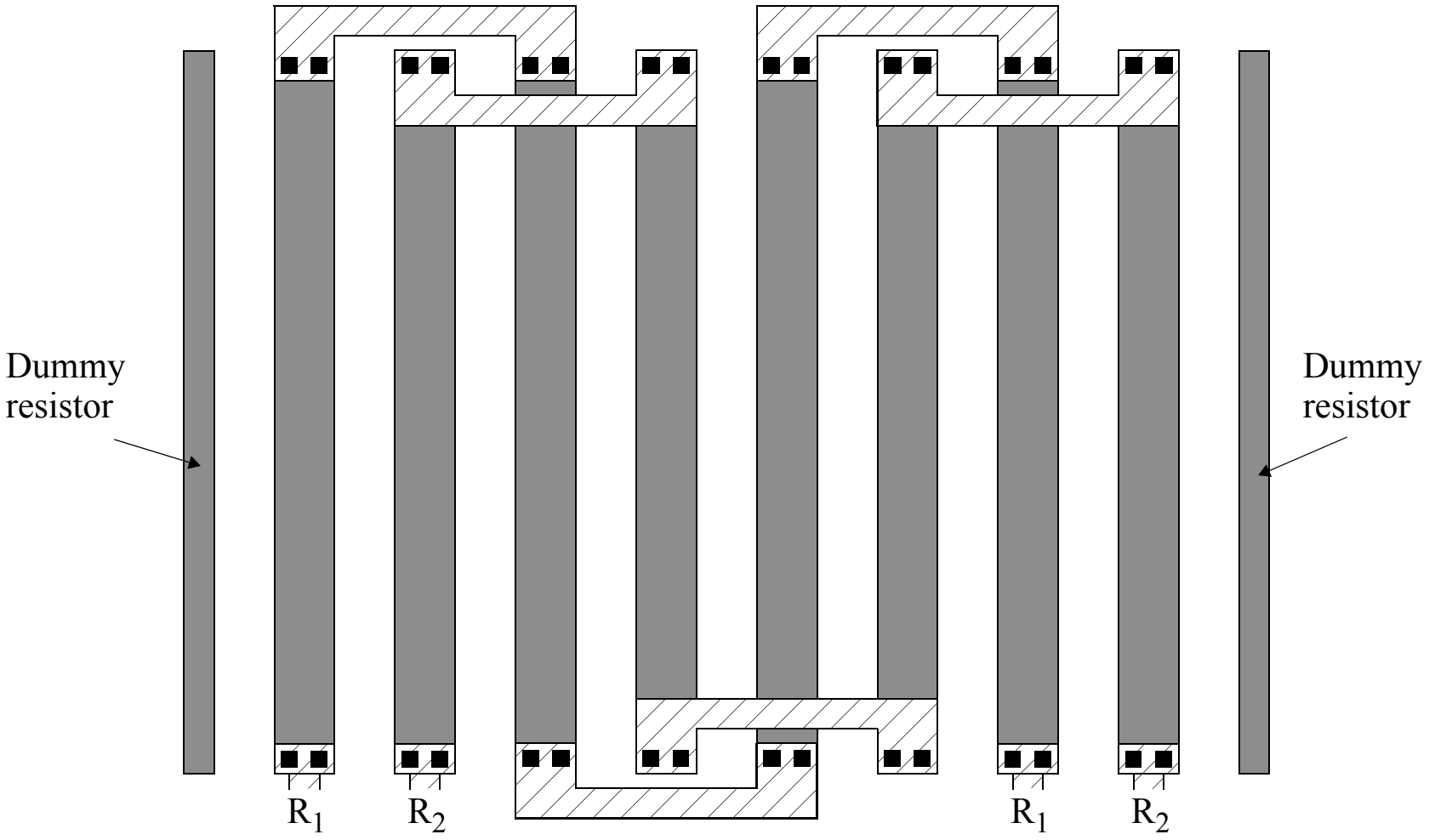
Example Capacitor Layout



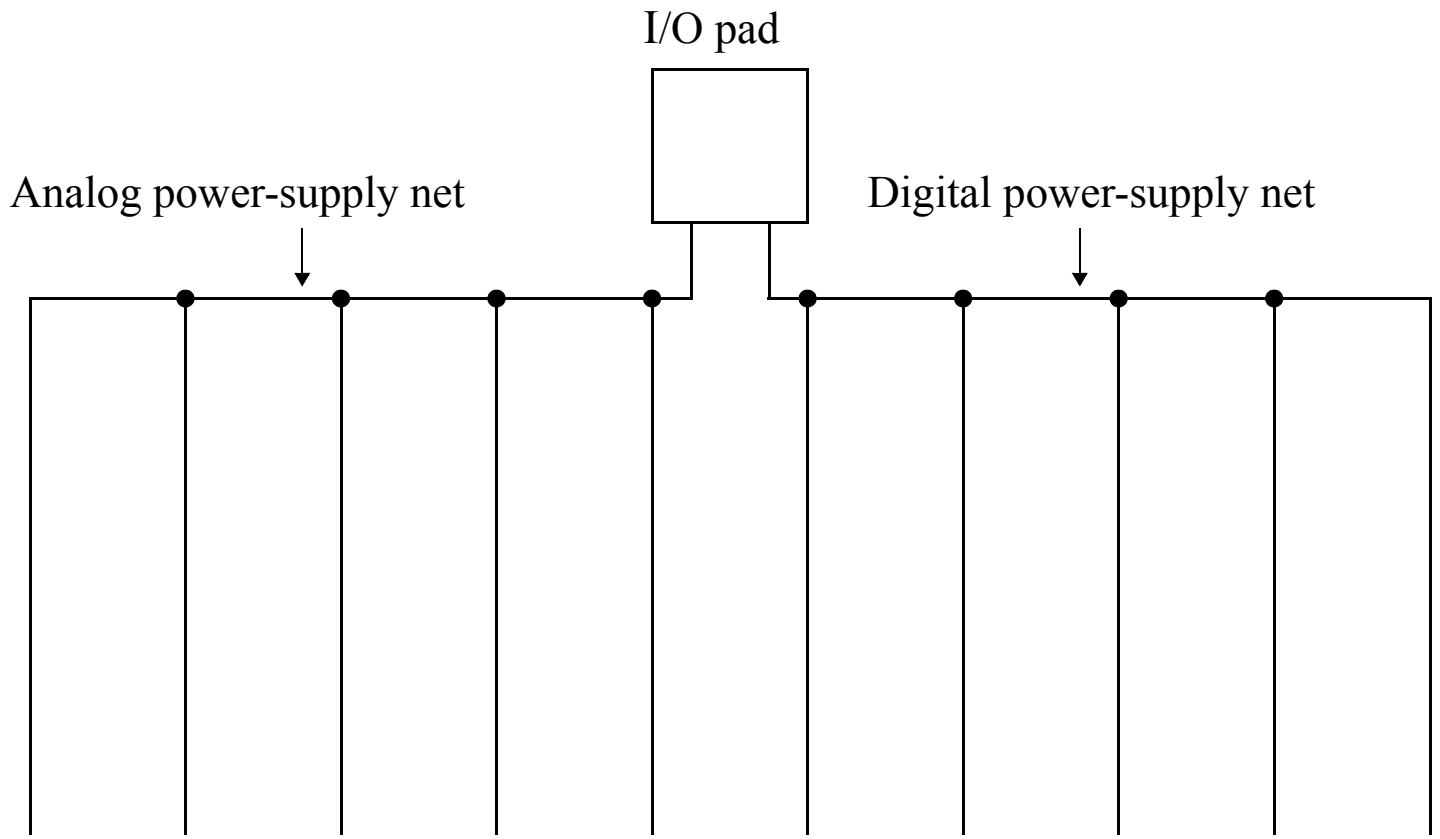
Typical Resistor Layout



More Accurate Resistor Layout

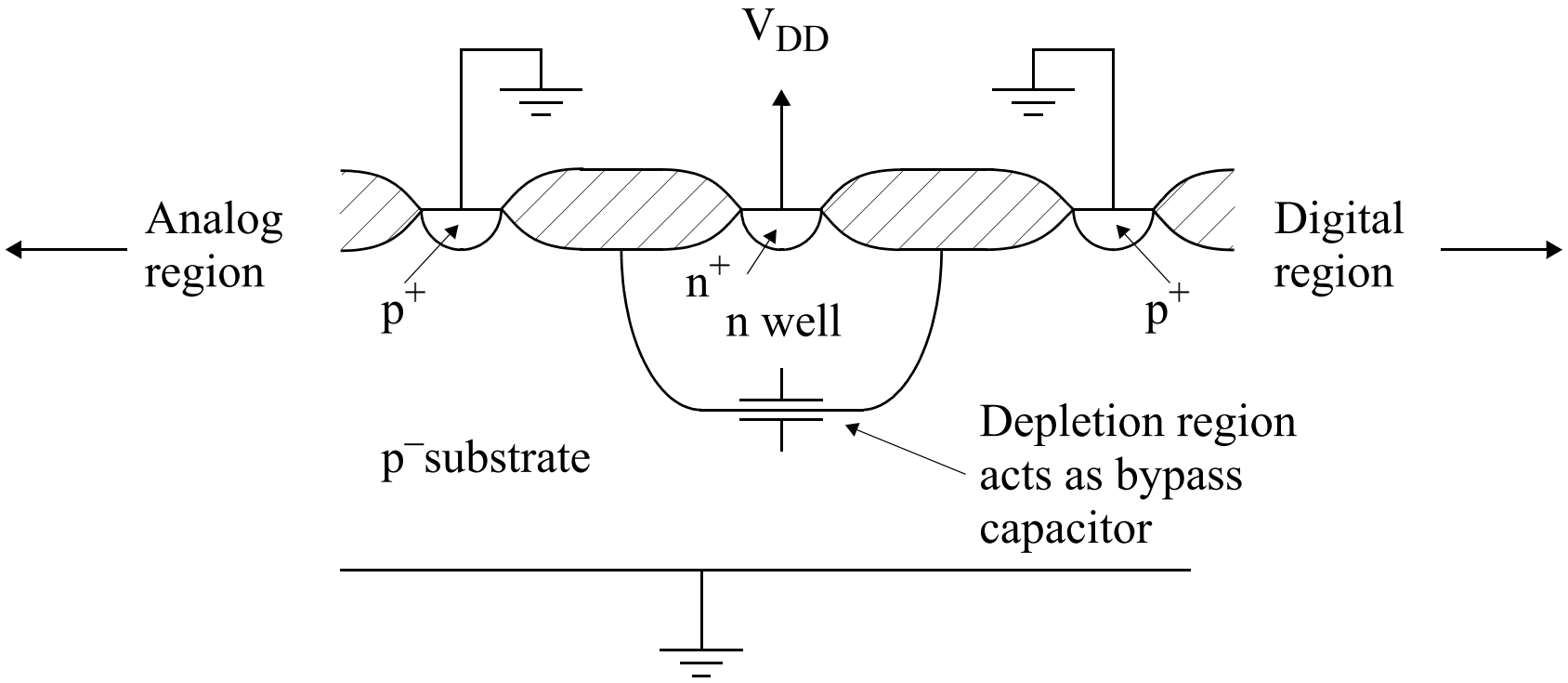


Separate Analog and Digital Power Supplies



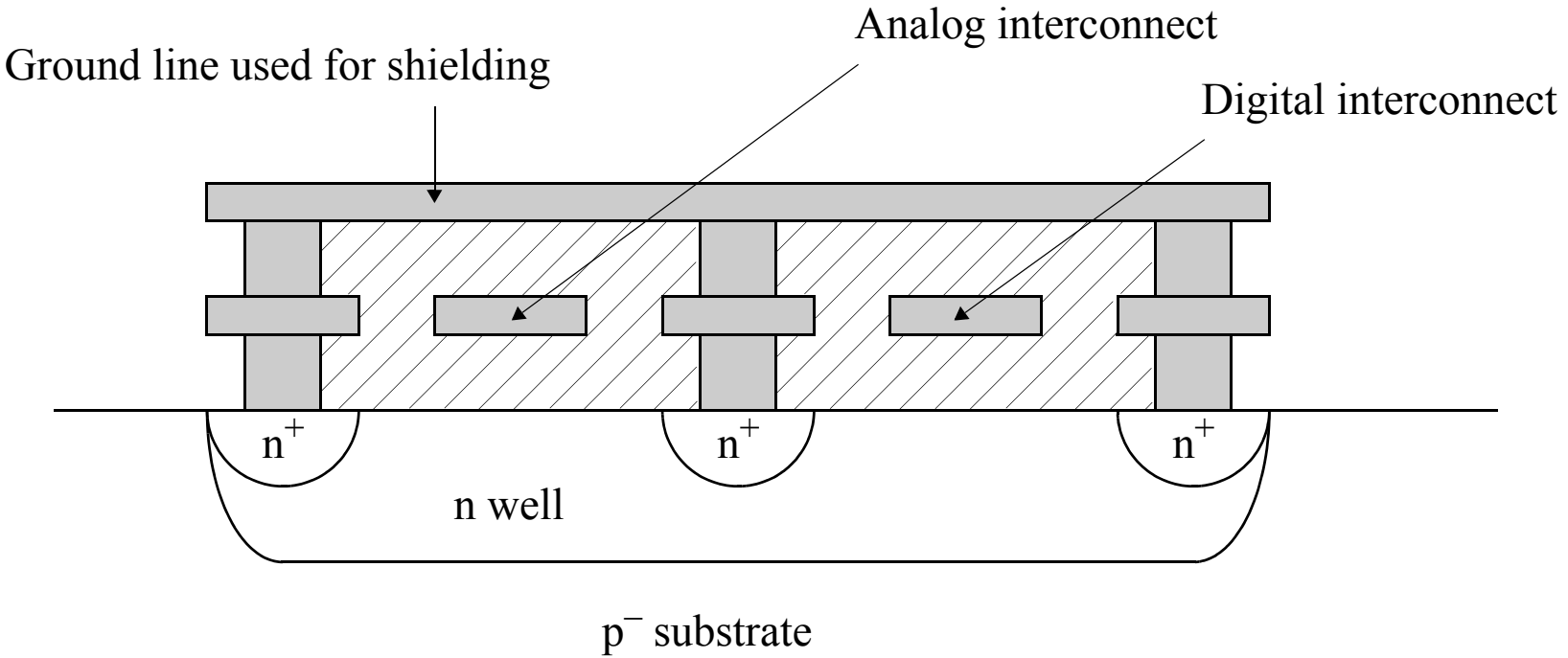
- Connect analog and digital supplies together as close to supply as possible

Guard Ring to Sheild Analog



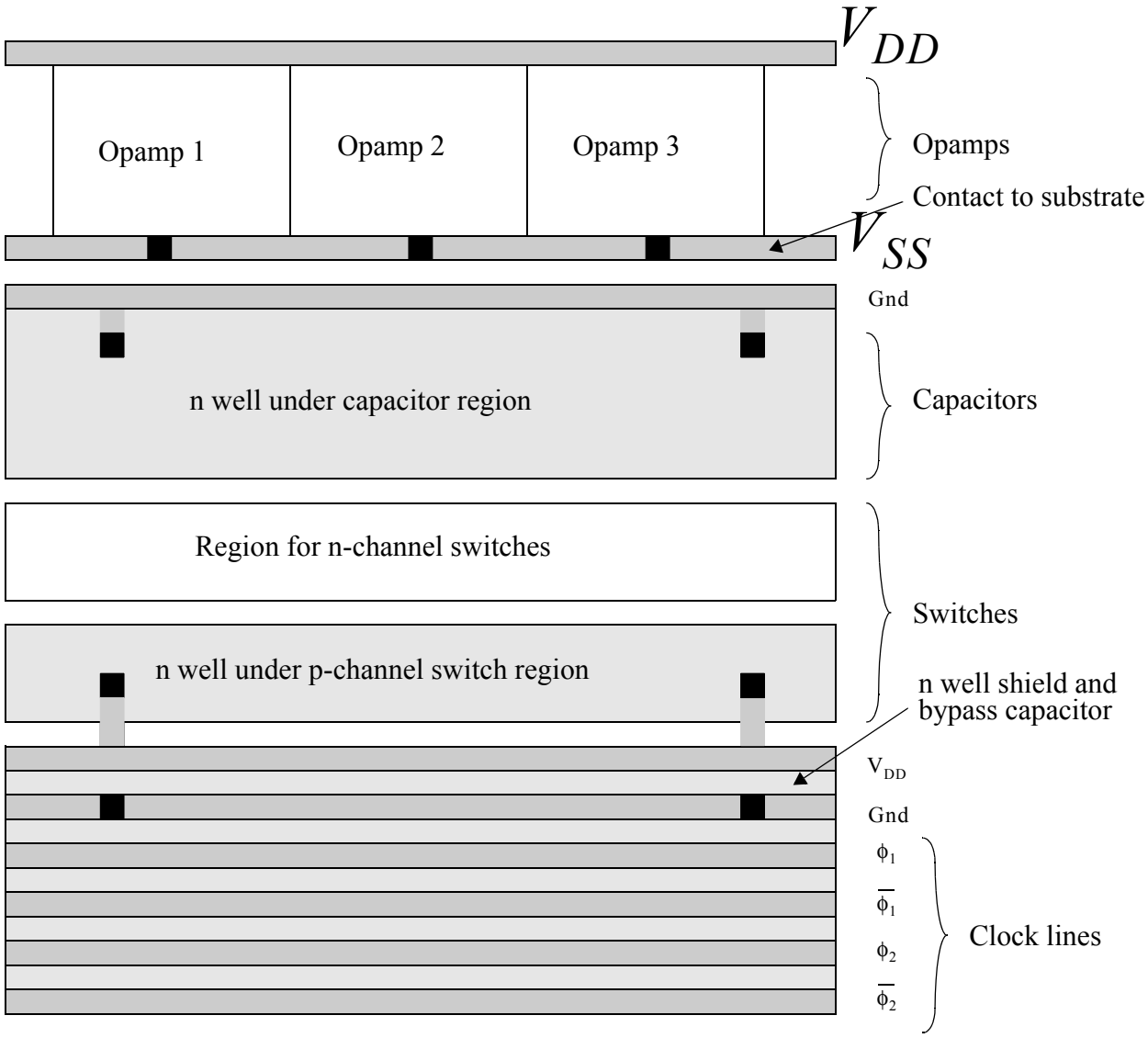
- Depth of well causes higher impedance since doping usually higher near surface of p- substrate (perhaps 10 times higher resistance!)

Sheilding Signals

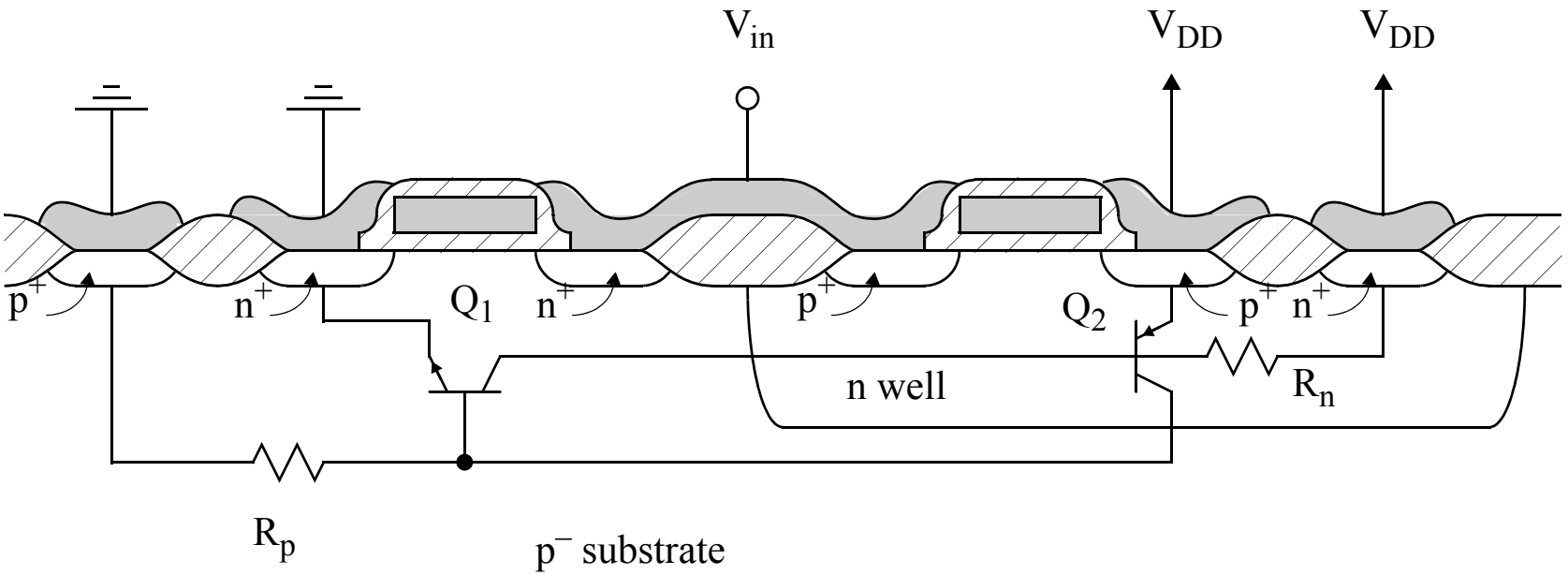


- Shields keep noise from being capacitively coupled into or out of substrate

Example Analog Floorplan

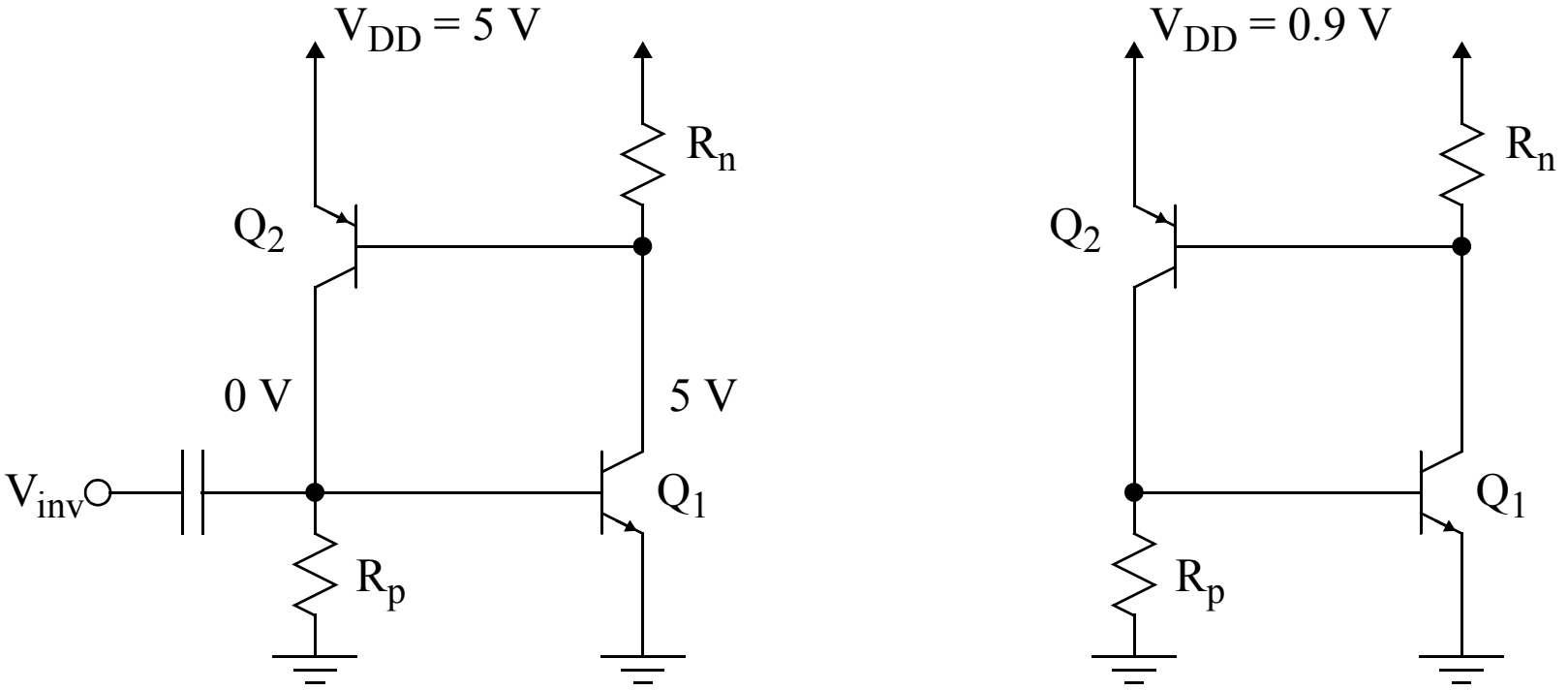


Latch-Up



- Occurs when large substrate or well currents
- Creates an SCR that might turn on and not off until harm done (or power turned off)

Latch-Up



- Capacitive coupling due to junction depletion caps of MOS drains
- Have many substrate contacts and guard rings