Chapter 13 - Problems

13.1) The longest duration for Phase II occurs when $V_{in} = V_{ref}$ in which the required number of clock cycles is

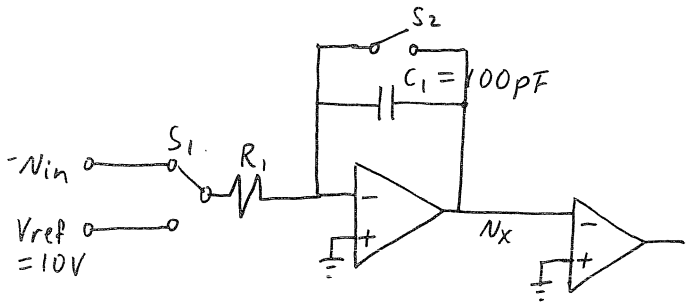
$$2^{18} + 1 = 2.62 \times 10^5 \text{ cycles}$$

$$\therefore T_2 = 2.62 \times 10^5 T_{clk} \quad \text{where } T_{clk} = 1/5MHz$$
$$= 52.4 \text{ msec}$$

and $T_1 = 2^{18} T_{clk} \approx T_2$

$\therefore$ the total conversion time is $T_1 + T_2 = \underline{105 \text{ msec}}$ maximum

13.2)



Find R_1

Worse case situation is when $V_{in} = 10V$

Now $T_1 = 2^{18} T_{clk} = 2^{18} \times \frac{1}{1MHz} = 0.262 \text{ sec}$

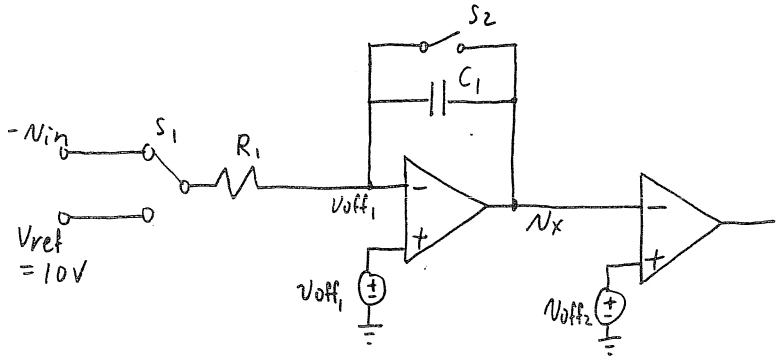
At the end of Phase I, set $v_x \equiv 10V$.

$$v_x = \frac{V_{in} T_1}{R_1 C_1} \Rightarrow R_1 = \frac{V_{in} T_1}{V_x C_1} = \frac{10 \times 0.262}{10 \times 100 \times 10^{-12}}$$

$$\underline{R_1 = 2.62 \text{ G}\Omega}$$

Note the large value required here.

13.3)



Derive Bout accounting for offset voltages.

During Phase I the input voltage is effectively

$$-(V_{in} + V_{off1})$$

and $V_x\Big|_{t=T_1} = \dfrac{(V_{in} + V_{off1})T_1}{R_1C_1}$ at the end of Phase I.

During Phase II, the reference voltage is effectively

$$V_{ref} - V_{off1}$$

$$\therefore \quad V_x(t) = -\frac{(V_{ref} - V_{off1})}{R_1C_1}(t - T_1) + \frac{(V_{in} + V_{off1})T_1}{R_1C_1}$$

$$= -\frac{V_{ref}}{R_1C_1}(t - T_1) + \frac{V_{in}T_1}{R_1C_1} + \frac{V_{off1}}{R_1C_1}t$$

The comparator now triggers when $V_x = V_{off2}$.

Solve for T_2:

$$V_x(T_2) = -\frac{V_{ref}}{R_1C_1}(T_2 - T_1) + \frac{V_{in}T_1}{R_1C_1} + \frac{V_{off1}}{R_1C_1}T_2 \equiv V_{off2}$$

$$\left(\frac{V_{ref}}{R_1C_1} - \frac{V_{off1}}{R_1C_1}\right)T_2 = \frac{V_{in}T_1}{R_1C_1} - V_{off2}$$

$$T_2 = \frac{V_{in}}{V_{ref} - V_{off1}}T_1 - \frac{V_{off2}R_1C_1}{V_{ref} - V_{off1}}$$

Now $T_1 = 2^N T_{clk}$

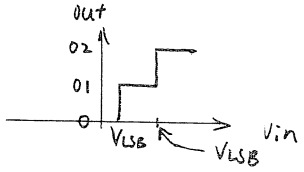
and $T_2 = 2^N B_{out} T_{clk} = T_1 B_{out}$

$$\therefore \quad B_{out} = \frac{T_2}{T_1} = \frac{V_{in}}{V_{ref} - V_{off1}} - \frac{V_{off2}R_1C_1}{V_{ref} - V_{off1}} \times \frac{1}{T_1}$$

$$B_{out} = \frac{V_{in} + err}{V_{ref} - V_{off1}} \quad \text{where } err = \frac{R_1C_1}{T_1}V_{off2}$$

$\therefore$ V_{off1} is equivalent to an error in the reference voltage while V_{off2} is equivalent to an offset in the input signal.

13.4) Find offset error given $V_{off_1} = 20mV$.



(ignore the ½ V_{LSB} offset that is normally present)

From the above transfer characteristic we expect ideally that if $v_{in} = V_{LSB}$, the output is 00001H (Hex)

or $B_{out} = 2^{-N} = \frac{T_2}{T_1} = \frac{T_2}{2^N T_{clk}}$

$\therefore$ $\underline{T_2 = T_{clk}}$

With the offset, however, from Problem 13.3,

$$T_2 = \frac{v_{in}}{V_{ref} - V_{off_1}} T_1 - \frac{V_{off_2} R_f C_1}{V_{ref} - V_{off_1}} \quad \because V_{off_2} = 0$$

$$= \frac{V_{LSB}}{V_{ref} - V_{off_1}} \times 2^N T_{clk} = \frac{V_{ref}}{(V_{ref} - V_{off_1})} \times T_{clk}$$

$$= \frac{10}{(10 - 0.02)} T_{clk} = \underline{1.002\, T_{clk}}$$

As each T_{clk} corresponds to 1 LSB, the offset voltage has created an offset error of $1.002 - 1\,LSB = 0.002$ LSB

13.5) The frequencies that are completely attenuated are those with periods that are a multiple of the integration time, T_1

$$T_1 = 2^N T_{clk} = 2^{16} \times \frac{1}{10^6 Hz} = 65.54\,msec$$

$$= \underline{1/15.3\,Hz}$$

$\therefore$ all multiples of 15.3 Hz are completely attenuated.

At 60Hz, the attenuation is

$$\frac{|\sin(\pi f T_1)|}{\pi f T_1} = \frac{|\sin(\pi \times 60/15.3)|}{\pi\, 60/15.3} = 1.98 \times 10^{-2}$$

$$= \underline{-34\,dB}$$

13.6) Repeating Problem 13.5 with $f_{clk} = 100\,kHz$.

$$T_1 = 2^N T_{clk} = 2^{16} \times \frac{1}{10^5 Hz} = 655.4\,msec$$
$$= 1/1.53\,Hz$$

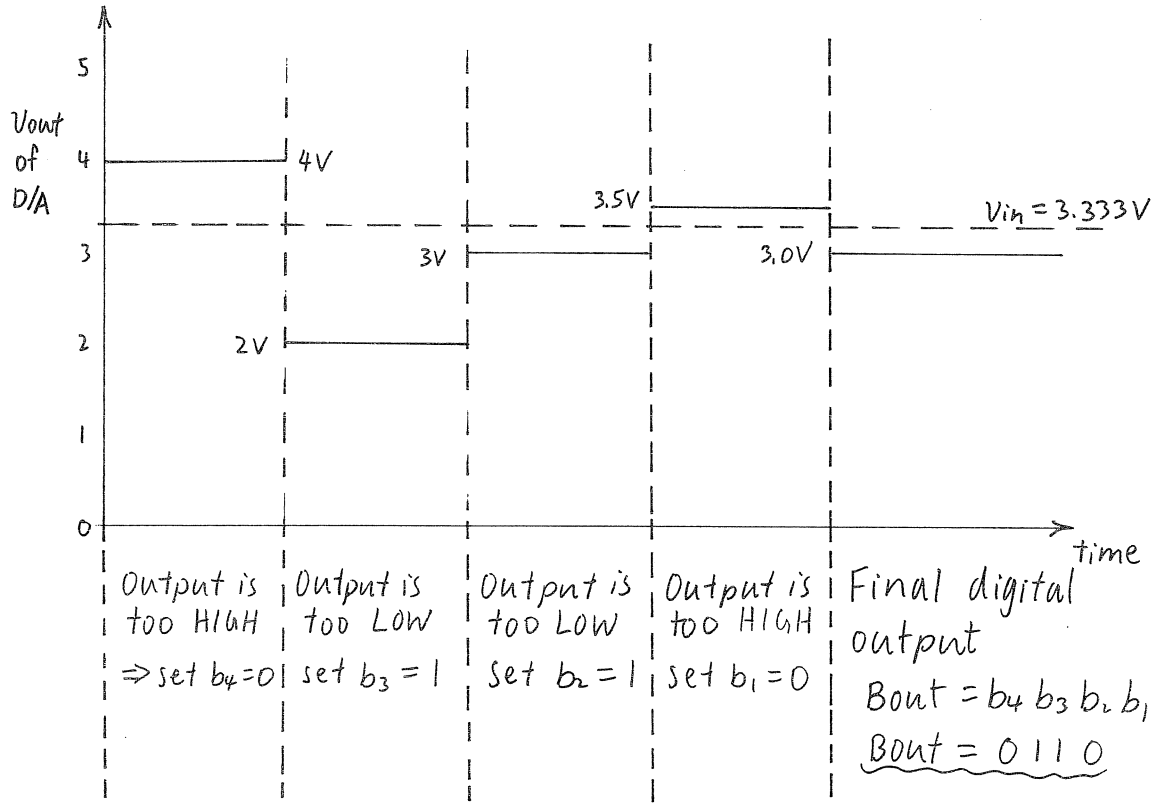
∴ all multiples of 1.53 Hz are attenuated

At 60 Hz, the attenuation is

$$\frac{|\sin(\pi f T_1)|}{\pi f T_1} = \frac{|\sin(\pi\, 60/1.53)|}{\pi\, 60/1.53} = 5.09 \times 10^{-3}$$

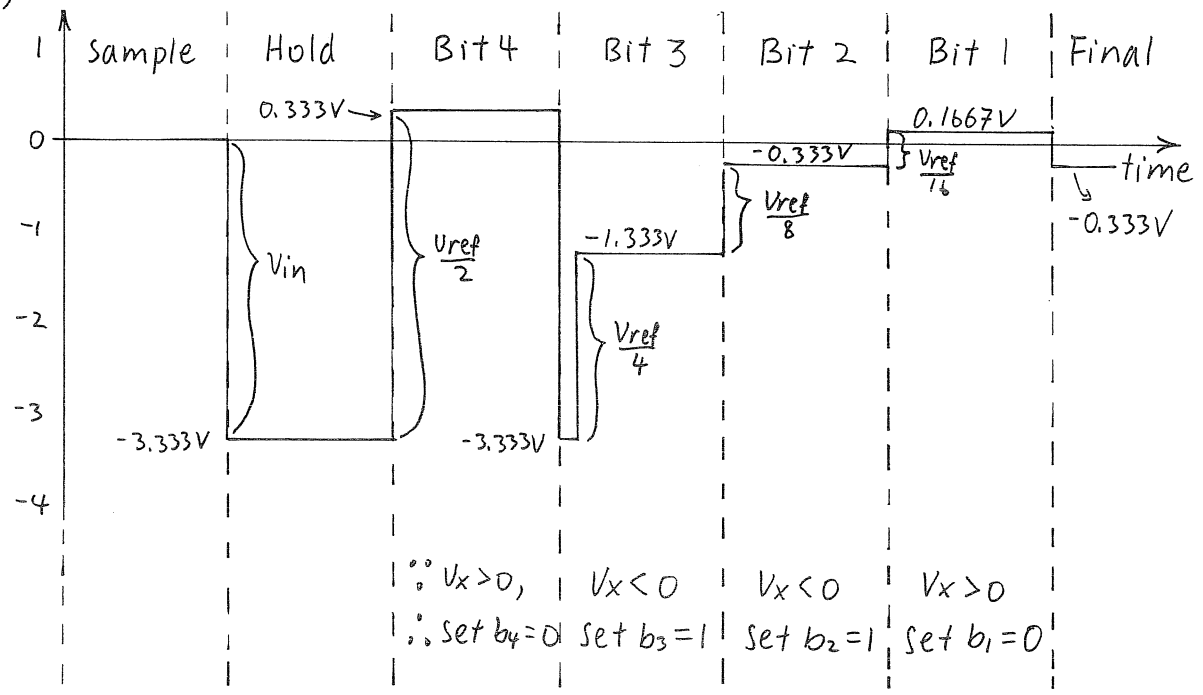
$$= \underline{-46\,dB}$$

13.7)



Final digital output $\underline{Bout = 0110}$

13.8)

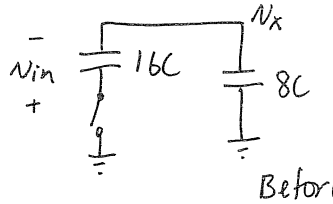


Final output Bout = $b_4 b_3 b_2 b_1$

= 0110

13.9) Repeat Problem 13.8 assuming a parasitic capacitance of 8C.

Hold mode:



Charge conservation (Before / After)

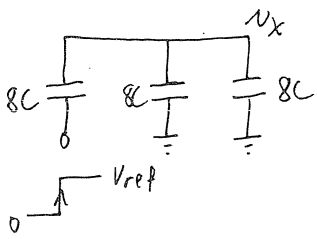
$Q = CV = C'V'$

$-16C \times V_{in} = 24C \cdot V_x$

$\therefore \quad V_x = -\frac{2}{3} V_{in} = -\frac{2}{3} \times 3.333V$

$= -2.222V$

Bit 4 cycle:



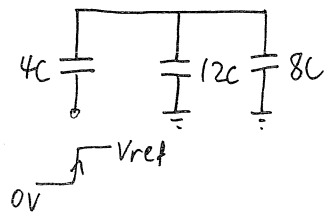
$\Delta V_{x b4} = \frac{8C}{24C} V_{ref} = \frac{2}{3} \times \frac{1}{2} V_{ref} = \frac{1}{3} \times 8V$

$= 2.667V$

(cont.)

13.9 (cont.)

Bit 3 cycle:



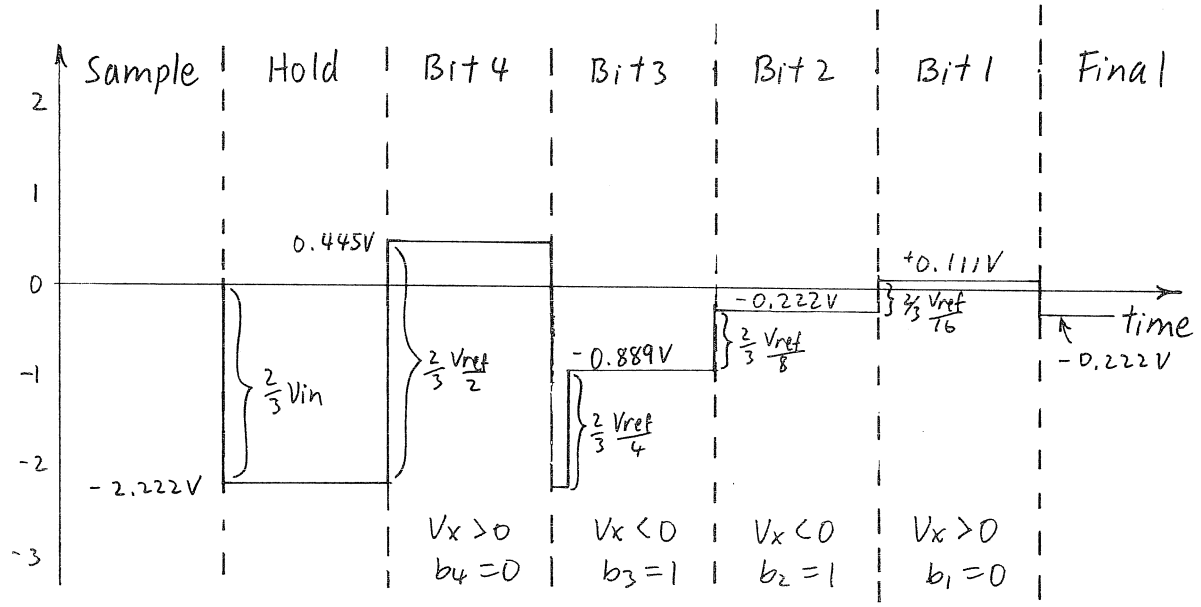
$$\Delta V_{xb_3} = \frac{4C}{24C} V_{ref} = \frac{2}{3} \times \frac{1}{4} V_{ref} = \frac{1}{6} \times 8V$$
$$= 1.333V$$

Similarly for

Bit 2 cycle, $\Delta V_{xb_2} = \frac{2C}{24C} V_{ref} = \frac{2}{3} \times \frac{1}{8} V_{ref} = 0.667V$

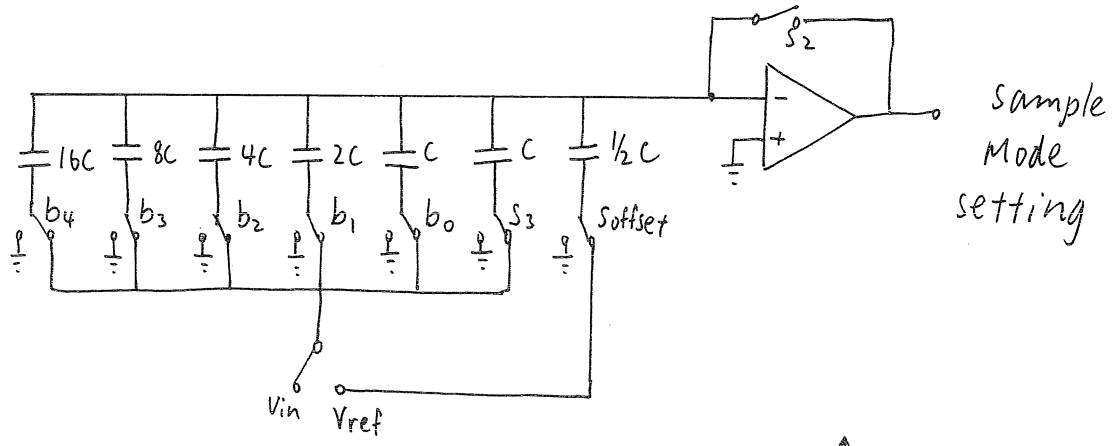
Bit 1 cycle, $\Delta V_{xb_1} = \frac{C}{24C} V_{ref} = \frac{2}{3} \times \frac{1}{16} V_{ref} = 0.333V$

Note: All voltage swings are 2/3 the original values but the final Bout result will remain unchanged.



Final output, Bout = $b_4 b_3 b_2 b_1$ = 0 1 1 0

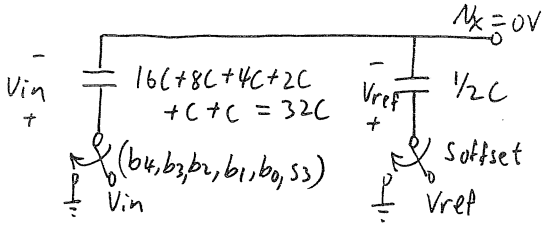
13.10)



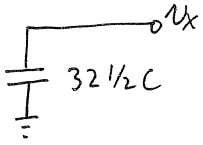
Charge redistribution A/D with offset

Explanation of operation:

At the end of the sample mode, we have



During the Hold phase, switches $b_4, b_3, b_2, b_1, b_0, s_3$ and soffset go to ground resulting in



By charge conservation

$$\underbrace{32C \times (-V_{in}) + \tfrac{1}{2}C(-V_{ref})}_{\text{BEFORE}} = \underbrace{32\tfrac{1}{2}C \times V_x}_{\text{AFTER}}$$

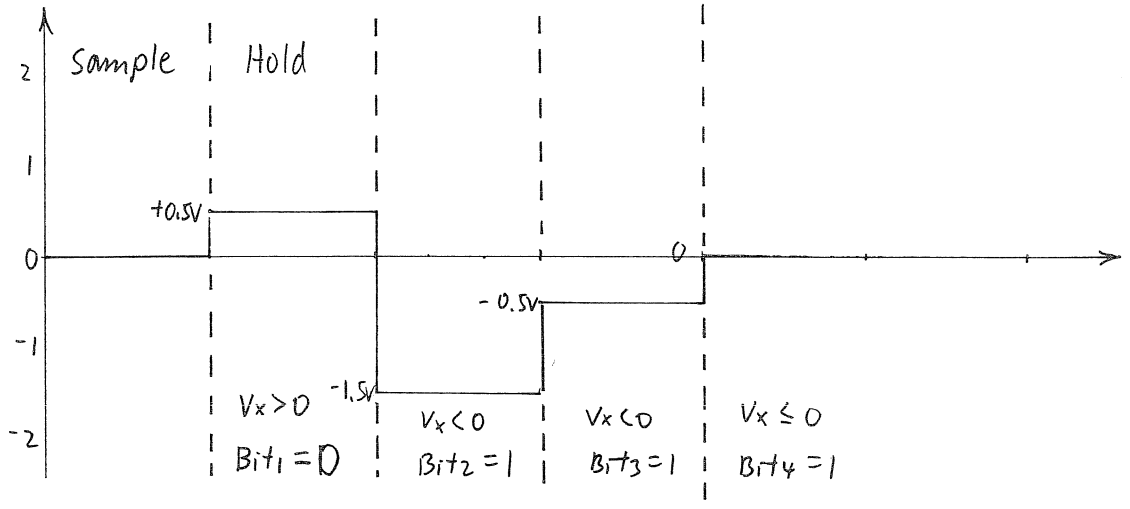
$$\therefore \quad V_x = -\frac{32}{32\frac{1}{2}} V_{in} - \frac{\frac{1}{2} V_{ref}}{32\frac{1}{2}}$$

$$= -\frac{32}{32\frac{1}{2}} \left(V_{in} + \tfrac{1}{64} \times V_{ref} \right)$$

Thus we see that we have created an offset in V_{in} of $\frac{1}{64} \times V_{ref}$ which is equivalent to ½ LSB. Afterwards, the ½C cap. acts as a parasitic cap. to ground, causing only a small degradation in the signal gain ($\approx 1.5\%$).

13.11) The output code from the signed charge-distribution A/D converter can be converted to a two's complement code by simply inverting the MSB.

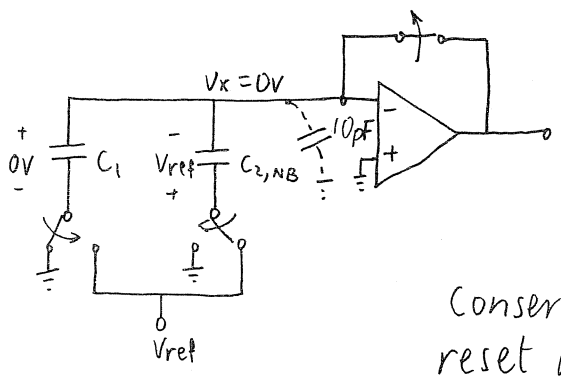
Example: A 4-bit converter with $V_{ref} = 8V$ and $V_{in} = -1V$



$\therefore$ Bout $= b_1 b_2 b_3 b_4 = \boxed{0}111$ represented by

while in 2's complement code $-1V$ is $\boxed{1}111$.

13.12) Find V_x and show $V_{e1} = 1/2\, V_{x1}$



$C_p = 10pF$

The voltage levels and switching directions correspond to the end of the reset phase.

Conservation of charge between reset and calibration stages gives

$$C_1 \cancel{\times 0V} + C_{2,NB} \times (V_{ref}) + \cancel{C_p \times 0V} = C_1 (V_{x_1} - V_{ref}) + C_{2,NB} V_{x1} + C_p V_{x1}$$

$$V_{ref}(-C_{2,NB} + C_1) = V_{x1}(C_1 + C_{2,NB} + C_p)$$

But $C_T = C_1 + C_{2,NB}$ and $C_1 = \frac{C_T}{2} + \Delta C_1$

$\therefore -C_{2,NB} + C_1 = -(\frac{C_T}{2} - \Delta C_1) + \frac{C_T}{2} + \Delta C_1 = 2\Delta C_1$

(cont.)

13.12 (cont.)

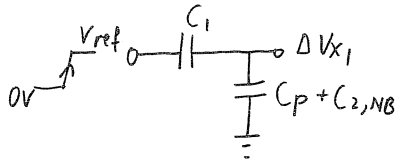
$$\therefore \quad V_{ref} \times 2\Delta C_1 = V_{x1}(C_T + C_p)$$

$$\underline{V_{x1} = \frac{2\Delta C_1}{C_T + C_p} V_{ref}}$$

Here $\Delta C_1 = C_1 - \frac{C_T}{2} = 31.5 - 32\,pF = -0.5\,pF$

$$\therefore \quad \underline{V_{x1}} = \frac{2 \times (-0.5)}{64 + 10} V_{ref} = \underline{-1.35 \times 10^{-2} V_{ref}}$$

To determine V_{e1}, note that during bit 1 of the conversion process, only C_1 is switched from ground to V_{ref}. All other switches are unchanged. Hence the voltage change in V_{x1}, ΔV_{x1}, is given by a capacitive divider rule



$$\Delta V_{x1} = \frac{C_1}{C_1 + C_{2,NB} + C_p} V_{ref}$$

$$= \frac{C_T/2 + \Delta C_1}{C_T + C_p} V_{ref}$$

$$= \left[\frac{1}{2} \frac{C_T}{C_T + C_p} + \frac{\Delta C_1}{C_T + C_p} \right] V_{ref}$$

Ideally $\Delta C_1 = 0$ and

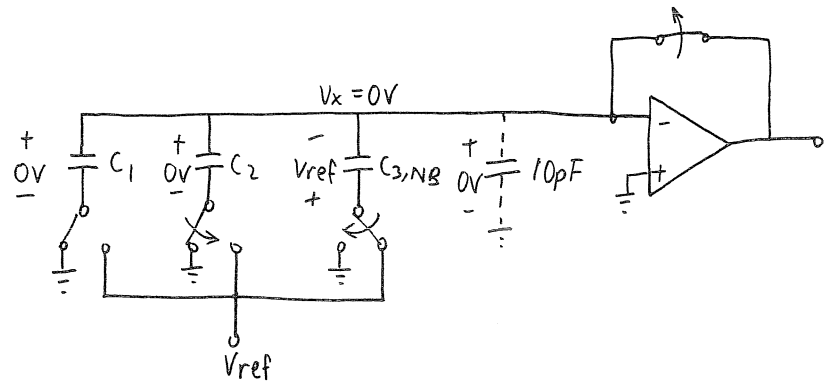
$$\Delta V_{x1} = \frac{1}{2} \frac{C_T}{C_T + C_p} V_{ref}$$

$$\therefore \quad V_{e1} \equiv \Delta V_{x1} - \Delta V_{x1\,ideal} = \frac{\Delta C}{C_T + C_p} V_{ref}$$

or $\underline{V_{e1} = 1/2\, V_{x1}}$

13.13) Find V_{x2} and show $V_{e2} = \frac{1}{2}(V_{x2} - V_{e1})$.

Continuing from Problem 13.12, we now analyze the calibration of C_2.



As in Problem 13.12, the diagram shows the voltage levels and switching that occurs at the end of the reset phase. Charge conservation gives

$$C_1 \times 0V + C_2 \times 0V - C_{3,NB} V_{ref} + C_p \times 0V = C_1 V_{x2} + C_2(V_{x2} - V_{ref}) + C_{3,NB} V_{x2} + C_p V_{x2}$$

$$(C_2 - C_{3,NB}) V_{ref} = (C_1 + C_2 + C_{3,NB} + C_p) V_{x2} \quad [1]$$

Now $C_2 = \frac{C_T}{4} + \Delta C_2$

and $C_1 + C_2 + C_{3,NB} = C_T$

$$\therefore \quad C_{3,NB} = C_T - C_1 - C_2$$

$$= C_T - \left(\frac{C_T}{2} + \Delta C_1\right) - \left(\frac{C_T}{4} + \Delta C_2\right)$$

$$= \frac{C_T}{4} - \Delta C_1 - \Delta C_2 \quad [2]$$

[2] → [1]

$$\left[\left(\frac{C_T}{4} + \Delta C_2\right) - \left(\frac{C_T}{4} - \Delta C_1 - \Delta C_2\right)\right] V_{ref} = (C_T + C_p) V_{x2}$$

$$V_{x2} = \frac{\Delta C_1 + 2\Delta C_2}{C_T + C_p} V_{ref}$$

$$\therefore \quad \underline{V_{x2} = \tfrac{1}{2} V_{x1} + \frac{2\Delta C_2}{C_T + C_p} V_{ref}} \quad [3]$$

Using $C_2 = 16.4\,pF$ and $V_{x1} = -1.35 \times 10^{-2} V_{ref}$ from Problem 13.12,

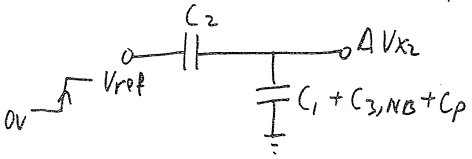
$$V_{x2} = \tfrac{1}{2}(-1.35 \times 10^{-2} V_{ref}) + \frac{2(16.4 - 16)}{64 + 10} V_{ref}$$

$$\underline{V_{x2} = -2.7 \times 10^{-3} V_{ref}}$$

(cont.)

13.13 (cont.)

During bit 2 of the conversion process only C_2 is switched from ground to Vref. Thus the change in V_{x2}, ΔV_{x2} is given by



$$\Delta V_{x_2} = \frac{C_2}{C_1 + C_2 + C_{3,NB} + C_p} V_{ref}$$

$$= \frac{C_T/4 + \Delta C_2}{C_T + C_p} V_{ref}$$

$$= 1/4 \frac{C_T}{C_T + C_p} V_{ref} + \frac{\Delta C_2}{C_T + C_p} V_{ref}$$

Ideally $\Delta C_2 = 0$

$\therefore$ $\Delta V_{x2\,ideal} = \frac{1}{4} \frac{C_T}{C_T + C_p} V_{ref}$

$\therefore$ $V_{e2} \triangleq \Delta V_{x2} - \Delta V_{x2\,ideal} = \frac{\Delta C_2}{C_T + C_p} V_{ref}$ [4] and $V_{e1} = 1/2 V_{x1}$ [5]

[5],[4] → [3] $V_{x2} = V_{e1} + 2 V_{e2}$

or $V_{e2} = 1/2 (V_{x2} - V_{e1})$

13.14) Find the settling time.

Given: $R_{sw} = R_{s1} = R = R_{s2} = 1k\Omega$

$C_T = 128\,pF$

From Eq. (13.27),

$$\tau_{eq} = (R_{s1} + R + R_{s2}) 2^N C = 3 \times R_{sw} \times C_T = 3 \times 1000 \times 128 \times 10^{-12}$$

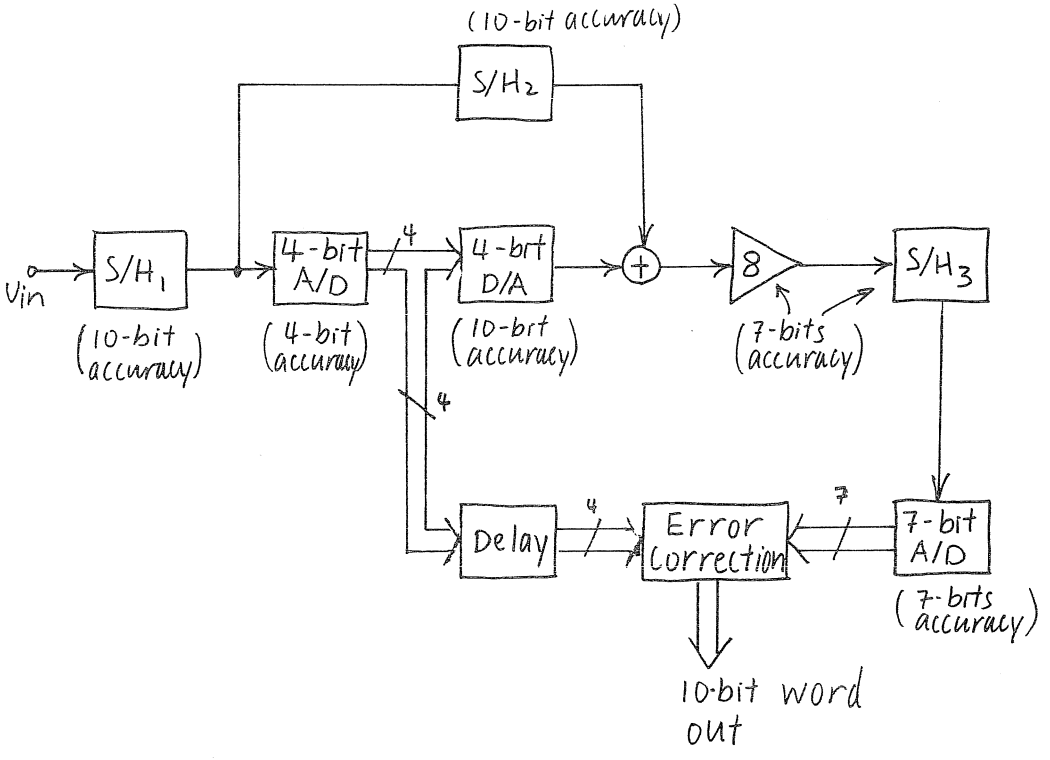
$$= 0.384\,\mu sec$$

From Eq. (13.29),

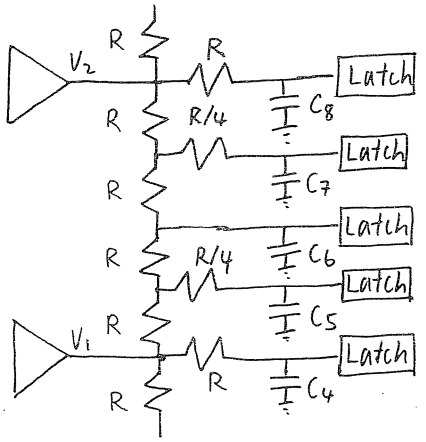
Settling time, $T = 0.69 (N+1) \tau_{eq} = 0.69 \times 13 \times 0.384\,\mu sec$

$= 3.44\,\mu sec$

13.15) A 10-bit, 2-step A/D converter:



13.16) The input capacitances of the latches are shown explicitly here:



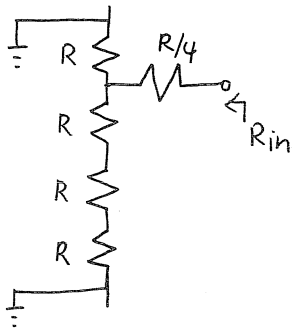
Assume nodes V_1 and V_2 are driven by low impedance op-amps (i.e., assume zero impedance outputs)

(cont.)

13.16 (cont.)

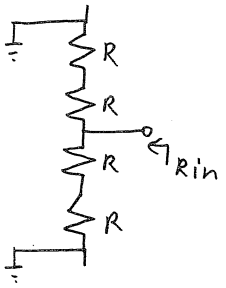
- From the diagram, it is clear that C_8 sees an impedance R to node V_2.

- C_7 sees



$$R_{in} = R/4 + (R \,//\, 3R)$$
$$= R/4 + \frac{3R^2}{4R}$$
$$= R$$

- C_6 sees



$$R_{in} = 2R \,//\, 2R$$
$$= \frac{4R^2}{4R}$$
$$= R$$

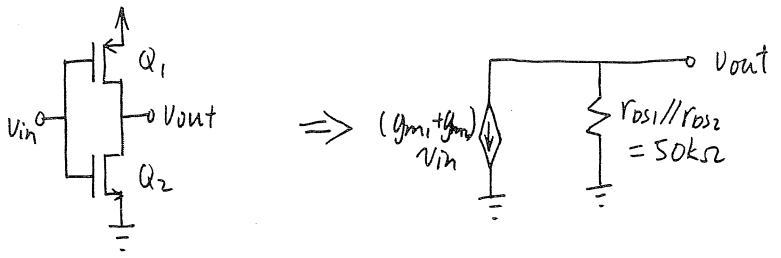
- C_5 sees the identical resistor network as C_7
  ∴ $R_{in} = R$.

- C_4 sees the same resistor network as C_8 and the entire structure is repeated.

  ∴ All latch capacitances have an impedance of R associated with them.

  If we assume all capacitances are equal to C then all time constants are equal to RC.

13.17)



$$gain = -(g_{m1} + g_{m2}) \times r_{os1} // r_{os2}$$

$$g_{m2} = \mu_n C_{ox} \left(\frac{W}{L}\right)_2 V_{eff} = 100\ \mu A/V^2 \times 1 \times (2.5-1)$$
$$= 0.15\ mA/V$$

$$g_{m1} = \mu_p C_{ox} \left(\frac{W}{L}\right)_1 V_{eff} = 50\ \mu A/V^2 \times 2 \times (2.5-1)$$
$$= 0.15\ mA/V$$

$\therefore$ gain $= -0.3\ mA/V \times 50\ k\Omega$
$= \underline{-15}$

$\therefore$ A $\frac{1V}{15} = \underline{67\ mV}$ differential input is required to produce a 1V output change.

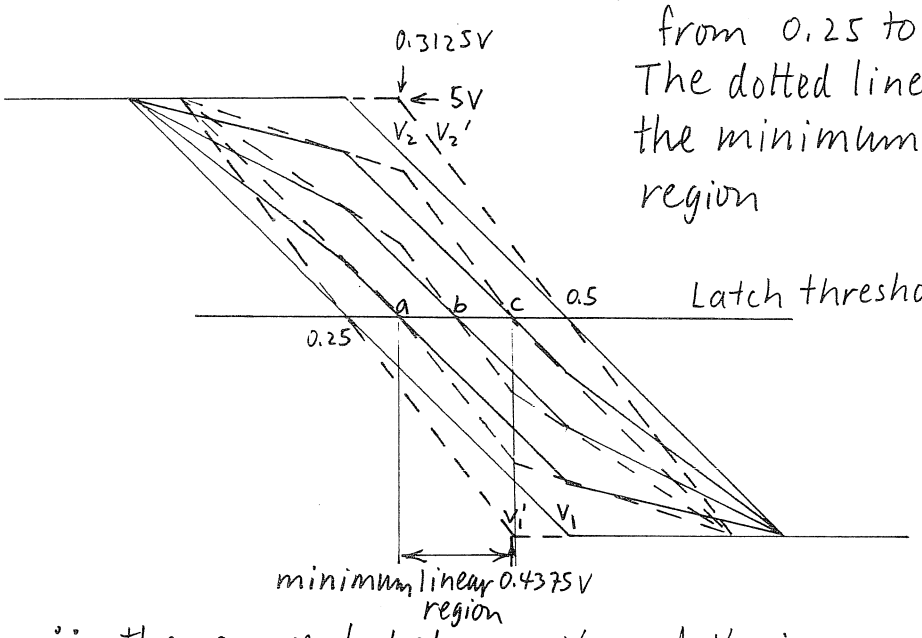
If $\frac{1}{2} V_{LSB} = 67mV$ or $V_{LSB} = 133\ mV$,
then the maximum number of bits this comparator can determine is given by N where

$$V_{LSB} = \frac{V_{ref}}{2^N}$$

$$\therefore\ 2^N = \frac{V_{ref}}{V_{LSB}} = \frac{5V}{0.133V} = 37.5$$

$$\underline{N} = 5.2\ bits \Rightarrow \underline{5\ bits}$$

13.18) For the minimum linear region, we can draw a simplified line diagram representing the linear and saturated regions of operations of the input amplifiers. The solid lines represent a linear region from 0.25 to 0.5V. The dotted lines represent the minimum linear region



$\therefore$ the current between V_1 and V_2 is

$$i = (V_2 - V_1)/4R$$

$$\therefore V_{2a} = V_1 + iR = V_1 + \frac{V_2 - V_1}{4}$$

$$= 3/4\, V_1 + (V_2)/4$$

Similarly

$$V_{2b} = 1/2\,(V_1 + V_2)$$

$$V_{2c} = (V_1)/4 + 3/4\, V_2$$

} Interpolated lines between V_1 and V_2

These lines are shown in the above diagram and are marked a, b, and c. We can see that the lines are evenly spaced across the threshold crossing as long as the linear region covers the crossing points of V_{2a} and V_{2c}

Thus the minimum linear region is

$$0.25 + \frac{0.25}{4} < V_{in} < 0.5 - \frac{0.25}{4}$$

$$\underline{0.3125V < V_{in} < 0.4375V}$$

13.19) The key limitation to the speed of an A/D converter is its ability to sample the input signal to within ½ LSB of accuracy.

For a clocked flash or interpolating A/D converter, this largely relates to the ability to synchronize the sampling times of the individual components. This can be accomplished by matching impedances and clock skew within the circuitry. With sample-and-hold circuits, however, we are faced with multiple challenges such as charge injection, signal-dependent jitter and parasitic capacitances which can cause signal feedthrough at high frequencies. Combined together, these problems can often prove more difficult to resolve than those associated with flash or interpolating designs.

13.20)

$$\text{folding rate} \times \#\text{ folding blocks}$$

$$= \frac{2^N}{\#\text{ latches}} \times \frac{1\text{ latch}}{\#\text{ folding blks}} \times \#\text{ folding blocks}$$

$$= 2^N$$

13.21) Given: N-bits with folding rate of 2^F

$$\text{Now } FR = \frac{2^N}{\#\text{ latches}}$$

$$\therefore \#\text{ latches} = \frac{2^N}{FR} = \frac{2^N}{2^F} = 2^{N-F}$$

13.22)

Design Ⓐ :
- 8-bit folding/interpolating A/D
- 4 folding blocks
- 5-bits MSB, 3-bits interpolation

Design Ⓑ :
- straight interpolating A/D
- same input capacitive load as Design Ⓐ

Design Ⓒ :
- 8-bit flash A/D

Let C_{dp} be the input capacitance associated with a differential pair

The input capacitance of design Ⓒ, $C_{in\text{Ⓒ}}$ is

$$C_{in\text{Ⓒ}} = 2^8 C_{dp} = \underline{256 C_{dp}}$$

For Design Ⓐ, a folding rate of 8 gives 3-bits, and 4 folding blocks give 2-bits.

∴ An interpolation by 8 is required to obtain the remaining 3-bits needed for an 8-bit converter.

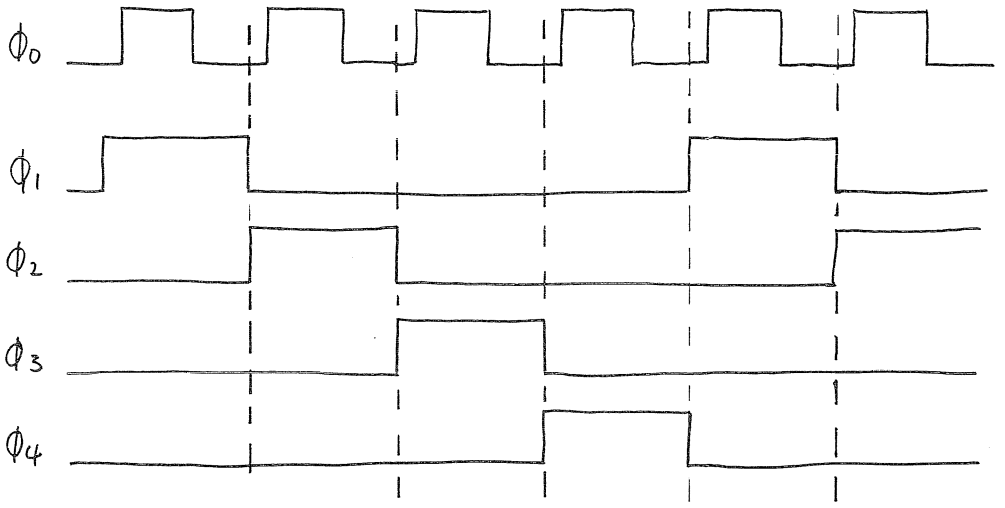
∴
$$C_{in\text{Ⓐ}} = \#\text{folding blocks} \times C_{\text{folding block}}$$
$$= 4 \times (\text{folding rate} \times C_{dp})$$
$$= \underline{32 C_{dp}}$$

∴ Between the folding/interpolating design Ⓐ and the flash design Ⓒ, there is a reduction factor of

$$\frac{C_{in\text{Ⓒ}}}{C_{in\text{Ⓐ}}} = \frac{256 C_{dp}}{32 C_{dp}} = \underline{8 \text{ in input capacitance.}}$$

In order for design Ⓑ to have the same input capacitance as Design Ⓐ, an interpolation factor of 8 must be used. Thus we need 8 resistors between the input caparators.

13.23) Assume that sampling occurs a signal is HIGH.



Note: ideally Phase ϕ_0 should slightly lag behind the other phases to ensure that the second stage S/H circuits have the most stable inputs from the first stage.