1 Description

The goal of this lab is to use commercial logic synthesis tool to synthesize the outputs of your behavioral synthesis tool into a netlist of gates. Synopsys and the CMC 0.35 design kit should be used. To use Synopsys logic synthesis tool:

>`source /CMC/tools/synopsys/source.csh`

For online documentation of Synopsys:

>`sold`

The following tasks should be completed for each benchmark:

- Synthesis scripts for timing and area optimization should be developed respectively.
- Detailed timing and area report should be generated.

2 Deliverables

One directory for each benchmark containing the following:

- The source code of your synthesis script;
- A Makefile that includes
  - a build target builds the C program into the synthesized logic netlist as well as the timing and area report;
  - A final report which document the implementation of the entire project as well as an analysis the synthesis result. A discussion on lessons learned and future work should also be included.

3 Due Date

5pm, May 7, Wednesday 2003.