

ECE1371S Design Exercise

Due Date: Monday, April 23, 2001

Design a 3-stage op-amp circuit using nested Gm-C compensation [1] for a 0.8 μm CMOS process, and apply it in a non-inverting, unity-gain configuration. While meeting the specifications in Table 1, optimize for (i.e., minimize) power dissipation. Level 3 HSPICE MOSFET models are available on the ECE1371 home page under "Design Exercise"/"MOSFET models used in textbook".

Table 1: Opamp Specifications

Parameter	Value
DC Open Loop Gain	$> 70 \text{ dB}$
Unity gain Phase Margin	$> 60 \text{ degrees}$
Slew Rate	$\pm 5 \text{ V}/\mu\text{sec}$
Unity gain bandwidth	1 MHz
Capacitive load	5 pF
Supply voltages	$\pm 1 \text{ V}$

You should include the following in your report:

- a) A complete HSPICE listing of your final circuit
- b) A circuit diagram including all final values for your devices
- c) AC open-loop frequency response curve (magnitude and phase) showing DC gain and phase margin assuming unity gain feedback.
- d) Unity gain, closed-loop transient step response. Determine rising and falling slew rates and their corresponding 0.1% settling times.
- e) AC frequency response curve for unity gain configuration (magnitude only).

Reference:

[1]F. You, E. Sanchez-Sinencio, "Multistage Amplifier Topologies with Nested Gm-C Compensation," JSSC Dec. 1997, pp. 2000-2011.