Power Reduction in Pipelined A/D Converters

Term Paper

ECE1371

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1. Introduction

There are a large number of applications requiring to employ A/D converters with medium speed and medium resolutions such as 10-bits A/D converters for video rate applications like camcorders, wireless local area network transceivers and Cable Modems.

Except than the nature of the architecture, the recent technology of choice to implement integrated circuits makes the pipelined architecture favorable. Using CMOS makes realizing all parts of a mixed-mode circuit (where the analog circuits are combined with a high number of digital circuits acting as signal processing units and memory) feasible on a single substrate. The CMOS transistors have gained speed while operating by a low voltage supply and dissipating low power which are results of shrinking the feature size of the transistors.

Therefore most circuits are preferred to be designed in CMOS technology for single chip and low cost production. One of the advantages of CMOS transistors compared to bipolar transistors in analog design is realizing the circuits by switched capacitor techniques. This offers lower power dissipation and higher accuracy in the operation of the analog circuits compared to those realized by resistor based circuits in the bipolar technology.

The trend in CMOS technology is to shrink the size of transistors to reduce the strong lateral and vertical electric fields and also to reduce the supply voltage to avoid velocity saturation of electrons. Reducing supply voltage in digital circuits results in decreasing the power dissipation because the dynamic power is proportional to

$$P_d \propto CV^2 f \tag{1}$$

For analog circuits such as those being employed in pipelined A/D converters, the power dissipation is mainly determined by the static power dissipation. As indicated in more details in [1,2] the static power dissipation is inversely proportional to the supply voltage. It means that to achieve the same SNDR (Signal to Noise and Dynamic Ratio), reducing the supply voltage may result in increasing the final power dissipation of the analog circuits. This is intuitively true because more power is to be dissipated to overcome stronger noise and distortions in circuits with less supply voltage and less signal swing.

$$\mathrm{SNDR} = 10\log\left(\frac{\text{Signal power [rms]}}{\text{(Noise power + Distortion power) [rms]}}\right) \quad \mathrm{dB} \tag{2}$$

Therefore the main concern in design of the pipelined A/D converters is to reduce the power dissipation while ensuring the resolution and the sampling speed are not deteriorated by the low supply voltage.

The operation of the pipelined architecture is briefly described in the next sections using systematic and circuit approach to help better understand how the power reduction methodology works on this architecture. The suggested method described in this paper are then introduced followed by results obtained from simulation.

2. Operation of the pipelined architecture

The pipelined A/D converter uses a tractable algorithm to extract codewords. As illustrated in Fig.1, a set of binary weighted, 4-bit digital codewords are assigned to a sine waveform to describe how the pipelined A/D converter works. The unipolar signal swing in the A/D converter is defined from 0 to the peak voltage of $+V_{ref}$ and is called the Full Scale peak-to-peak Range (FSR). As illustrated in Fig.1(a), the Most Significant Bit (MSB) is 1 for voltage levels higher than $\frac{1}{2}V_{ref}$ and is zero for voltage levels less than $\frac{1}{2}V_{ref}$. Therefore the MSB can be extracted easily by a comparator with threshold voltage of $\frac{1}{2}V_{ref}$. To continue extracting the codewords, the signal is mapped on its FSR, with respect to its remainder codewords as shown in Fig.1(b). For example, the voltage levels corresponding to the codewords of 1111 and 0111 are mapped on the same level because after the first MSB is extracted, both voltage levels have the same remaining codewords of X111 (X denotes don't care bit). By extracting the remainder MSB using a comparator with threshold at $\frac{1}{2}V_{ref}$ and continuing to map the signal based on its remainder bits on the FSR, an algorithm is developed to extract the equivalent binary codewords of a signal one by one from

MSB to LSB (Least Significant Bit). The mapping procedure is possible by subtracting a utility voltage (i.e. $\frac{D}{2} \times V_{ref}$, where D is either 0 or 1 when appropriate) from the signal and then amplifying the resultant residue by two with respect to the FSR. Ideally an infinite number of bits can be extracted from any voltage level by repeating the mapping procedure for an infinite number of iterations.

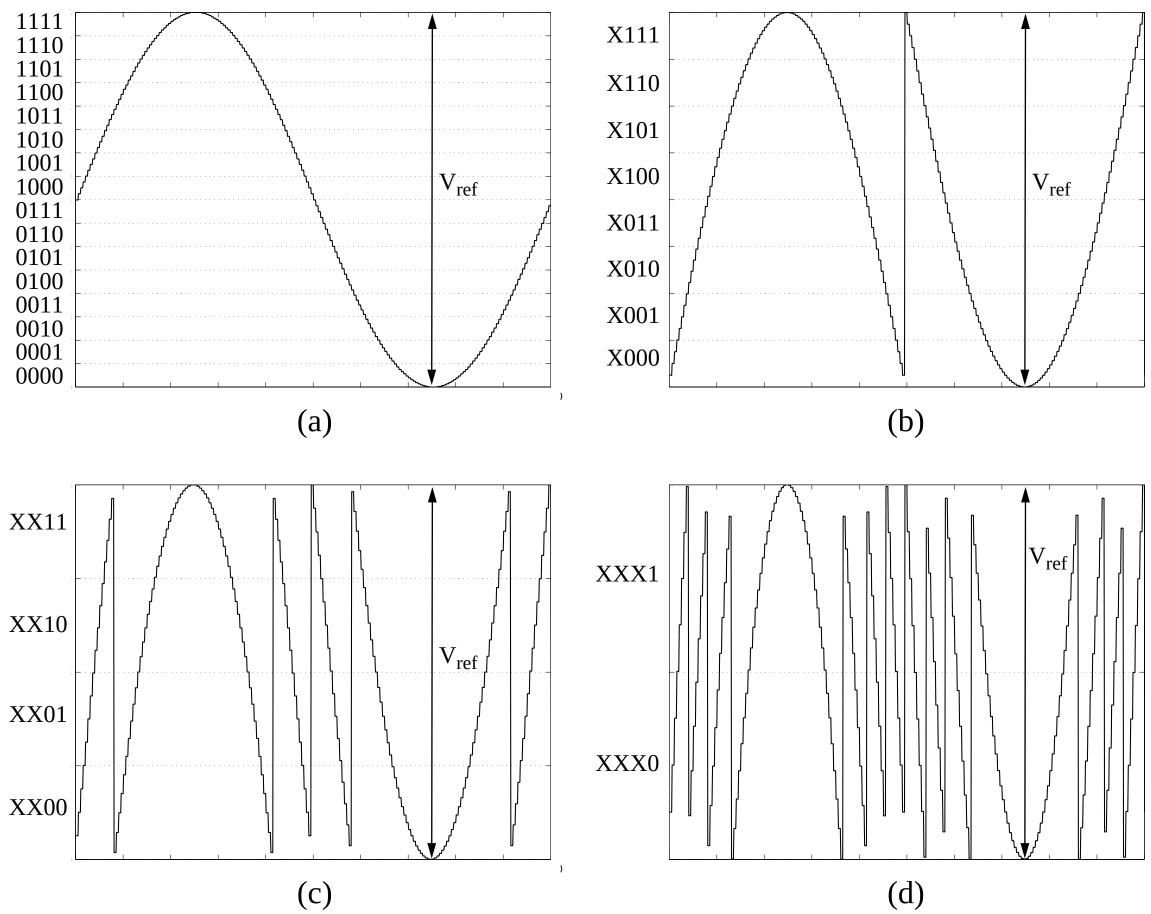

Fig. 1: Mapping procedure and codewords assignment in the pipelined A/D converter, (a) The input signal, (b) The first residue, (c) The second residue, (d) The third residue

3. Circuits in the pipelined architecture

The A/D converter architecture in Fig.2 includes the input track-and-hold (T&H) circuit and the pipelined stages. The pipelined stages are cascaded and each stage includes a subconverter A/D and the Multiplying Digital to Analog Converter (MDAC) block. The MDAC includes a subconverter D/A and the interstage sampling, subtracting and amplifying-by-2 circuit as shown in

Fig.3. The output from the T&H is fed to the first stage and in operation, during the sampling phase, the interstage amplifier in the MDAC samples the input residue and in parallel the subconverter A/D tracks and digitizes the input residue. In the amplification or the mapping phase, the extracted digital code is converted to a voltage level (i.e. 0 or $\frac{1}{2}V_{ref}$) by the subconverter D/A which is then subtracted from the sampled residue in the MDAC and the difference is amplified by two and is fed to the next stage.

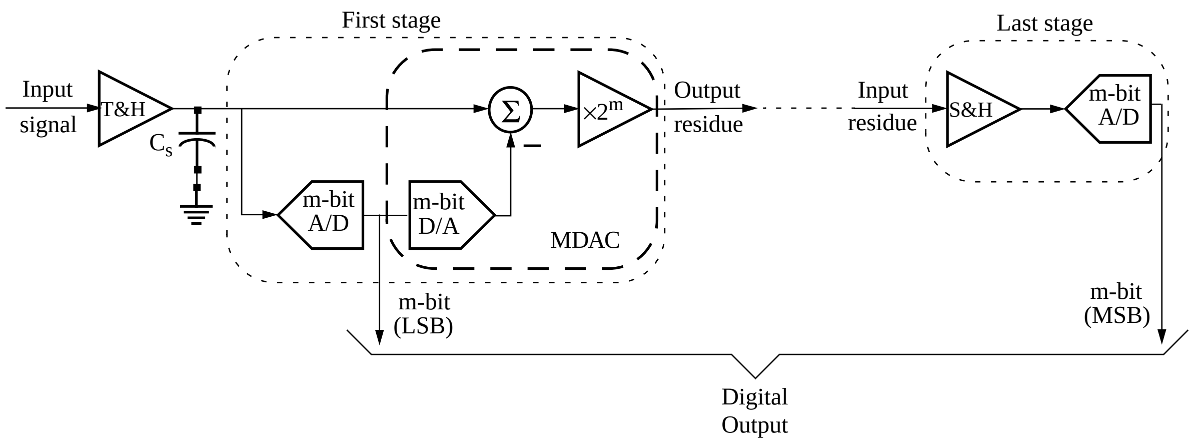

Fig. 2: Pipelined A/D converter system architecture

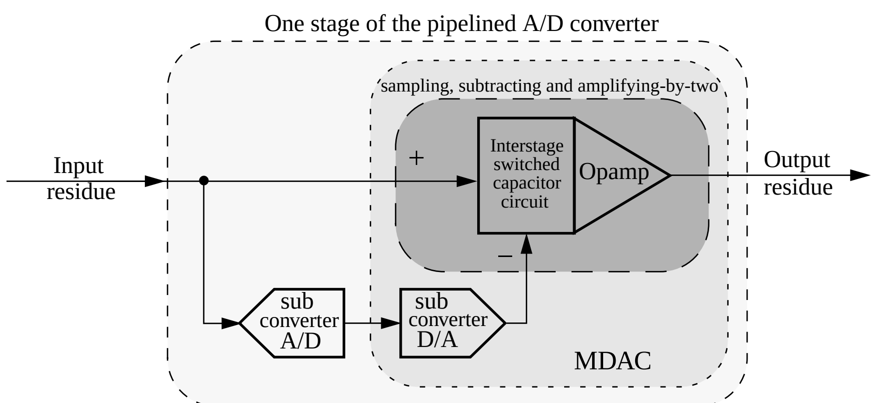

Fig. 3: The MDAC block in each stage of the A/D converter

A basic and practical circuit for the interstage switched capacitor circuit employed in MDAC is shown in Fig.4. A good choice for the opamp, specially for the purpose of the investigation in this paper is a two-stage architecture, shown in Fig.5, for which a complete characteristics and design steps can be found in [3].

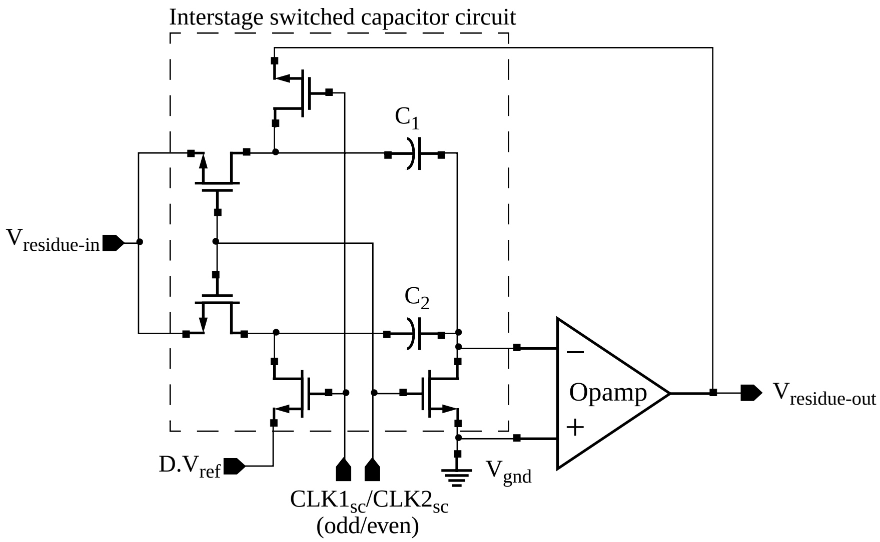

Fig. 4: Interstage sampling, subtracting and amplifying-by-two circuit

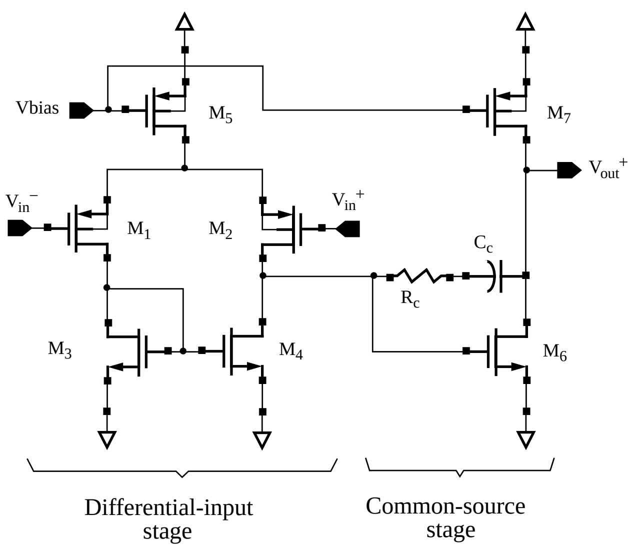

Fig. 5: Two-stage opamp

4. Power reduction methodology

Now after getting familiar with a simple pipelined architecture, we focus on how to reduce the power dissipation in CMOS pipelined A/D converters without degrading the resolution. For this purpose, noise is studied and modeled to account for possibility of power reduction.

4.1 Error sources

There are various noise sources in a CMOS A/D converter which deviate its operation from the ideal analytical approach during the design and fabrication. These factors are considered as error sources and degrade the overall performance of the system under investigation by contributing on the noise or distortion.

One type of the error sources comes from the circuit characteristics such as the finite gain, the signal swing and the settling time of the opamp (used in the interstage switched capacitor circuits). The finite gain of the opamp reduces the coefficient accuracy of the stage transfer function and the limited unity-gain frequency and the large settling-time of the opamp reduces the maximum conversion speed. The limited phase-margin or large overshoot in transient response of the opamp reduces the resolution of the A/D. Therefore the design of a fully differential opamp is one of the fundamental steps during the design of the A/D converter.

The nonidealities of the comparators (used in the subconverter A/Ds) should be also taken into the account. The offset voltage of the comparators results in missing codes in quantization transfer function and can be eliminated by auto-zero design techniques. The small gain in the comparator causes metastability problem and the kick-back noise of the latch circuit will introduce spikes in analog residue. Using a preamplifier followed by a dynamic latched comparator will significantly reduce these errors.

The clock feed-through and charge-injection of switches are another source of errors and can be cancelled by signal-varying bootstrap clock generators [4]. The final type of the error comes from the layout characteristics and includes mismatches and the mixed-signal noise. Assuming that all these errors are minimized during the design of the pipelined A/D converter, the main source of the error which is the concern of this paper is the thermal noise of the transistors which is stored in the feedback capacitors and changes the magnitude of the residue signal. This thermal noise, its modeling and how to deal with that are investigated more in the following sections.

4.2 Thermal noise

The noise contribution of transistors and the on-resistance of switches in A/D converter determines the amount of the SNR. The thermal noise is the dominant type of noise in the pipelined A/D converter and is caused by the random motion of electrons above absolute zero temperature. In each stage of the A/D converter, the thermal noise directly contributes to the residue signal which is stored in the feedback capacitors during the amplifying phase. Although all transistors and switches generate thermal noise, the main noise contribution in each stage comes from the opamp and the on-resistance of switches in the switched capacitor feedback network [5].

On the other hand, the most noise contribution among the pipelined stages comes from the first stage since the opamp input thermal noise from the succeeding stages are reduced by the gain of the preceding stages when referred to the input of the A/D converter. The noise model of the pipelined A/D converter is shown in Fig.6.

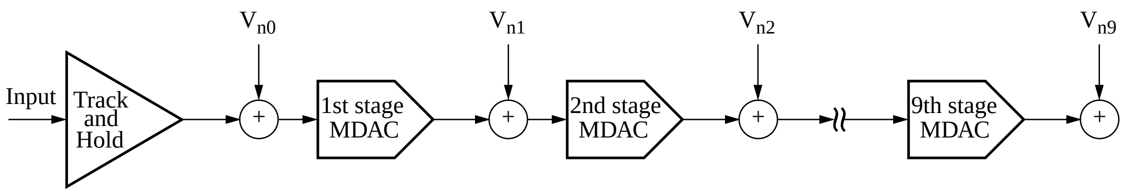

Fig. 6: Noise model of the pipelined A/D converter

Because the noise voltage is small signal, the input referred noise of the pipelined A/D converter is calculated by linearly adding the noise contribution of all stages while dividing the noise voltage of each stage by the total gain of the preceding stages [6]. The closed loop gain of each stage for a 1 bit/stage resolution is 2, therefore the total input noise power is obtained by

$$\overline{V_{input}^2} = \overline{V_{n0}^2} + \frac{\overline{V_{n1}^2}}{2^2} + \frac{\overline{V_{n2}^2}}{2^4} + \ldots + \frac{\overline{V_{ni}^2}}{2^{2i}} + \ldots + \frac{\overline{V_{n9}^2}}{2^{18}} \qquad V_{rms}^2 \tag{3}$$

The first term in the above equation is the thermal noise of the T&H circuit given by

$$\overline{V_{n0}^2} = \frac{KT}{C_s} \quad V_{rms}^2 \tag{4}$$

where K is Boltzmann’s constant (1.38×10^{-23} J/°K) and T is the temperature in Kelvins (300 °K at room temperature) and C_s is the sampling capacitor of the T&H circuit. The second term and the terms after that in Eq.3 represent the thermal noise of the pipelined stages.

The thermal noise of each pipelined stage is obtained by the model shown in Fig.7 where C_1 and C_2 are feedback and feedforward capacitors of the interstage switched capacitor circuit respectively and C_3 represents the equivalent total gate capacitor of the opamp input transistor. For a stage gain of two, C_1 and C_2 should have the same size.

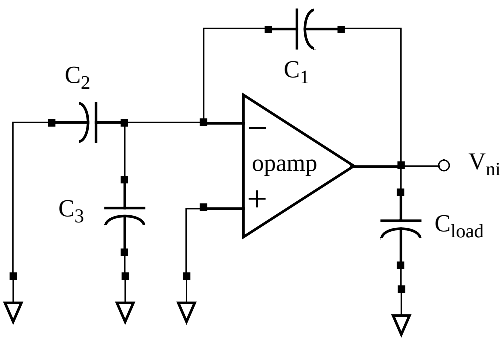

Fig. 7: Closed loop configuration of the interstage amplifying-by-two circuit

To calculate the output noise power of the opamp, the noise bandwidth should be obtained from the transfer function of the two-stage opamp which is

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{eq}}\right)} \tag{5}$$

where ω_{p1} and ω_{eq} are the two real poles of the opamp. The transfer function of the closed-loop configuration in the switched capacitor feedback network is given by

$$A_{cl}(s) = \frac{A(s)}{1 + \beta(A(s))} \tag{6}$$

and the equivalent noise bandwidth is

$$B = \int_0^{\infty} \left|A_{cl}(jf)\right|^2 df = \frac{\pi}{2}\frac{f_u}{\beta} \tag{7}$$

where f_u is the unity-gain bandwidth of the opamp and β is the feedback factor given by

$$\beta = \left(\frac{C_1 + C_2 + C_3}{C_1}\right)^{-1} \tag{8}$$

Because the noise contribution of the second stage of the opamp is negligible in a two-stage configuration when transferred to the input of the opamp due to being divided by the gain of the preceding stage, the total noise contribution of the opamp is mainly determined by the differential input stage of the opamp as shown in Fig.8.

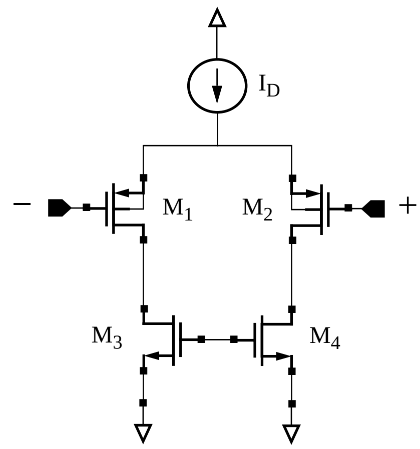

Fig. 8: Differential input stage of the opamp

The total thermal noise of each stage during the amplifying phase when the opamp is in the closed loop configuration is calculated by

$$\overline{V_{ni}^2} = \frac{1}{\beta}\frac{kT}{C_1} + \overline{V_{nop}^2} \qquad V_{rms}^2 \tag{9}$$

The first term in Eq.9 is the thermal noise due to the on-resistance of the switches and the second term is the noise power at the output of the opamp.

The single ended input referred thermal noise of the opamp is given by [3]

$$\overline{V_{neq}^2} = \left(\frac{2}{3}\right)4KT\frac{1}{g_{m1}}\left(1 + \frac{gm3}{gm1}\right) \qquad \frac{V^2_{rms}}{Hz} \tag{10}$$

where g_{m1} and g_{m3} are the input and current load transconductances of the transistors in the differential input stage of the opamp. To transfer the input referred noise of the opamp to its output node, the noise power is multiplied by the equivalent bandwidth and divided by the squared of the feedback factor as given by

$$\overline{V^2_{nop}} = \left(\frac{C_1 + C_2 + C_3}{C_1}\right)^2 \times \left(\frac{2}{3}\right) 4KT\frac{1}{g_{m1}}\left(1 + \frac{gm3}{gm1}\right) \times \frac{\pi}{2} f_u \qquad V^2{}_{rms} \tag{11}$$

Therefore the output referred thermal noise power of each pipelined stage is obtained by adding the thermal noise power of the capacitors of the interstage switched capacitor circuit and the thermal noise power of the opamp as

$$\overline{V^2_{ni}} = \left(\frac{C_1 + C_2 + C_3}{C_1}\right)\frac{kT}{C_1} + \left(\frac{C_1 + C_2 + C_3}{C_1}\right)^2 \left(\frac{2}{3}\right) 4KT\frac{1}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}}\right)\frac{\pi}{2} f_u \quad V^2_{rms} \tag{12}$$

To assure that the thermal noise of the design will not limit the resolution of the A/D converter, the total noise contribution of all cascaded stages in the pipelined A/D converter as well as the noise contribution of the stage before the last one should be less than $\frac{1}{2}LSB$.

4.3 Scaling for power reduction

The size of the feedback capacitors in the interstage switched capacitor circuit is determined by the resolution, the power budget and the speed factors. The resolution requirement indicates a minimum size limit for the feedback capacitors by the thermal noise (KT/C) constraint. On the other hand, increasing the size of the load capacitor reduces the opamp speed. This implies that the size of the load capacitors has a maximum value for a specific sampling rate. Therefore the size of the feedback capacitors can vary in a limited range (i.e. from 200fF to 1pF) for an acceptable trade-off between the speed and the resolution of the pipelined A/D converter.

Scaling is a method of reducing the power consumption of the pipelined A/D converter without reducing the sampling speed [7]. The largest amount of power in the A/D converter is dissipated by the opamps in the interstage gain blocks. To reduce the power consumption of each opamp, the biasing currents in the amplifier circuit can be reduced. This reduction will decrease the transconductance of the transistors and the unity gain frequency of the opamp. Since all cascaded stages in the pipelined A/D converter operate at the same speed, the settling time of opamps in all stages should be equal. To keep the settling time of opamps constant, the feedback factor and the unity gain frequency must be kept constant while other parameters such as the gain, the slew rate and the phase margin of the opamps in the later stages are not degraded. These conditions can be achieved if the following equation is satisfied in all pipelined stages

$$\frac{W_{(i+1)}}{W_{(i)}} = \frac{C_{1(i+1)}}{C_{1(i)}} = \frac{C_{c(i+1)}}{C_{c(i)}} = \frac{I_{D(i+1)}}{I_{D(i)}} = \alpha \quad , \alpha < 1 \tag{13}$$

where i indicates the i^{th} stage of the pipelined A/D converter, $W_{(i)}$ is the width of the differential input transistors in the opamp and $I_{D(i)}$ represents the biasing currents in the opamp. $C_{1(i)}$ and $C_{c(i)}$ are the feedback and the Miller compensation capacitors respectively. If the power dissipation of the opamp in the first stage is assumed to be p [mW], the total opamp power consumption of all stages without scaling is

$$P_{ot} = (N-1)p \tag{14}$$

where N is the number of stages. Because the last stage of the pipelined A/D converter does not generate residue signal, it does not include an opamp. For the scaling factor α, the total opamp power consumption is

$$P_{ot}' = p + \alpha p + \alpha^2 p + \ldots + \alpha^{N-2} p = \frac{1-\alpha^{N-1}}{1-\alpha} p \tag{15}$$

and the relative reduction in the total power dissipation of all opamps in the cascade stages is

$$\frac{P_{ot} - P_{ot}'}{P_{ot}} = \frac{\Delta P_{ot}}{P_{ot}} = 1 - \left(\frac{1}{N-1} \times \frac{1-\alpha^{N-1}}{1-\alpha} \right) \tag{16}$$

For example in a 10-bit A/D converter, the total opamp power consumption with the scaling factor $\alpha = 0.88$ can be reduced by 37%. Higher scaling ratios result in significant power saving [8], but the smaller the feedback capacitors and the opamp transconductance are, the larger the thermal noise is which may affect the overall resolution of the pipelined A/D converter.

As an example [9], if the opamp in the first stage has the following parameters and dissipates 5.5mW:

$$W_{(1)} = 200\mu m,\ C_{1(1)} = 400fF,\ C_{c(1)} = 1.2pF,\ I_{D(1)} = 300\mu A \tag{17}$$

Without scaling, the total power consumption of the opamps will be 50mW. With the scaling ratio of α=0.88, the opamp in the last stage will have the following parameters:

$$W_{(9)} = 64\mu m,\ C_{1(9)} = 126fF,\ C_{c(9)} = 380fF,\ I_{D(9)} = 96\mu A \tag{18}$$

and the total static power consumption of the opamps after scaling reduces to

$$\frac{\Delta P_{ot}}{P_{ot}} = 37\% \Rightarrow P_{ot}' = 31mW \tag{19}$$

5. Conclusion

The operation of the pipelined architecture, the main circuit blocks and the error sources were briefly introduced in this paper. The main focus then was how to reduce the power dissipation with respect to the models of the thermal noise and the pipelined stages. The conventional approach for this was to reduce the size of all elements in the later pipelined stages which requires redesigning the complete succeeding stages from the scratch assuming there is less power budget for these stages. To summarize the outlined in this paper for reducing the total static power dissipation in pipelined architecture, the design should start from the last stage by considering the amount of thermal noise with respect to the size of the LSB. Then the size of all critical components can be found easily by the desired scaling factor while the size of the other elements are mostly the same. These critical sizes are the width of the differential input transistors in the opamp, the biasing currents in the opamp, the feedback and the Miller compensation capacitors. Any other design approach can result in excess power dissipation or reduced accuracy with respect to an optimum design.

6. References

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