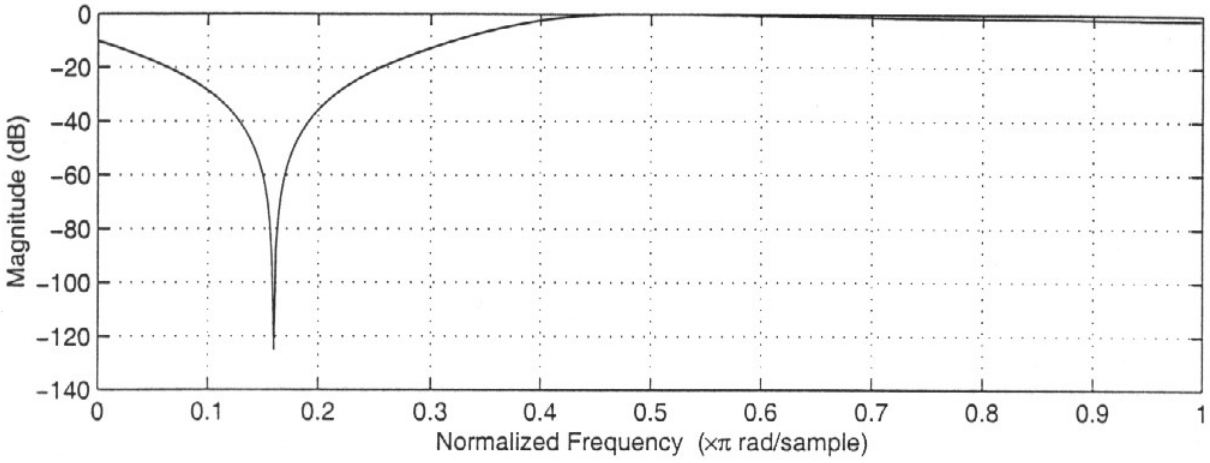
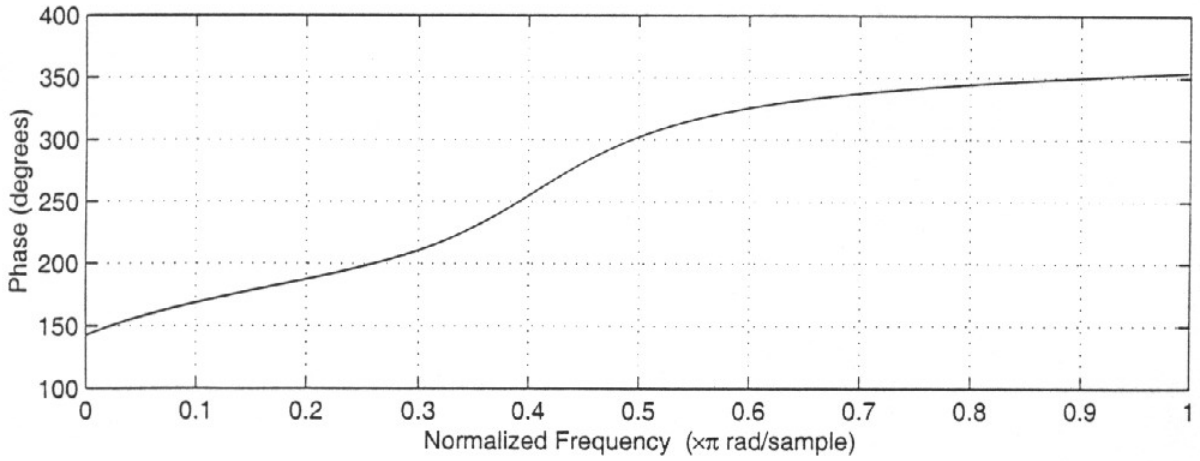
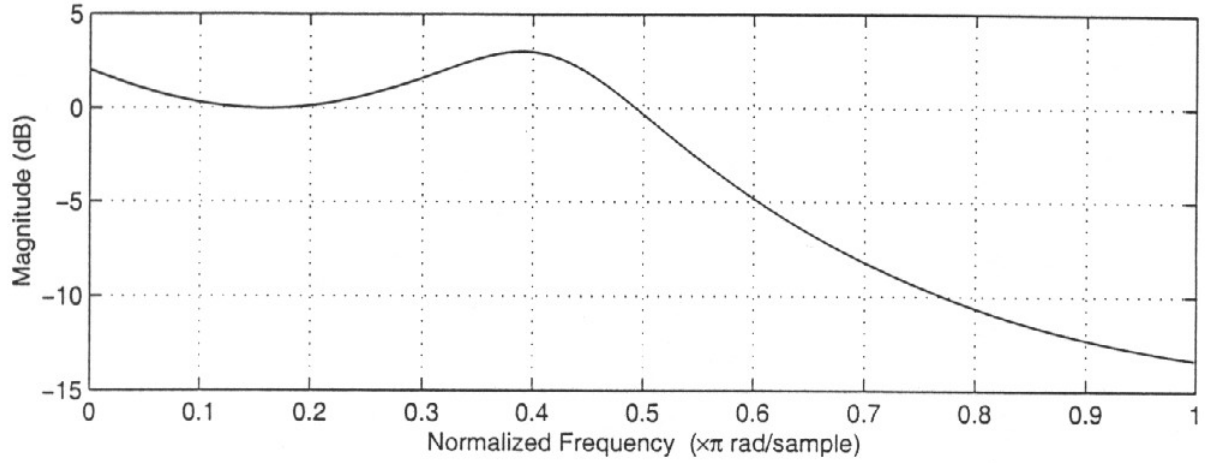
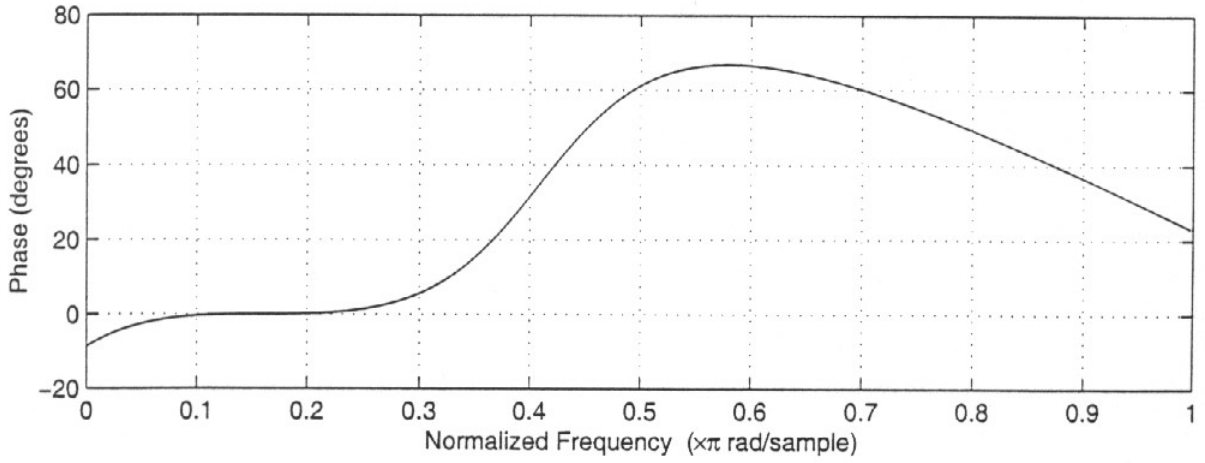
NTF Band Pass 4’th Order





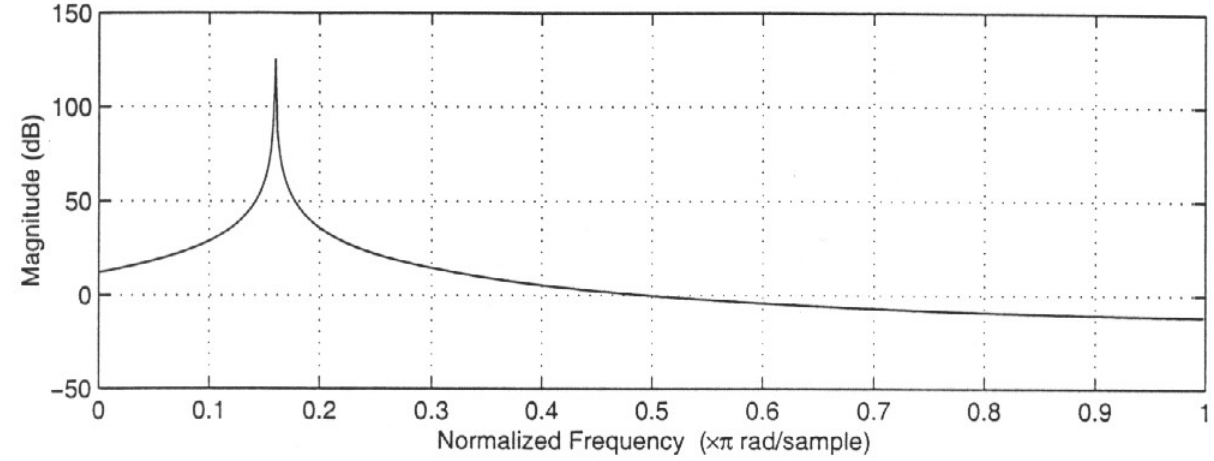
STF Band Pass 4'th Order

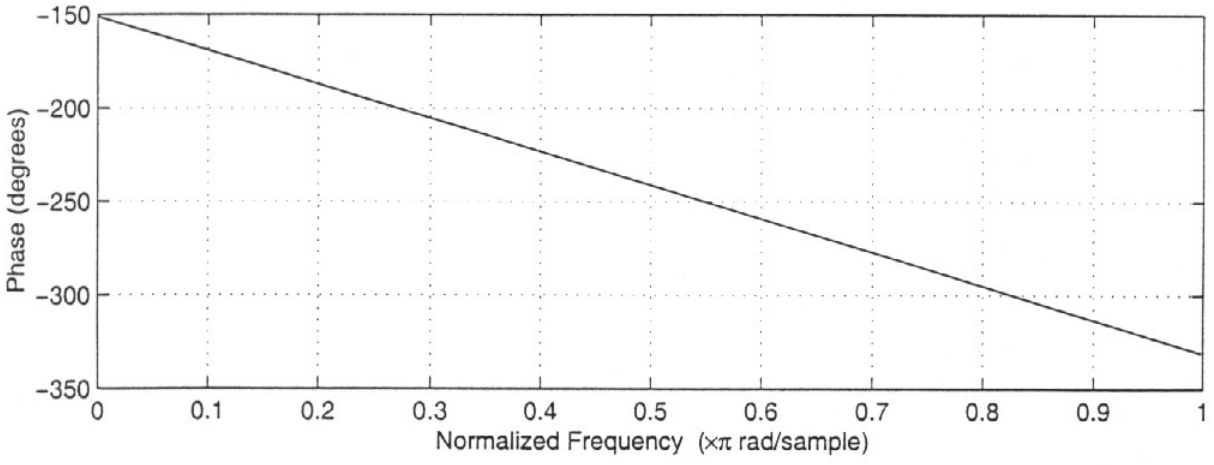




Band Pass 4’th Order

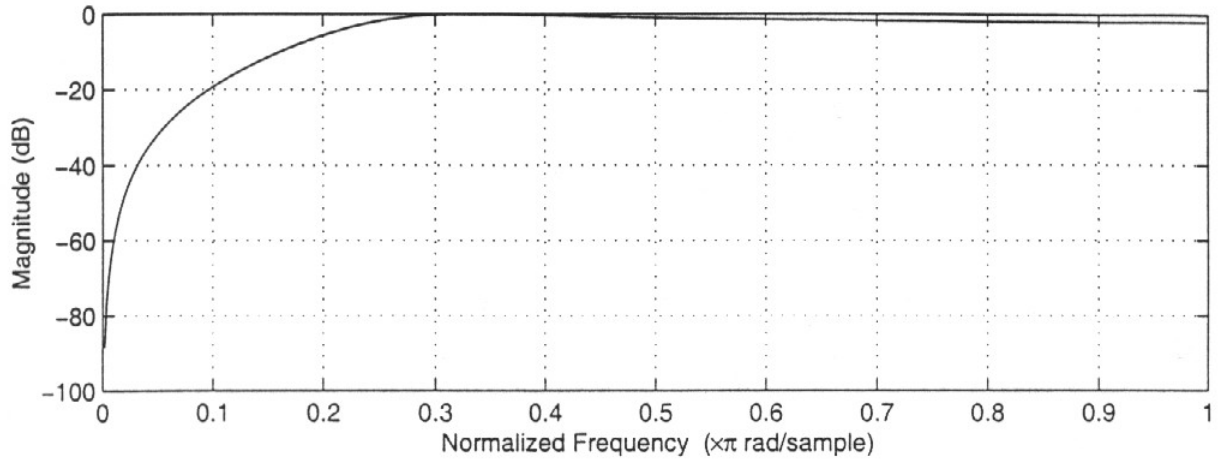
H(z)

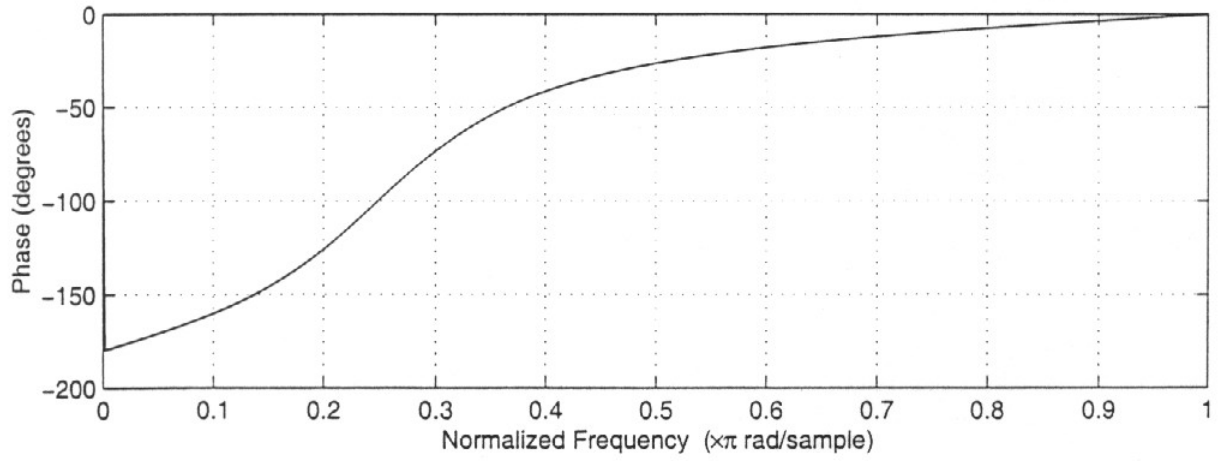




Second Order Lowpass

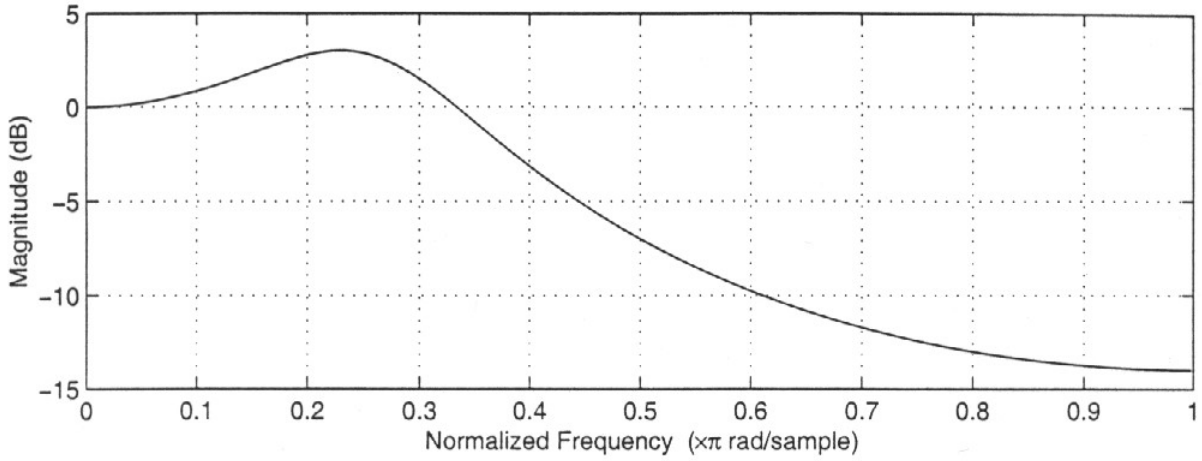
$$NTF = \frac{1}{1 + H(z)} = \frac{z^{-2} - 2z^{-1} + 1}{2z^{-2} - 2z^{-1} + 1}$$

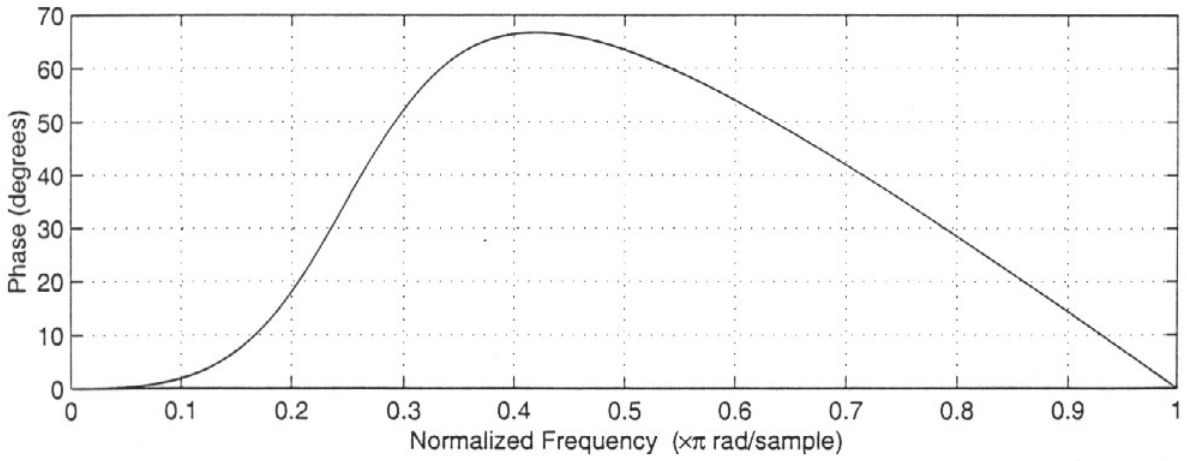




Second Order Lowpass

$$STF = \frac{H(z)}{1 + H(z)} = \frac{z^{-2}}{2z^{-2} - 2z^{-1} + 1}$$

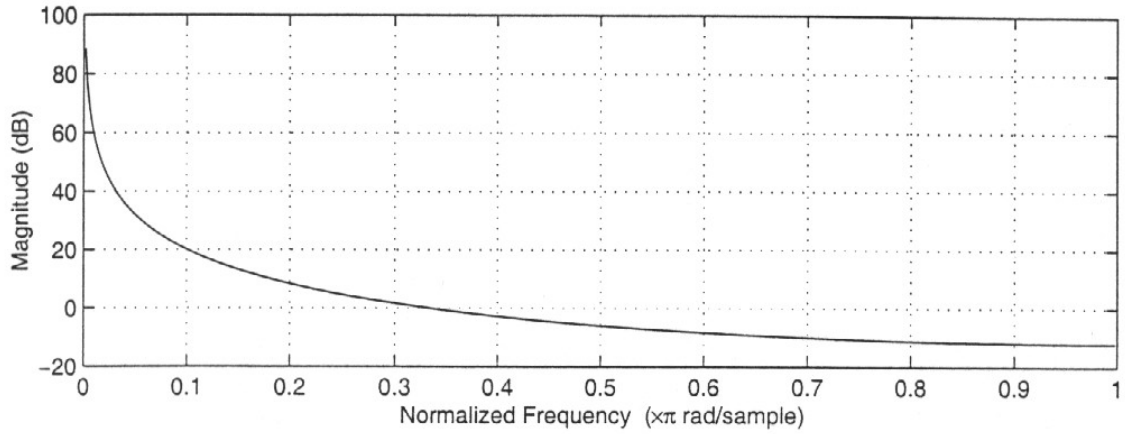


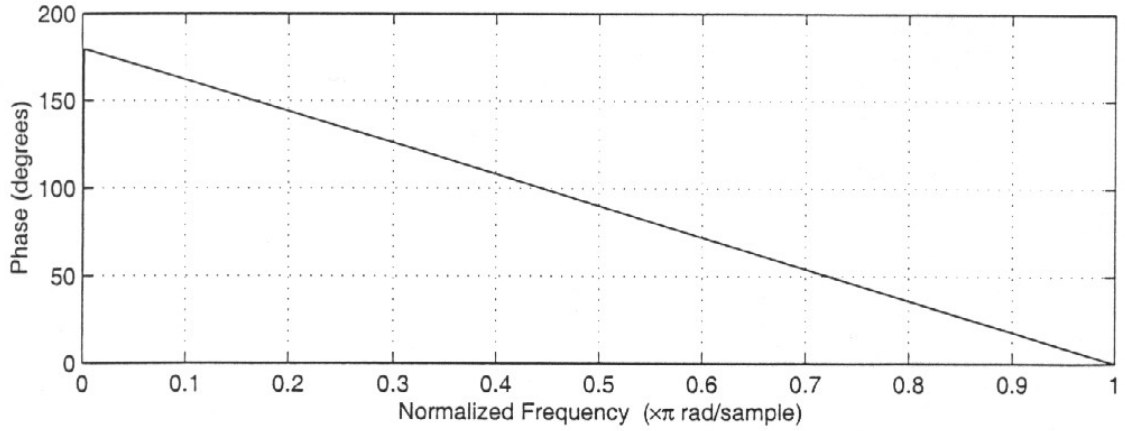


Lowpass filter

Second order

$$H(z) = \frac{z^{-2}}{z^{-2} - 2z^{-1} + 1}$$





Converter. However, in multibit Delta-Sigma modulators, improvements in process technologies and hence, less process variations will minimize the mismatch effects.

References:

[1] L.R. Carley, " A noise shaping Coder Topology for 15+ bit Converters", IEEE journal of solid state circuits, April 1989.

[2] R.W. Adams and T.W. Kwan, " Data-directed Scrambler for Multibit Noise Shaping D/ A Converters, US patent, 1995.

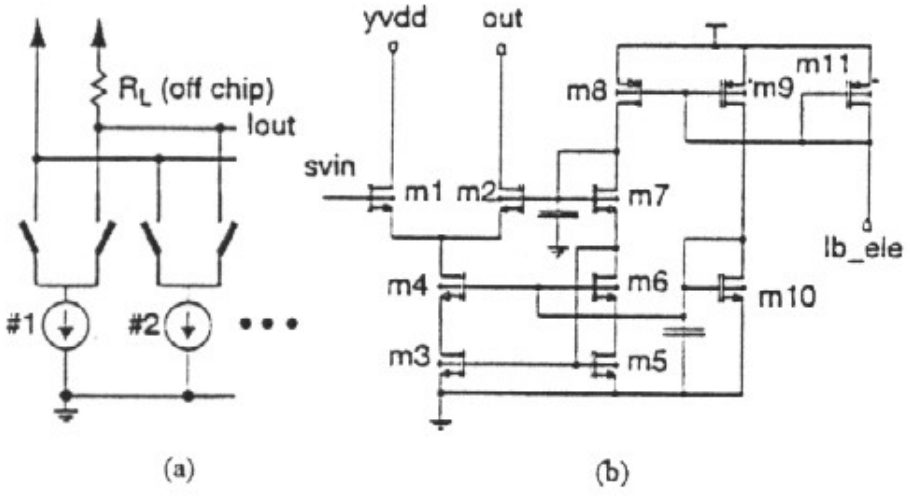
[3] H. Lin and R. Schirier, 'A Bandpass Mismatch-Shaped Multi-Bit Sigma-Delta Sweitched _Capacitor DAC ud]sing Butterfly Shuffler", ISSCC 1999.

[4] R.K. Hendersonand and O.J.A.P. Nys 'Dynamic element matchingtechniques with arbitary noise shaping function ' in Proc. 1996 IEEE

[5] S. Linfors, P. Oopik, K.Halonen,'N-path dynamic elementmatching for multibit Sigma-Delta bandpass modulators' Int .J . circuit Theory Application Sept. 1997

[6] T.Shui ,R. Scherier and F.Hudson, " Mismatch shaping for a current-mode multi bit-Delta-Sigma DAC",IEEE journal of solid state circuits, March 1999.

The reason for reusing the most recently used element is that the impulse response is {1, 1} indicating that the errors made in the last step need to be repeated. At end a current -steering DAC employing 16 nominally equal current sources is shown. Each current source includes a single ended switch driver (M1, M2), a cascode current source (M3,M4), and a local biasing network (M5,..., M11). The single ended switch driver allows adjustment of the threshold level of the input switch, thereby providing some control over on/off delay difference.The cascode transistor yields a high output impedance eliminating the noise and distortion caused by finite output impedance.The local Biasing network provides isolation between elements.

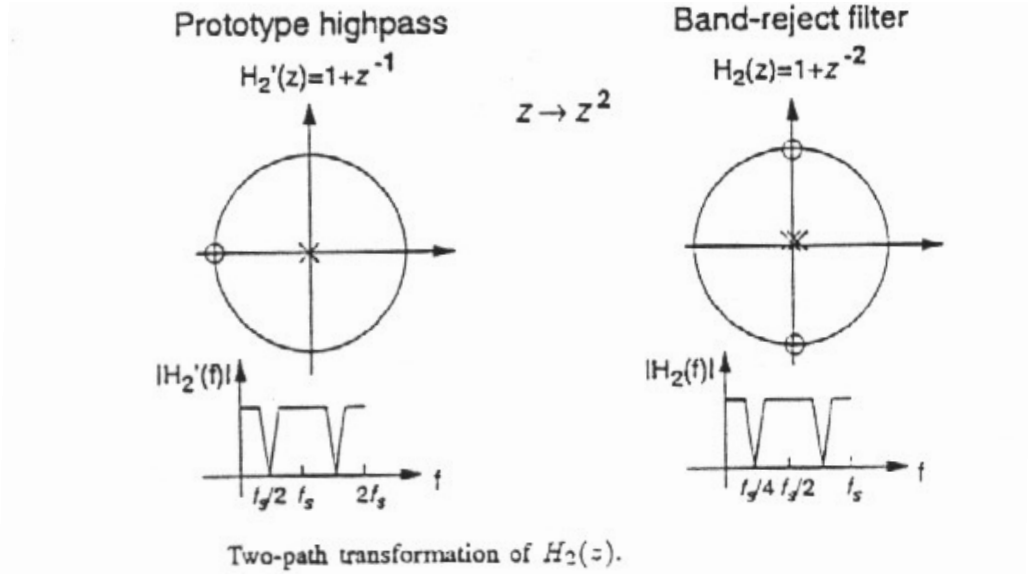


Current-mode DAC: (a) system diagram and (b) unit-element

CONCLUSIONS & FUTURE:

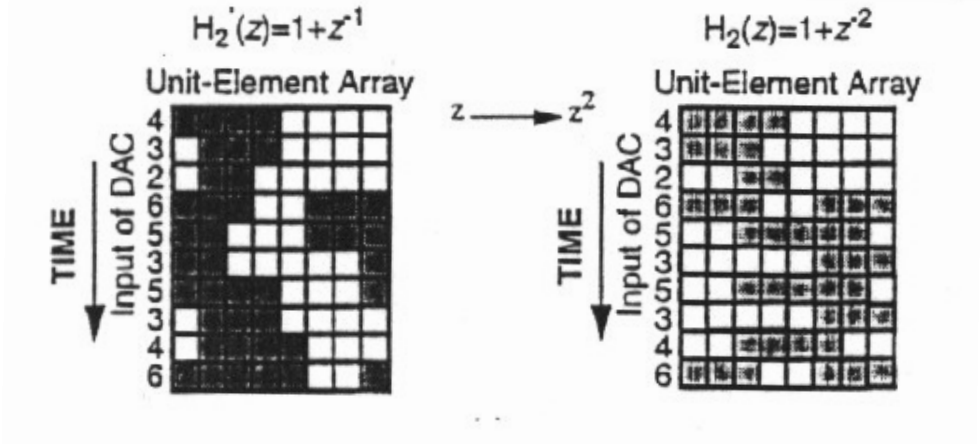
In case of Bandpass Delta-Sigma Modulation the most important thing is to choose the Quantizer one bit or multibit. If high SNR is desired we should use multibit Quantizer but in such a case that linearity is the most important factor one bit Quantizer looks better to be chosen. A key future of a 1-bit Delta-Sigma modulator is to achieve perfect linearity by virtue of its 1-bit Digital to Analog

Other unwanted zeros (at DC and fs/2) degrades the effectiveness of the mismatch shaping by 6 dB. But the best solution that we can found is to use $H(z) = 1 + z^{-2}$ but with using two $H1(z) = 1 + z^{-1}$ in parallel. $H(z) = 1 + z^{-2}$ effectively shapes the noise in the band of interest caused of mismatch error so a two path transformation $z \Rightarrow z^2$ on H'(z) will implement the desired MTF. The zeros of H(z) at z=-1 are mapped to z = +j and z = -j (providing the desired notch at fs/4.



Two-path transformation of $H_2(z)$.

Unit element array for both cases are shown next.



TF

$$H_P(z) = 1 - z^{-1}$$

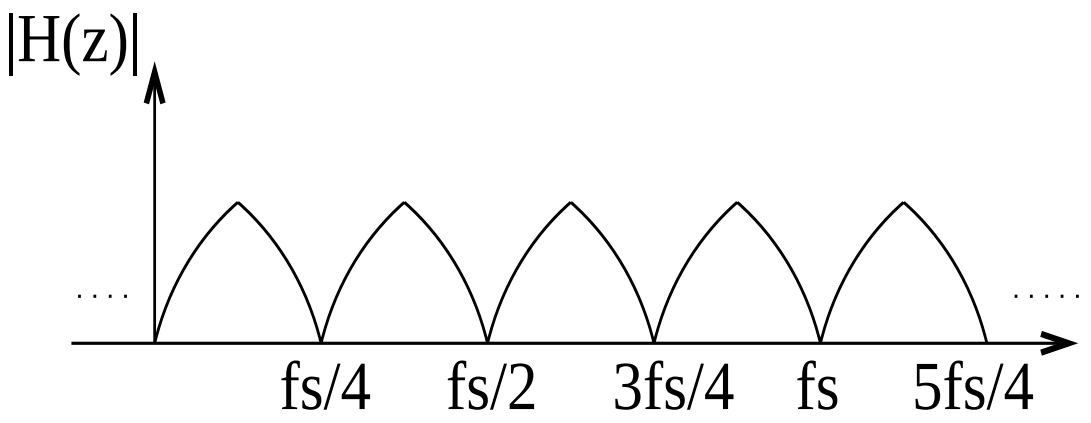
Each clock frequency equals fs/N

fs : System clock frequency .

In case of N = 4 : H(z)

This TF frequency response is shown below:

$$H(z) = 1 - z^{-4}$$

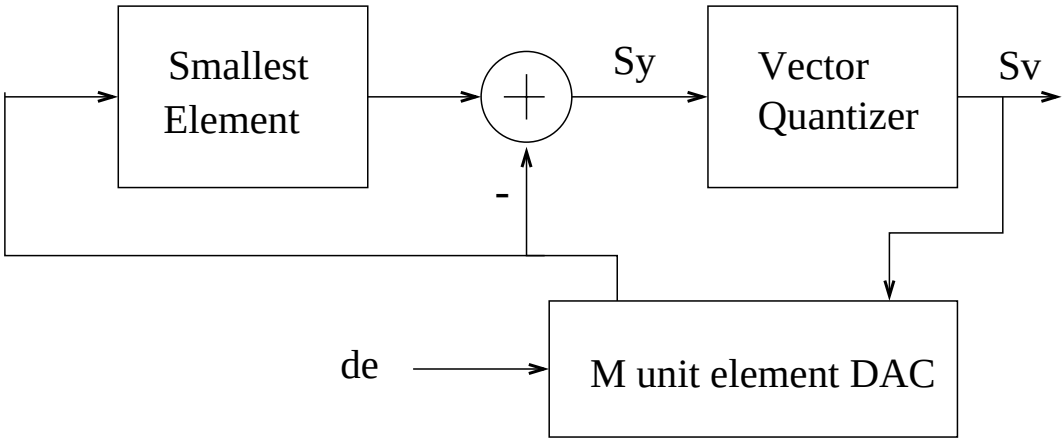


Zeros at fs/4 and 3fs/4 suppress the mismatch noise (for a bandpass center frequency of fs/4).

Again it has an important disadvantage:

The MTF has four zeros spread around the unit circle and only the two zeros at fs/4 and at 3fs/4 are useful in reducing the mismatch noise in the band of interest.

ALGORITHM Discrete time implementation of Delta=Sigma modulator are the most common, but continuous time modulators are more attractive in high speed applications. Next is block diagram of a general mismatch shaping system:



Output of a Delta-Sigma modulator produces an M+1 level signal V(n) which is fed into mismatch shaping logic block, Sv(n) has M bits each enables a particular unit element so the number of enabled elements is V(n), output of DAC:

DV(z) = K V(z) + DE(z) MTF(z)

K : average element value

DE(z): error signal introduced by element mismatch. Henderson [4] choosed $MTF = 1 + z^{-2}$ But it requires several steps in each cycle to generate the element selection bits and also a considerable amount of digital hardcover.

Laundries [5] and Hernandez [6] offered another method based upon application of N path filter principle to the element rotation scheme . Each path implements a first order highpass

It is just like a Delta-Sigma modulator box with replacing a logic block instead of normal Quantizer.

Sv = y0 - y1

Best approximation to Sy given the restriction that y0 - y1 = x0 - x1.

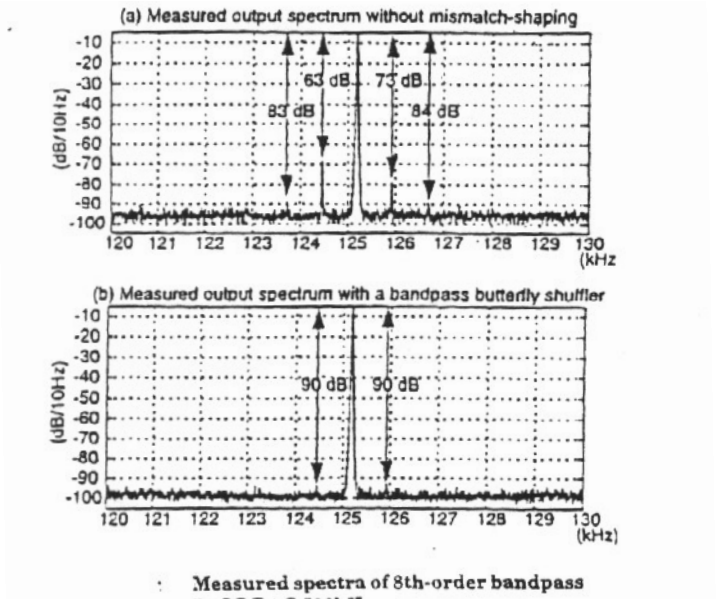
So Sy is Quantized to Sv it's Quantization error is SC (switch capacitor) is bounded

then Sv is a spectrally shape sequence.

$$Sv\,(z) = Se\,(z)\,NTF\,(z)$$

Second order mismatch shaping swapper is designed like this:

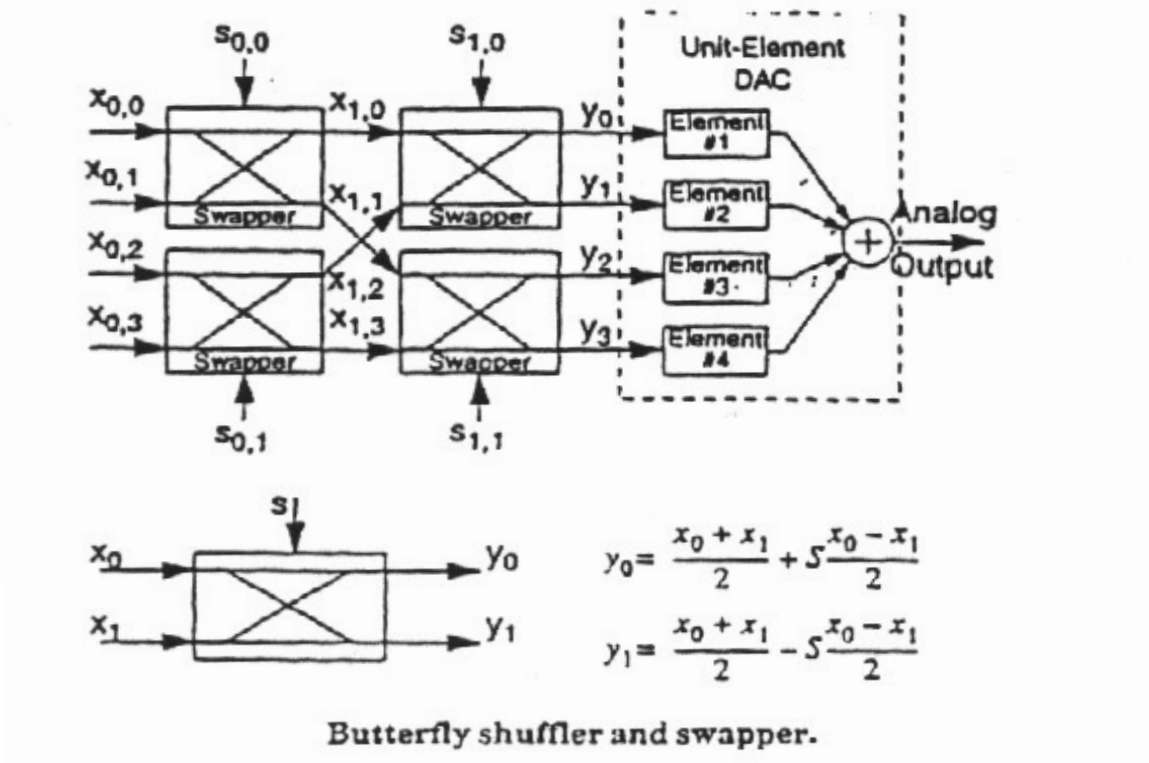
$$NTF(z) = (1 + z^{-2})$$



Measured spectra of 8th-order bandpass

Next is mismatch shaping this time for a current mode one: Dynamic error caused by frequent element switching is major source of error in a current Mode DAC with a continuous-time output. A mismatch shaping algorithm will be introduced to yield a continuous time Delta-Sigma DAC being insensitive to both element mismatch and element switching Dynamics. So Static errors and Dynamic errors will be reduced simultaneously. The ELEMENT SELECTION

We have n stages where each stage has n/2 swapper. For example a 4 element DAC is shown below:



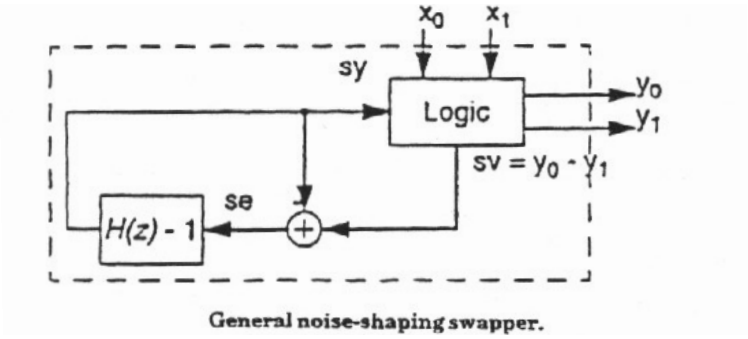
Butterfly shuffler and swapper.

Swapper cell duty:

If S = 1 THEN Y0 = X0 & Y1 = X1

If S = 0 THEN Y0 = X1 & Y1 = X0

So mismatch error term at the output is a linear combination of the differences of all swapper outputs with weighting factors that are themselves linear combination of the element error. A mis-match shaping swapper either passes X1 to Y1 and X0 to Y0 or swaps X0 to Y1 and X1 to Y0.



General noise-shaping swapper.

	I1=I+Δ	I2=I- Δ	I1+I2=2I	No errors
	□	□	□	□
2	⁕	⁕		
3	⁕		⁕	⁕
1		⁕		
4	⁕	⁕	⁕	⁕

Selecting algorithm

In last part we introduce two methods of mismatching first for the case of Switched-capacitor Delta-Sigma DAC and the second for the case of Current Mode Multibit Delta-Sigma DAC.

Butterfly Shufler is the best structure for a bandpass mismatch shaped multibit Delta-Sigma switched-capacitor DAC. Its first order has been used by [1], [2].

A second order of it is presented next by [3] 16 element switch capacitors (1.2 um technology double poly CMOS process) 8‘th order bandpass modulator Dynamic Range of 90dB at 125 KHZ center frequency .

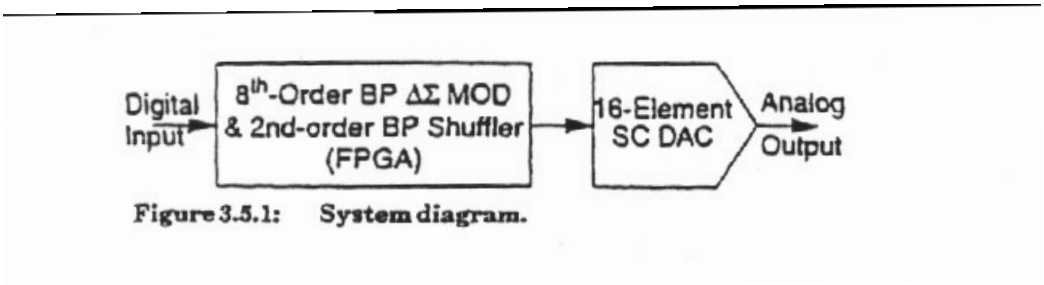
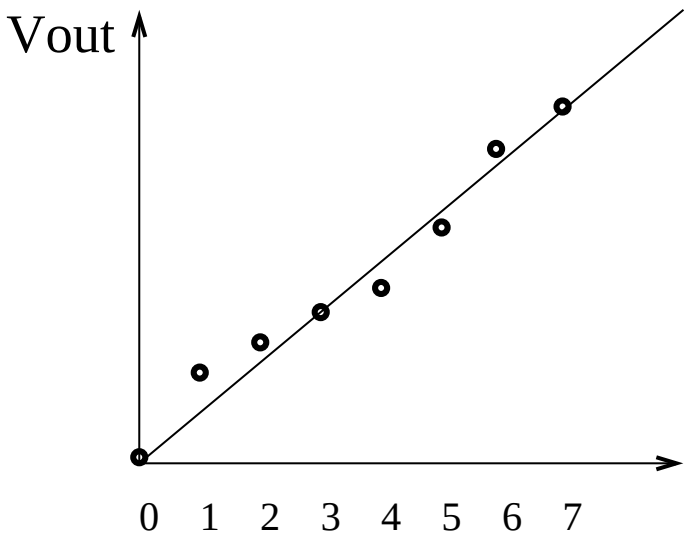


Figure 3.5.1: System diagram.



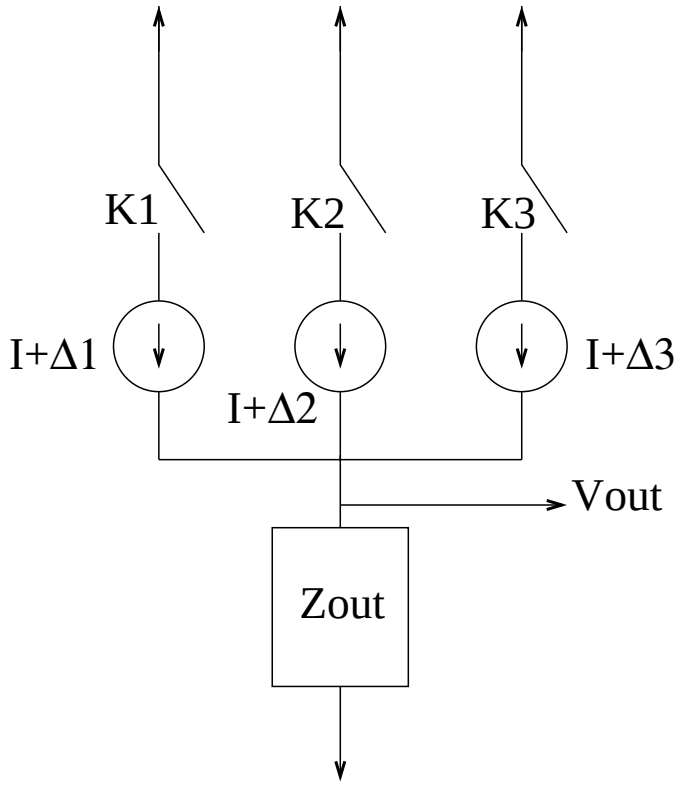
So we should find a solution and there it is:

DYNAMIC ELEMENT MATCHING (DEM).

XII. DEM Techniques for BAndpass Delta-Sigma Modulators:

Finally it is time to introduce a DEM technique to increase linearity. Mismatch observed here to be caused by elements so we have better to solve it using digital trick so we use DEM algorithm to obtain desired matching. Just as an example imagine a 2bit case, we have just four output levels again assume that each result is satisfied by a non ideal current source, using an algorithm like this may improve the linearity by cancelling error of each others:

Assume three real current source to show a 3bit DAC



K3	K2	K1	Level
On	On	On	7
On	On	Off	6
⋮	⋮	⋮	
Off	Off	Off	0

So we have 8 levels by this 3 bit DAC.

Each moment our Vout is summation of Ii and it has some errors.

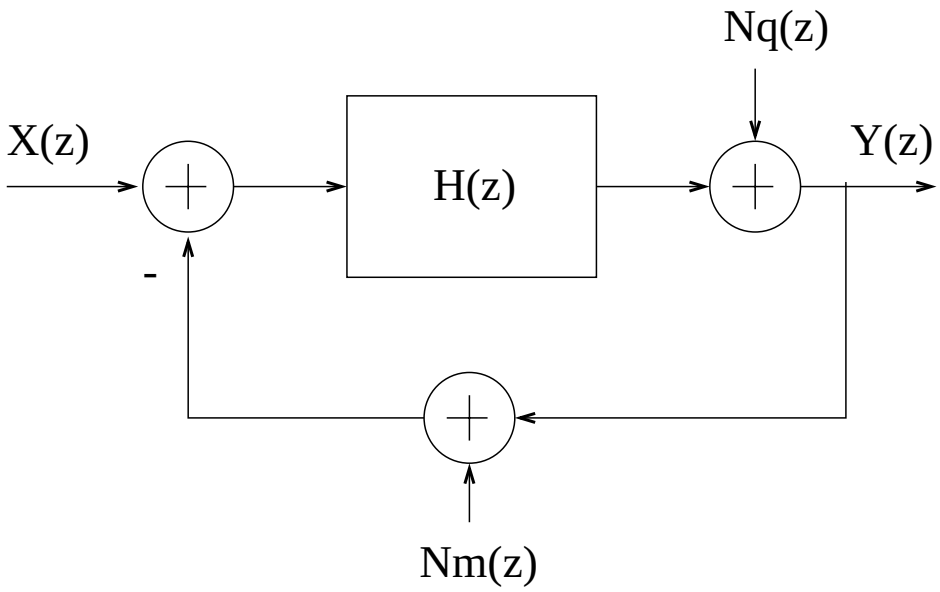
For 7'th level:

$$V_{out} = Z_{out}(3I \pm \Delta 1 \pm \Delta 2 \pm \Delta 3)$$

This will conclude a nonlinear output as shown:

So mismatch shaping can yield a highly linear DAC (Digital to Analog Converter) errors are dominated more effectively by static mismatch. However it can even increase the noise and spurs caused by nonideal dynamics.

Now we try to feel this problem and then introduce a way to care it.We simulate noise as voltage sources as shown below:



No: Quantization Noise & Nm: Mismatch Noise

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Nq(z) - \frac{H(z)}{1+H(z)}Nm(z)$$

We see considerable increasing in nonlinearity . So our goal is to improve specially the linearity of the multibit DAC.

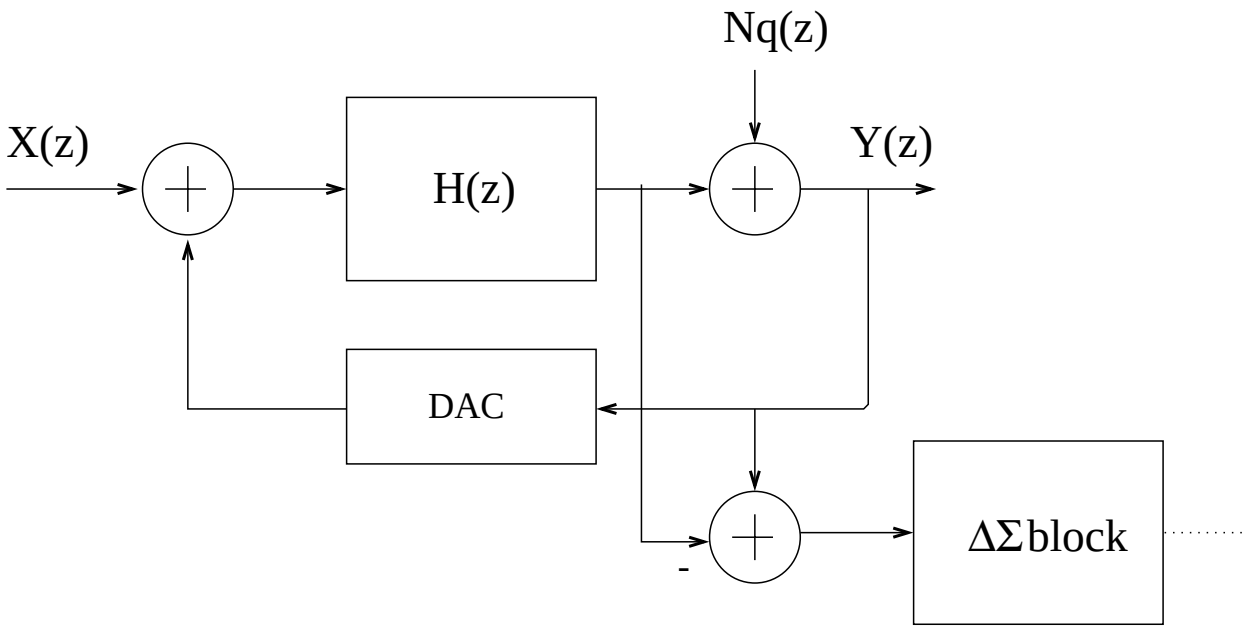
Let’s show this with a very simple example just to see its affect:

post filtering stage, reduces the sensitivity of the output to edge jitter and relaxes the slewrate requirements on the analog output stage.

XI. Mismatch caused by multibit Delta-Sigma Converters:

When we are using multibit Delta-Sigma modulator we encounter different types of mismatching. Once when your goal is simplifying the circuit as more as possible you use several Delta-Sigma boxes in your conversion process.

In this case we have MASH mismatch effect which is caused between two or more boxes of Delta-Sigma Modulators .



Another mismatching happens inside a Delta-Sigma modulation Block that it can be caused by common mode current sources or mismatching related to OPAMP gains or switch capacitors.

So we have errors of elements. A lot of researchers have tried to reduce these effectsthat we call them Dynamic Element Mismatching as more as possible .

X. Multibit Quantizer in comparison with one bit quantizer:

We discussed about one bit quantizer and its mismatch effects and a suitable way to shape this mismatch noise with introducing some circuits as switch capacitors and so on. In continue we compare multibit Quantizer with One bit.

Multibit Quantization can greatly improve the SNDR (Signal to Noise Distortion Ratio) and our goal to use Delta-Sigma Modulation is to be used as an important method
for Data Conversion. In the case of willing high SNR/SNDR and moderate signal bandwidth.

Multibit Quantization improves Delta-Sigma modulator performance by increasing he modulator resolution or increasing the modulator bandwidth while at the same time whitening the Quantization noise and improving modulator stability.

One bit Delta-Sigma modulator have been widely used in high linearity, moderate bandwidth data converters. However a multibit can not be made perfectly linear without the use of perfectly matched components. This nonidealities are equivalent to errors added
directly to the input signal .

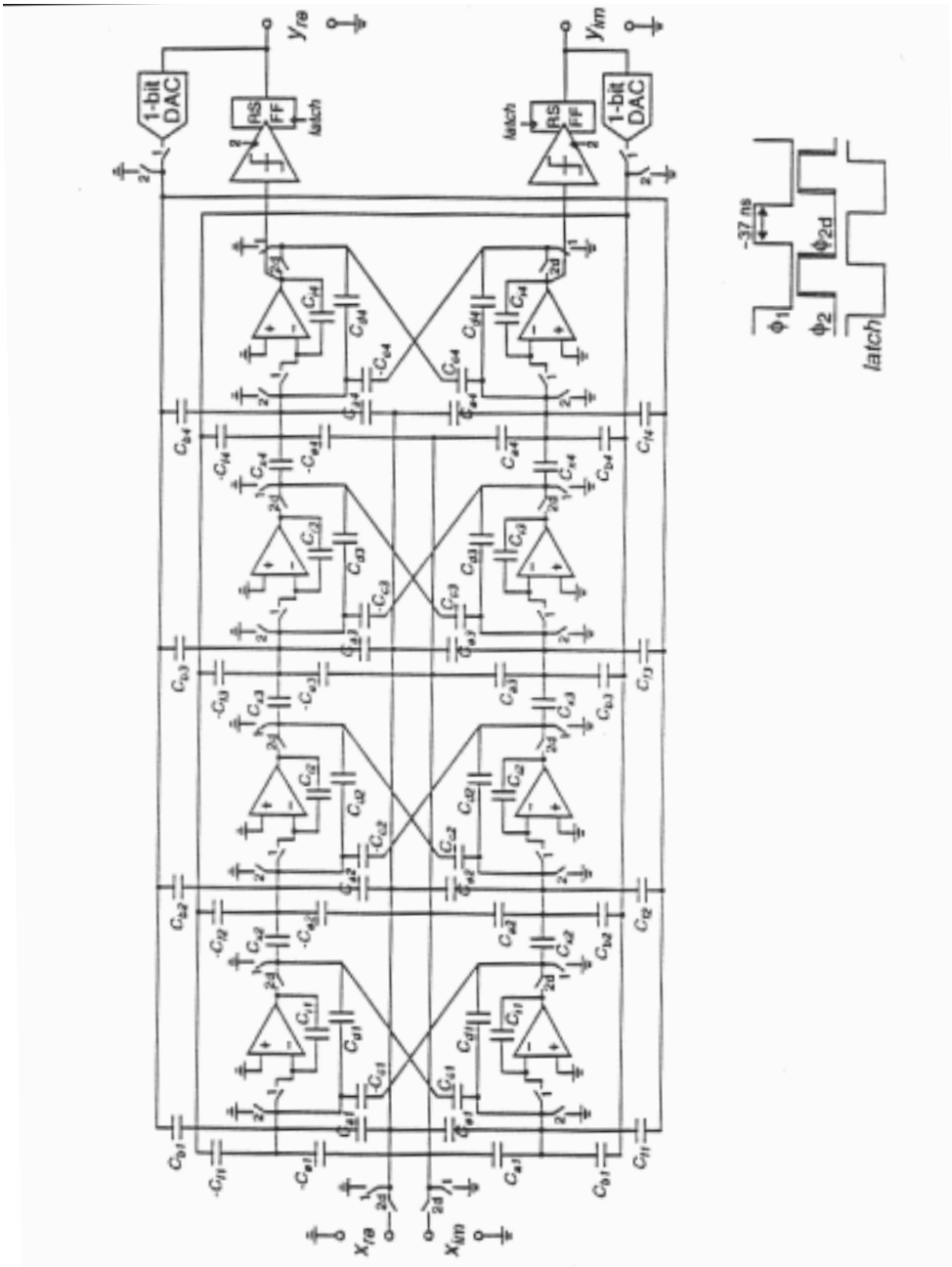
Conclusively we can say multibit Delta-Sigma converters posses two important advantages over single bit converters. The first advantage is that much higher performance is possible through the use of a more aggressive noise transfer function. Let ‘s have an example:
A fifth order binary modulator operated at an oversampling ratio of 16 can achieve SNR of at most 60 do (experienced by Richard Scherier Aug 1993), However by increasing the number of Quantization levels to eight and redesign the NTF,SNR = 108 dB can be achived with the same Modulator order and the same OSR (simulation result).

The second advantage is that the output of the modulator more closely resembles the desired output and contains much less out of band noise that eases the burden on the

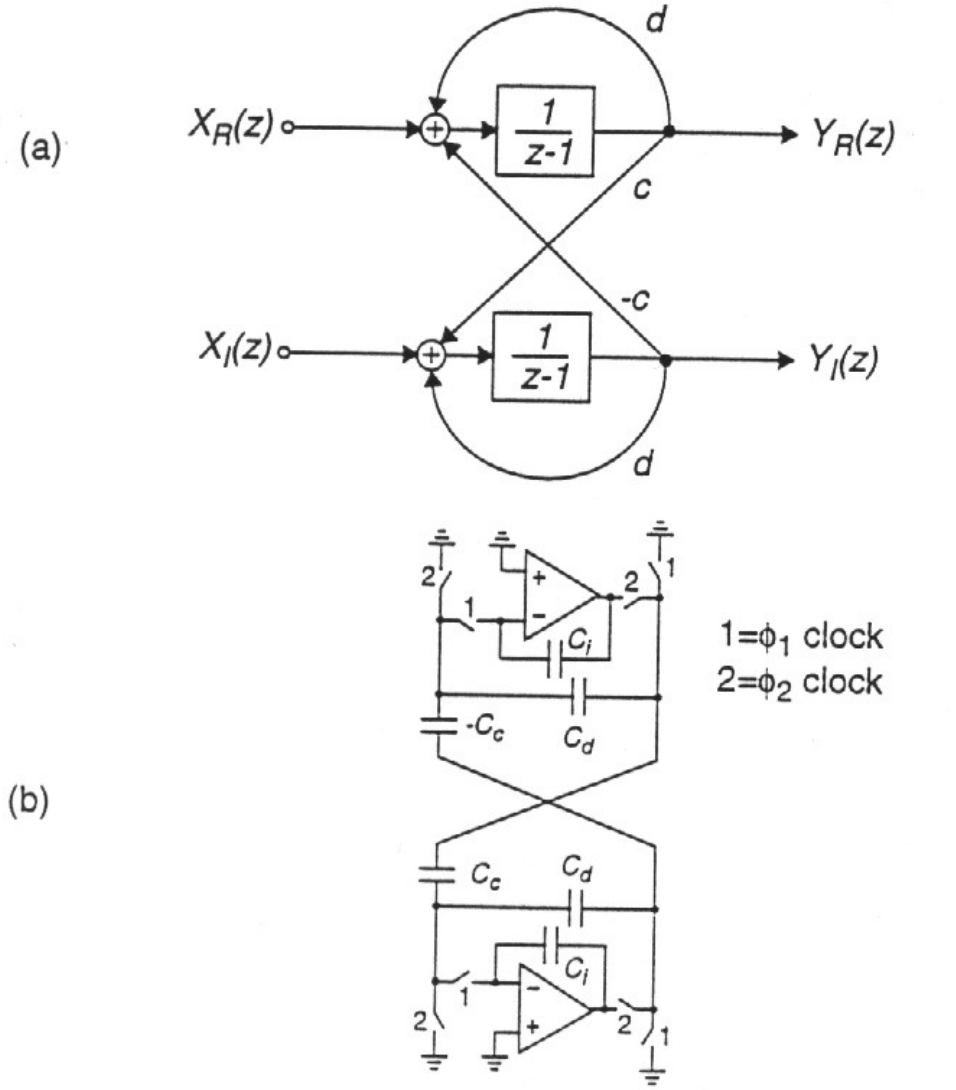
Stage Capacitor Sizes and Spreads

Parameter	Capacitor	Stage 1	Stage 2	Stage 3	Stage 4
feed-in coefficients $A = a + je$	C_a	1.719 pF	123 fF	60.8 fF	91.4 fF
	C_e	341 fF	379 fF	171 fF	—
feed-back coefficients $B = b + jf$	C_b	165 fF	176 fF	110 fF	124 fF
	C_f	60.8 fF	60.8 fF	190 fF	62.5 fF
zero-forming coefficients $p = d + jc$	C_d	2.73 pF	2.567 pF	2.742 pF	1.728 pF
	C_c	1.071 pF	1.063 pF	1.196 pF	716 fF
inter-stage capacitors	C_x	—	207 fF	488 fF	1.458 pF
integration capacitors	C_i	1.576 pF	1.503 pF	1.632 pF	1.013 pF
capacitor spreads	C_{max}/C_{min}	46	43	46	28

The negative value of each capacitor is easily realized in a fully differential implementation by reversing the connection to differential amplifier outputs. A fourth order complex modulator contains four complex integrators inside a global feedback loop.



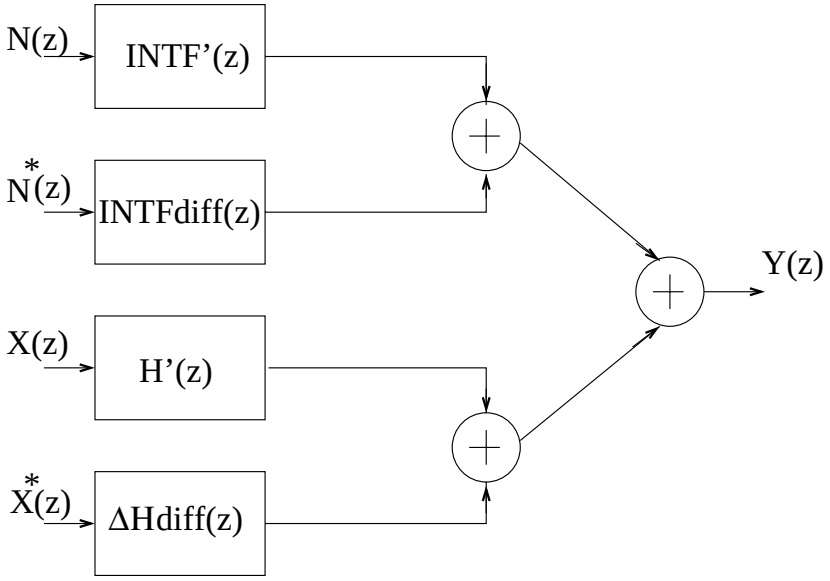
Single-ended representation of the quadrature bandpass ΔΣ modulator circuit.



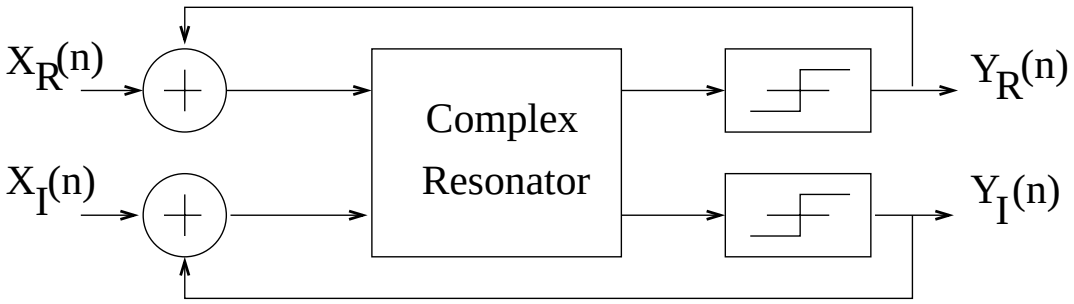
(a) Complex-integrator system. (b) Single-ended circuit realization of a z-plane complex pole.

$$C = \frac{Cc}{Ci}$$

$$d = \frac{Cd}{Ci}$$



One can improve these TF by changing poles and zeros places. Yntzi recommends a new NTF and STF. With his design SNR (Signal to Noise Ratio) is so near to the ideal one



IV. Mismatch effects on a bandpass Delta-Sigma Modulator One bit Quantizer:

Stephen Andrew Jantzi has designed a 4”th order bandpass filter with a bit quantizer, he has used Quadrates Bandpass Delta-Sigma Modulator.

NOTE: Using a modulator signal demands for a filter with a passband two times greater than the signal information band, so with multiplying two different signal one in cos(t) and the other one in sin (t) (making two vertical signals), we can send them by a common frequency named Quadrature Signals. He has shown it’s non ideal effects.

Common Mode errors similar to effects of coefficient mismatch in real filter and also Differential error, this mismatch effect is defined as a response from the conjugate input or image input to the output:

$$\Delta H_{diff}(e^{j\omega}) = \frac{Y(e^{j\omega})}{X(e^{-j\omega})}$$

Input Output transfer function with mismatch is slightly perturbed from its ideal value H’(z) insted of H(z).

$$INTF_{diff}(e^{j\omega}) = \frac{Y(e^{j\omega})}{N(e^{-j\omega})}$$

With this change $H_L(z)$ changes to $H_B(z)$ so we have:

$$z^{-1} \rightarrow z^{-1}e^{j0.16\pi}$$

$$H_B(z) = \frac{z^{-2}e^{j0.32\pi}}{z^{-2}e^{j0.32\pi} - 2z^{-1}e^{j0.16\pi} + 1}$$

$$STF_B(z) = \frac{z^{-2}e^{j0.32\pi}}{2z^{-2}e^{j0.32\pi} - 2z^{-1}e^{j0.16\pi} + 1}$$

$$NTF_B(z) = \frac{z^{-2}e^{j0.32\pi} - 2z^{-1}e^{j0.16\pi} + 1}{2z^{-2}e^{j0.32\pi} - 2z^{-1}e^{j0.16\pi} + 1}$$

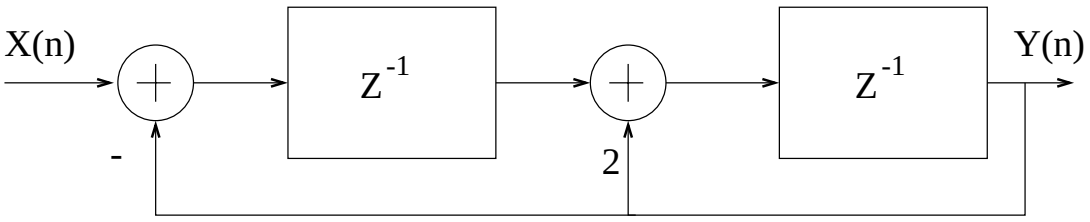
In appendix magnitude and phase degree of both cases lowpass and bandpass are shown.

Using one bit oversampling converters although caused no mismatch effects and has the advantage of high linearity, it has some disadvantages.

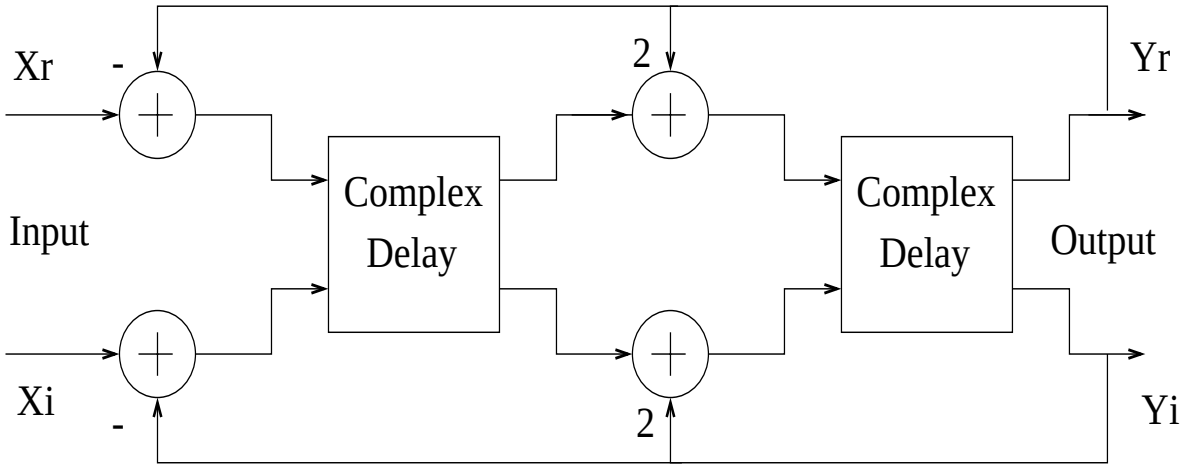
One bit oversampling modulators are prone to instability due to the high degree of nonlinearity in the feedback and also existence of idle tones .

In oversampling D/A converters , it results in a large amount out of band quantization noise so it requires higher order analog filtering . So using a multibit Quantizer reduce the large amount of quantization noise but mismatching happens there. because of nonlinearity effects .

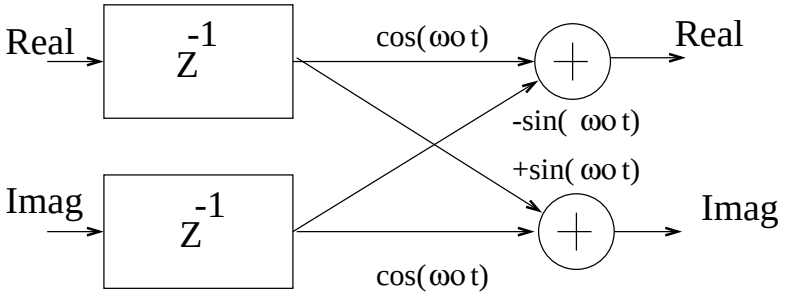
Realization:



Changing to bandpass using complex signal:



Complex delay:



$$H_L(z) = \frac{1}{(z-1)^2} = \frac{z^{-2}}{z^{-2} - 2z^{-1} + 1}$$

$$STF_L = \frac{H(z)}{1 + H(z)} = \frac{z^{-2}}{2z^{-2} - 2z^{-1} + 1}$$

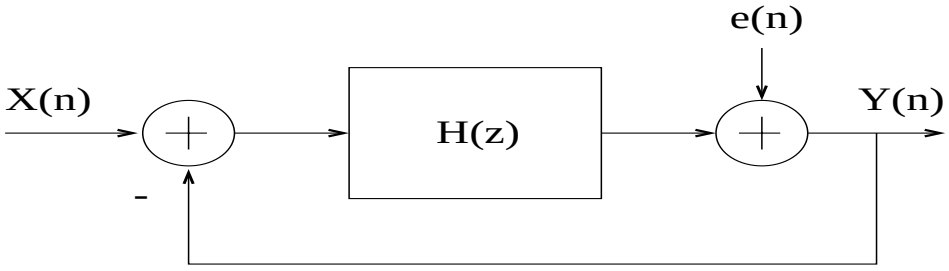
$$NTF_L = \frac{1}{1 + H(z)} = \frac{z^{-2} - 2z^{-1} + 1}{2z^{-2} - 2z^{-1} + 1}$$

$$\frac{Y(z)}{X(z)} = \frac{z^{-2}}{z^{-2} - 2z^{-1} + 1} \Rightarrow Y(z) = z^{-2}X(z) + 2z^{-1}Y(z) - Y(z)z^{-2}$$

We approximate the Quantization Noise by a noise source of e(n),so we have:

Signal Transfer Function SFT = H(z) / (1 + H(z))

Noise Transfer Function NTF = 1/ (1 + H(z))



In lowpass Delta-Sigma modulator the conversion is accurate from DC to some small fraction of the sampling rate whereas in bandpass Delta-Sigma the conversion is accurate in a narrow band, typically at a significant fraction of the sampling rate.

Here we should have the transfer function H(z) having a high gain near a frequency value of fc. With such an approach the quantization noise is small around ft. so using a narrow bandpass filter remove quantization noise.Oversampling Ratio in this case is equal to OSR = fs/f0 which f0 is the width of narrow band filter .

To obtain a high gain in H(z) near ft. (center frequency of the bandpass filter) we act similar to the lowpass case. We use a lowpass TF and shift it to bandpass.

III. Introduction a second order lowpass filter and a shifted forth order Bandpass filter:

We show a second order lowpass filter transfer it to bandpass using complex signals.

In this case fc = 0.08fs.

We assume a bit quantizer just to show the act of filter so we won't have any mismatch effects caused by multibit quantizer and that of element mismatch.

We put two poles on the zero frequency of unit circle so:

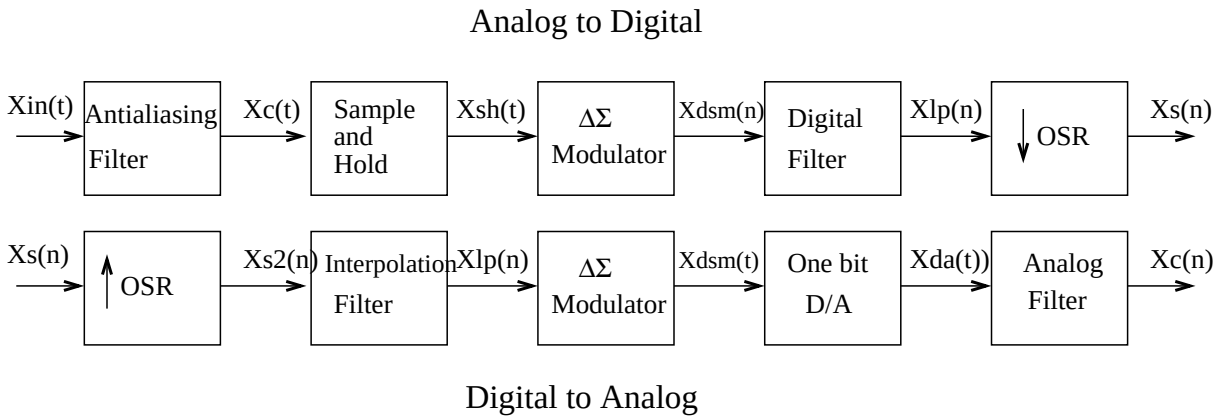


Figure 1. System block diagram

Delta-Sigma modulation is a technique for performing both A/D and D/A conversion that uses very simple analog components and digital signal processing to achieve high accuracy and an immunity to component errors.

Delta-Sigma Modulator box that we are going to focus on it contains a filter (it can be a lowpass filter or bandpass filter related to the form of input signal or desired information range) and a Quantizer.

II. WHY BANDPASS FILTER?

Sometimes we encounter signals that do not appear to easily lend themselves to oversampling approaches such as modulated radio signal.Such signals have information in only a small amount of bandwidth. We usually modulate them with a higher frequency carrier signal. In this case use of bandpass oversampling converters is clear.

Bandpass modulation is more attractive than translating the signal to baseband and applying low-pass modulation since it leads to simpler circuits and is not subject to such non-idealities as 1/f noise and mismatching in mixing process.

Abstract:

In this text we will see the importance of oversampling as well as bandpass Delta-Sigam modulation. Then we will have an introduction of a second order lowpass filter and a shifted fourth order bandpass filter.Next is Mismatch effects explained for a bit quantizer and then a complete comparison between one bit and multibit is described.Mismatch caused by multibit Delta-Sigma converters is next and finally DEM techniques for bandpass Delta-Sigma Modulators.

I. WHY OVERSAMPLING?

In digital communication systems, analog waveforms are changed to digital signals within an Analog to Digital block. In the receiver side the digital data is changed back to analog waveforms within a digital to analog block.

Nyquist sampling theory says that to obtain main signal we should sample it with Nyquist frequency of wn that is greater than the biggest frequency of original signal so if our information signal has data in a category of frequency 0 to wm our sampling frequency should be greater than 2wm (i.e. ws > 2wm). Using Nyquist frequency really needs a sharp lowpass filter that it is so expensive and complicated to build such a filter. So the use of oversampling conversion appears.

Oversampling converters relax the requirements placed on the analog circuitry at the expense of more complicated digital as well as simplifying the requirements placed on the analog anti-aliaing filter for A/D converters and smoothing filters for D/A converters. Here is a complete oversampling procedure:

Mismatch Effects on Bandpass Sigma-Delta Modulators

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