Reading Assignment

ECE1352

Optoelectronic Integrated Circuits using Porous Silicon

Shahla Honarkhah

University of Toronto

Abstract:

The need for silicon-based optoelectronic components that can be integrated into microelectronic technology has stimulated a significant development effort. Photodetectors, waveguides, wavelength demultiplexers and modulators have all been fabricated in silicon-based technology. The capability of fabricating light-emitting devices (LEDs) in silicon-based technology would greatly expand the use of silicon as an optoelectronic material. Applications where silicon-based light emitters could be utilized include data transceivers for local area network, communication, optical interconnects for high speed system integration, and low-cost high resolution displays to name a few. This paper presents an overview on LEDs that are based on nanoscale silicon. There are a number of different methods used to prepare crystalline silicon structures in the nanometric size regime, perhaps the most well-known being porous silicon formation via electrochemical anodization of crystalline structure.

1.0 Introduction

The motivation behind the effort in advancing silicon-based optoelectronics is quite clear; the ability to effectively integrate optoelectronic components and systems with microelectronics. When considering silicon as a material for optoelectronic applications, the device for which conventional silicon technology falls short is the light emitter, since crystalline silicon is an inefficient light-emitting material. Because silicon is an indirect bandgap material which leads to low optical efficiency. With a few exceptions, the active material in the fabrication of light emitting devices are usually a direct bandgap compound semiconductors, such as GaAs/AlGaAs and InGaAs/InP. Thus, direct integration of these materials with silicon electronics is extremely difficult because of major differences in materials characteristics and processing requirements.

Crystalline silicon is an indirect bandgap semiconductor with an energy gap of 1.12 eV at room temperature, which is below the visible part of the electromagnetic spectrum. Radiative recombination is only possible via absorption or emission of a phonon to maintain conservation of momentum, and this results in a long radiative lifetime (t_{rad}~10ms) and a low radiative recombination rate. Luminescence from crystalline silicon is extremely inefficient due to competition from faster nonradiative recombination events. However there have been several approaches applied in the attempt to squeeze light out of silicon.

1) Avalanche Breakdown Emission:

Bulk crystalline silicon p-n junction diodes fabricated by standard microelectronic processing techniques can emit visible light under string reverse bias, however the reported efficiency of such devices is extremely low(~10^{-6}%). Light emission is believed to be due to the recombination of electron-hole pairs generated through avalanche breakdown.

2) Hydrogenated Amorphous Silicon:

Hydrogenated amorphous silicon (a-Si:H) exhibits photoluminescence (PL) at low temperature (10-20K), however at room temperature the luminescence intensity is low and almost undetectable. The spectrum is featureless and broad with a peak at 1.3-1.4 eV. The luminescence intensity is highest when the defect density is lowest, and the generally accepted model of emission involves transitions between conduction and valance band tail states. Luminescence is quenched at higher temperatures due to the enhancement of competing non-radiative transitions.

3) Nanoscale Silicon:

Crystalline silicon structures in the nanometer size regime have shown an advantage over the bulk crystalline silicon in suppressing non-radiative recombination events. For recombination emission in silicon to yield photons in the visible range, the effective energy bandgap must increase. When the size of the silicon becomes small enough (~3nm) the bandgap widens due to quantum confinement, pushing emission into the visible region. Fig.1 shows the photoluminescence spectra for four different samples of porous silicon, normalized to the same vertical scale. By varying the preparation conditions it is possible to vary the luminescence wavelength from the infrared to the green.

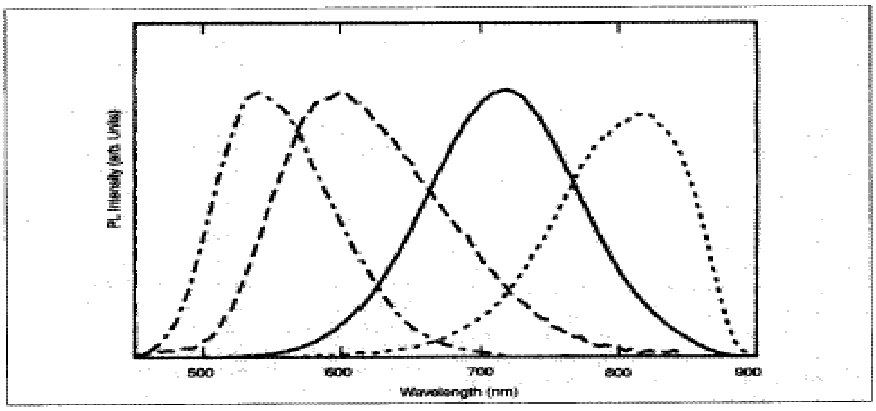


Fig.1 Photoluminescence spectrum for porous silicon

2.0 Porous Silicon Formation and Properties

Porous silicon is typically prepared by anodic electrochemical etching. A schematic diagram of an etching system for producing porous silicon is shown in Fig.2. The silicon wafer and a platinum electrode are immersed in an electrolyte which is commonly a mixture of water, ethanol and HF (a typical ratio would be 2:1:1, respectively). A current source is attached between the silicon and the Pt electrode, with the silicon and the Pt elec-

trode, with the silicon biased positively. Upon application of an appropriate current (~1-100 mA/cm^2), porous silicon is formed at the surface of the wafer. The structural, electronic and optical characteristics of porous silicon strongly depends on the fabrication conditions. The main processing parameters for porous silicon are (1) resistivity and conductivity type of the substrate, (2) concentration of HF in the electrolyte and (3) current density. Illumination during anodization also has a significant impact on the properties of the porous layer.

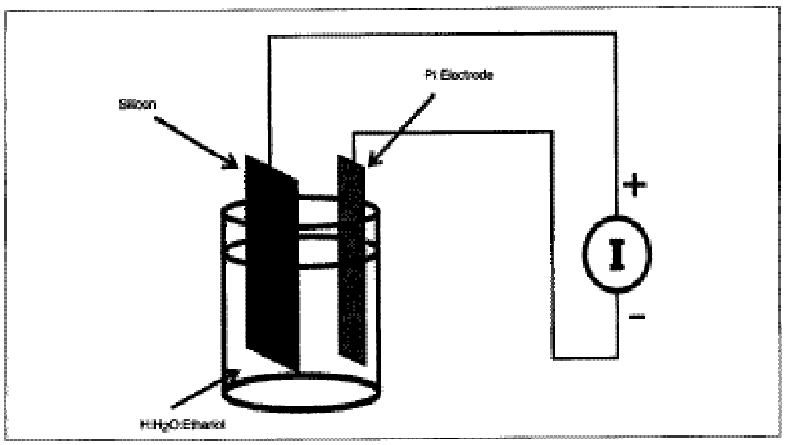


Fig. 2 Schematic diagram of an electrochemical cell for producing porous silicon

2.1 Theory:

Luminescence from porous silicon is most frequently discussed in terms of a quantum confinement model. As the characteristic size of a semiconductor is reduced to the nonometer regime, confinement of the electron and hole wavefunctions effectively increases the bandgap of the material and hence the luminescence energy. Simple particle-in-a-box estimates along with more elaborate pseudopotential and cluster calculations indicate that characteristics dimensions on the order of 1-4 nm are required to move silicon's bandgap into the visible part of the spectrum. As noted above, features with this characteristic dimension are observed in porous silicon.

Fig.3 shows the electroluminescence (EL) as well as photoluminescence (PL) spectrum which exhibits a distinctive double-band emission. By adjusting and optimizing process parameters, the EL spectra can be tuned from the silicon bandedge upward into the visible (from smaller silicon noncrystalline) or downward into the infrared. Typical EL threshold conditions of the LEDs are at an applied voltage of ~2 eV and a current density of~10 mA/ cm^2, with a maximum output light density measured to be as high as 1mW/cm^2. It is worth while to notice that, although not shown in Fig. 3, porous silicon can also emit brightly in the blue (at an applied voltage >2.5 eV) or in the infrared, between 0.8-1.3 eV. The blue PL, whose decay is fast (~1 ns) is related to recombination in OPS. The infrared PL depends on the noncrystalline bandgap.

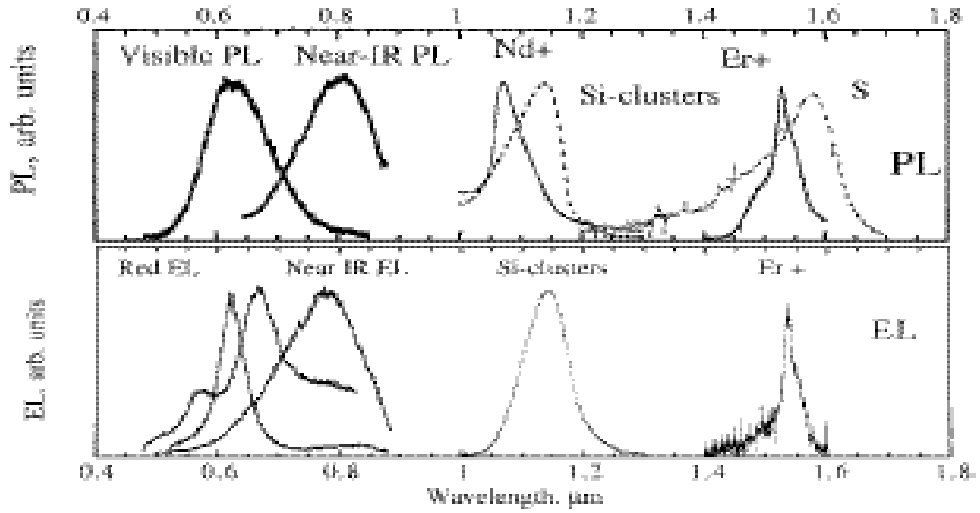


Fig. 3 Room temperature PL and EL spectra of PSi

A p-n junction diode of porous silicon exhibits a reasonably fast response as shown in Fig. 4. The frequency response of PSi LEDs are measured by modulating the applied voltage and characterizing the modulated EL. By using a thin PSi layer, the 3-dB frequency can approach 1 MHz. In the pulsed mode of operation, in which a voltage pulse is applied

to the device to produce a pulse of light, rise and fall times of the order of 100 ns have been reported.

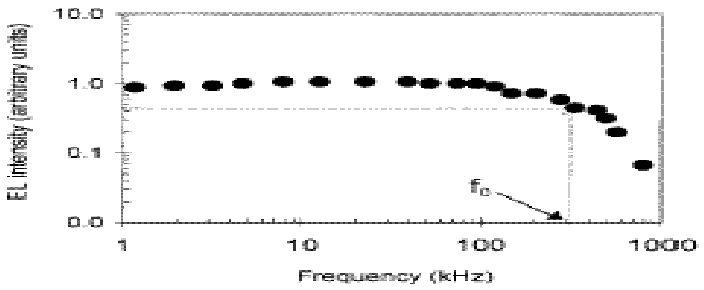


Fig. 4 EL intensity versus modulation frequency in a PSi diode

2.2 Integration with Microelectronics:

Many of the properties of nonoscale Si LEDs remain inferior to those made of other materials, such as III-V semiconductors or organics. In particular, the efficiency and modulation speed remain one order of magnitude or more below those of conventional LEDs. The major potential advantage of nonoscale Si LEDs is that in principle they can readily be integrated with silicon microelectronic circuits. The reliability and cost advantages of such a monolithic technology over those of any hybrid technology are what drives research in the field. To integrate PSi LEDs with microelectronic circuits, the size of the PSi LEDs must be very small and the anodization should not effect the Si material that is in proximity. PSi LEDs structures with sizes as small as 1 μm are feasible. Fig. 5 shows an integrated bipolar transistor and PSi LED structure. The transistor was fabricated first and then protected using Si_3N_4 prior to the fabrication of the LED. The integrated structure was fabricated using only accepted silicon microelectronic fabrication procedures, in a fabrication line environment. The device has the following specifications at room temperature: rectifying ratio of 10^5; EL peak from 1.7 to 2.0 eV; detectable light emission at an

applied voltage of ~2V and a current density of ~1 mW/cm^2 ; highest external power efficiency 0.1%; modulation bandwidth exceeding 1 MHz. The driver transistor, connected in common-emitter configuration, modulates light emission by amplifying a small base input signal and controlling the current flow through the LED.

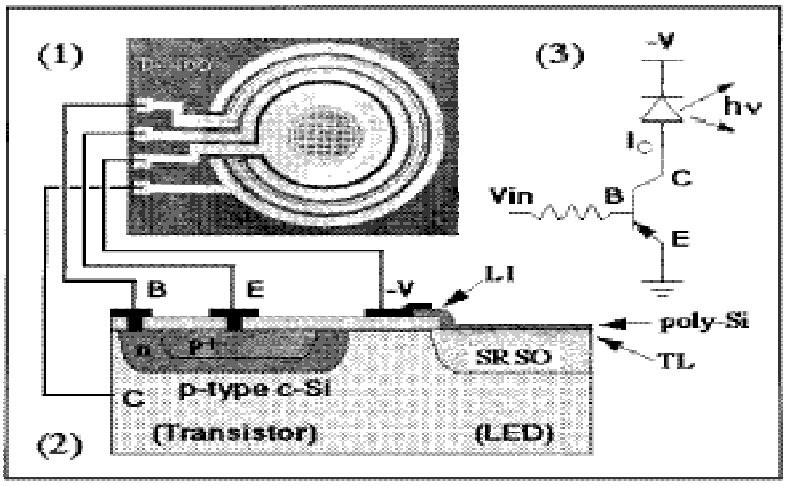


Fig. 5 Integrated bipolar transistor with PSi LED structure

3.0 The Application of Porous Silicon to Optical Wavegiuding Technology:

Porous silicon is a widely studied material which has significant potential for the realization of monolithic, all silicon, optoelectronic integrated circuits(OEIC's). In addition to complementary metal-oxide-semiconductor (CMOS) based electronic circuitry, such OEIC's may make use of silicon-based photodetectord and light sources. With the advent of high efficiency (external quantum efficiency > 0.1%) solid state electroluminescent devices based on the porous silicon, which emit at visible wavelength (λ~670nm),

and at room temperature, silicon can be used as the only material for all monolithic circuits. However to maintain monolitically, irrespective of the light source technology used, silicon based optical waveguides is required, which these enabling light from the source to be routed and split to different points, on-chip or otherwise. To qualify for use as optical waveguides, the deposited/grown layer should have a higher refractive index than the underlying porous silicon cladding layer. Single crystal silicon, for example, has a refractive index of around 3.5 in the infrared compared to the porosity dependent refractive index of porous silicon, which theoretically can vary from unity to less than 3.5. Thus, a layer of silicon deposited or grown on porous silicon can act as an optical waveguide. The most advantage of using porous silicon as a medium for the fabrication of optical waveguides covering the visible to the infrared is that, it achieves the optical losses <1 dB/cm. Although there are number of techniques during the fabrication of this layer which make possible of such a low optical loss compared to other materials in used.

4.0 Porous silicon as Semi-Insulating substrate for Optical-Sensing Devices:

(Hsieh) studied MSM (metal-semiconductor-metal) photoconductor structure that was fabricated both on porous silicon substrate and conventional silicon substrate, respectively. Experimental results show the optical current ratio can be improved up to 400% at room temperature and 3000% at 200 C operating temperature, respectively, with the porous silicon substrate. The structure of the MSM photosensor is fabricated as discussed before, by anodization method to form porous silicon layer. The resistivity of the PS layer is around 7 x 10^{7} Ω-cm. Comparing with usually used material of GaAs (10^{6}~10^{8} Ω-cm), PS is in the same range. Fig.6 gives the measured dark current of the Sic-MSM photoconductors

under 5V reverse bias as a function of operating temperature. As shown in the figure, the dark current suppressed by the PS layer up to 200 C is very significantly. As the result of the dark current suppression, the optical current gain or the ratio of photo current to dark current has been improved very much, especially at a high operating temperature. In addition Fig.7 shows the responsivity of the MSM photoconductors with 5V reverse bias, as a function of incident light wave length under room temperature and 200 C, respectively. The response is shifted from 585 nm to 740 nm as temperature raised from room temperature to 300 C for the Si substrate, but smaller shift from 595 nm to 650 nm has been found for the PS substrate. Based on the experimental results, the potential application of the PS layer as semi-insulating substrate for SiC high temperature optical sensing devices is promising.

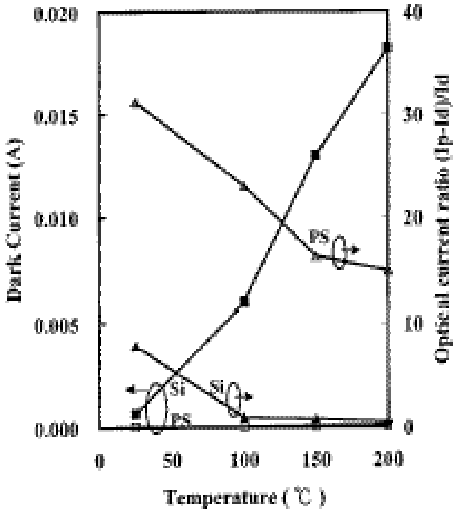


Fig.6 Dark current vs. temperature

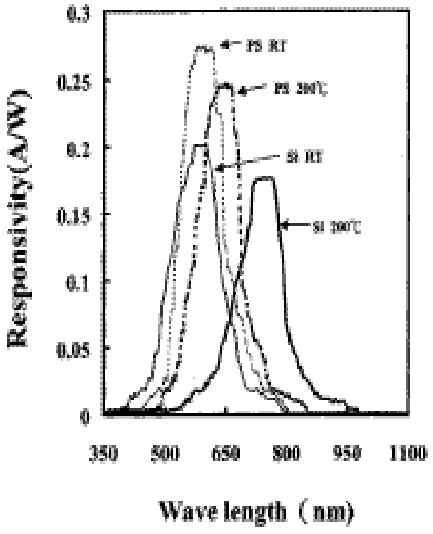


Fig. 7 responsivity of PS

5.0 Porous Silicon Technology for RF Integrated Circuit Applications:

To address the increasing demands for wireless communication systems, there is a growing demand to implement low cost microwave circuits on silicon substrates, and to integrate them with analog and digital circuits on the same chip. It is extremely challenging technologically to integrate passive RF components, especially inductors, with the main stream CMOS technology. The semi-insulating substrate offered by GaAs is expensive, fragile, and has low thermal conductivity. On the other hand, high density CMOS typically uses highly doped substrates with a thin epitaxial layer to insure latch up immunity at tight design rules. The resistivity of the substrate is of the order of 0.01 Ω-cm. The difficulty then comes from the capacitive (electrostatic) and the electromagnetic coupling between individual passive component and the low resistivity substrate typically used for suppressing latchup. The problem is particularly severe in the case of inductors, in which the capacitive coupling limits the achievable inductance and quality factor, Q of a <10nH inductor, below six, thereby greatly reducing the degree of freedom in designing suitable integrated inductors for modern silicon ICs with high f_T and f_{max}.

Two features of porous silicon make it attractive for RF applications: 1) Its resistivity could be on the order of 10^6 Ω-cm, even though the value for the starting Si wafer could be as low as 10^{-3} Ω-cm. 2) PS layers of several hundred μm thick could etched into Si wafer without any hazard to the wafer.

Welty, and Hong studied the approach of using porous silicon as substrate in RF applications. It is shown that PS reduces the capacitive coupling effect more than an order of

magnitude. Potentially PS can be used for isolation of inductors and waviguides as well as for isolation between digital and RF integrated circuits, as shown in Fig.8 .

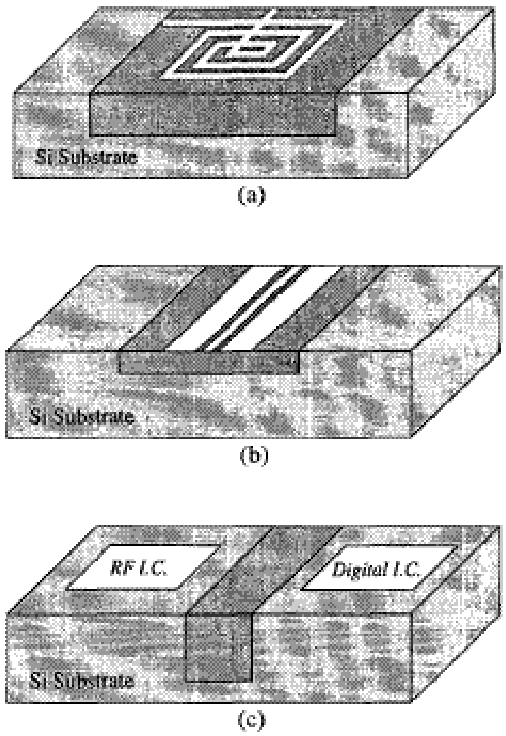


Fig.8 (a) inductor on PS. (b) coplanar wavguide on PS (c) analog and digital circuits isolated via a deep PS trench

4.1 The Spiral Inductor Fabrication and Characterization:

Porous silicon with thickness ranging from 50 to 250 μm can be formed as discussed before. After anodization, a plasma enhanced CVD SiO_2 layer of 1000 A is deposited on top of the porous silicon region, followed by a1.5 μm thick Al. A single level photo lithography is used to define spiral inductor.

Microwave measurement are shown in the Fig.9 . C_p (the capacitance to the substrate) and Q is defined as the ratio of imaginary and real parts of the input impedance. C_p and $f(Q_{peak})$ are plotted against the nominal porous layer thickness in Fig.10 . The capacitance decreases while the resonance frequency increases monotonically with increasing porous layer thickness. Such behavior indicates that the resonance frequency is still dominated by the parasitic capacitance between the inductor and the substrate. Fig.11 presents the extracted L and Q plotted vs. the frequency for an inductor with L ~ 8 nH and a maximum Q ~ 6.5 at 3 GHz. It is obvious that the value of Q is not high in general. The reason is the higher series resistance than expected. Studies are under way to find the source of the high series resistance.

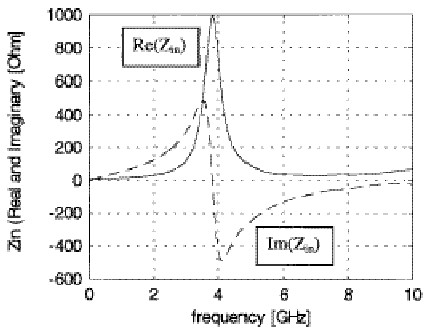


Fig. 9 The 1/Y11 raw data from PS

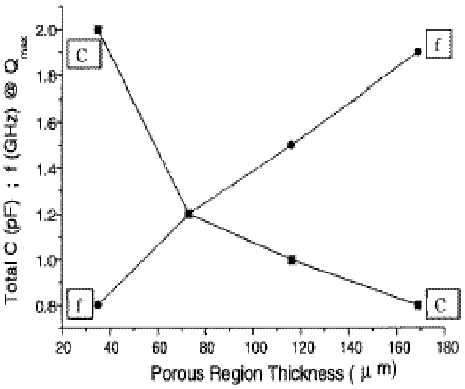
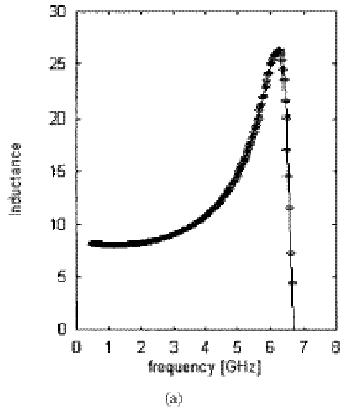


Fig. 10 Q, fpeak, and C vs. PS thickness



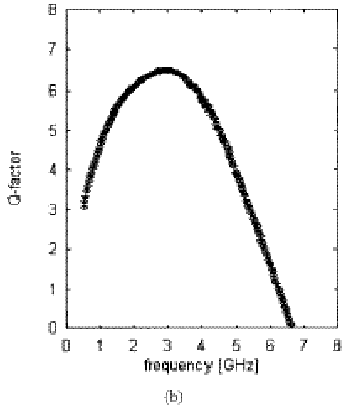


Fig. 11 Extracted L and Q vs f

Choong showed the characteristics of planar inductors on oxidized porous silicon (OPS). They have shown the modeled and measured S-parameters of 4.5-turn inductor. The inductor has an inductance value of 6.29 nH and an estimated resonant frequency of 13.8 GHz. In this design inductors on OPS with 25 μm thick SiO2 are fabricated. The results indicates that a thick oxide layer increases the resonant frequency and the quality factor in planar inductors because of the reduced parasitic resistance and low parasitic capacitance between inductor metal and the silicon substrate. Table 1 show the comparison of different implementation of spiral inductors on silicon substrate.

The measured RF performance of these inductors on PS are very comparable to those on the semi-insulating GaAs substrate. As matching or biasing elements, these inductors on PS layer can be used in applications such as 2.4-GHz communications and several giga-hertz-range satellite reception, including GPS and DBS.

Finally, porous layers can be used as coplanar transmission lines. the measured results were compared to modeled results for an infinity thick layer of porous silicon. R, L and C were calculated, and by using these values the characteristic impedance, effective dielec-tric constant and loss as a function of frequency computed.

The following table shows comparison of different implementations of spiral inductors.

L (nH)	**No. of turns**	**W / S (μm/μm)**	**self-resosnant f(GHz)**	**Qmax (GHz)**	**Fabrication technology**
9.70	9	6.5 / 6.5	2.47	3 (0.9)	1.7 μ**m SiO$_2$ layer**
6.0	6.5	15 / 5	4.4	3(1.2)	1.7 μ**m SiO$_2$ layer**
9.33	6	7 / 13	6.0	5.6(1.3)	9 μ**m**-thick polymide layer
5.10	6	12 / 4	10.3	11.5 (1.8)	multi-level interconnect
6.29	**4.5**	**5 / 5**	**13.8**	**13.3(4.6)**	**25μm-thick OPS layer**

Conclusion:

Realization of porous silicon from the silicon material with all significant characteristics suitable for optoelectronics through a very simple methods make this material interesting enough to be the center of the research of many. Porous silicon is made in a simple process of electrochemically anodization of silicon in the HF solution. Depending on the porosity of the layer the bandgap, the refractive index of that changes. Therefore it is possible to make different layers of PS with different characteristics in a simple way. The porous layer can be used in LEDs to emit visible light, which are the main block in OEICs. The PS layer used to fabricate wavegiudes, optical sensors and used in making optical packaging. There is one more aspect of using this layer, in RF applications and that is to fabricate the inductors on PS layers to increase the L and Q. Therefore silicon substrate is going to be used for all different building blocks of OEIC.

References:

Helena F. Arrand, Trevor M. Benson, Phillip Sewell, “The application of porous silicon to optical waveguideing technology” , IEEE Journal of Selected Topics in Quantum Electronics, Vol. 4, No. 6, pp. 975 November/December 1998.

Balucani, M.; Bondarenko, V.; Fazio,”Oxidised porous silicon waveguide technology for silicon optoelectronics”, IEEE Lasers and Electro-Optics Society 1999 ,Volume: 2, pp. 643, 1999.

M. L. Ciurea, V. Iancu , “ Electrical Properties of Nanocrystalline Porous Silicon”,Appl. Phys. Lett., vol57, 1046,pp.1567, 1993.

Choong-Mo Nam and Young-se Kwon, “ High performance planar inductor on thick Oxidized porous silicon sunstrate”, IEEE Microwave and guided wave letters, Vol. 7, No. 8 , pp. 236, August 1997

R.T. Collins and M.A. Tischler, “Porous Silicon Sheds a New Light on OEICs” IEEE Circuits and Devices Magazine , Volume: 9 Issue: 5 , pp.22, 1993.

Philipe M. Fauchet, “ Progress Toward Nanoscale silicon light emitters”, IEEE Journal of Selected Topics in Quantum Electronics, Vol.4 , No.6 , pp.1020, 1998

Hirschman, K.D. “Light emission from nanoscale silicon: the king of microelectronics advancing toward”, optoelectronic integrated circuits, pp. 177, 1997

W. T. Hsieh, Y. K. Fang, “Using porous silicon as semi-insulating substrate for β-SiC high temperature Optical-sensing devices”, IEEE Transaction on Electron Devices, Vol. 48, No. 2, pp. 801 february 2001.

Fauchet, P.M. “Progress toward nanoscale silicon light emitters”, Selected Topics in Quantum Electronics, IEEE Journal on , Volume: 4 Issue: 6 , pp.1020, Nov.-Dec. 1998 .

Loni, A.; Bozeat, R.J.; Krueger, M.; Berger, “ Application of porous silicon technology to optical waveguiding “, Microengineering Applications in Optoelectronics, IEE Colloquium on, pp. 8/1 , 1996

Ya-Hong Xie , M. R. Frei, A. J. Becker, “ An approach for fabricating high-performance inductors on low resistivity substrate” ,IEEE Journal of solid-state circuits, Vol.33, No.9 , pp. 1433, 1998.

Welty, R.J.; Park, S.H.; Asbeck, P.M.; Dancil, “Porous silicon technology for RF integrated circuit applications”, Silicon Monolithic Integrated Circuits in RF Systems, pp.160, 1998.