ECE1352 - Analog Electronics

Reading Assignment

High-Speed Low-Power Sense Amplifier Design

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Abstract

Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories[1]. Their performance strongly affects both memory access time, and overall memory power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These objectives are somewhat conflicting when it comes to memory sense-amp design. With increased memory capacity usually comes increased bit-line parasitic capacitance. This increased bit-line capacitance in turn slows down voltage sensing and makes bit-line voltage swings energy expensive resulting in slower more energy hungry memories

This paper examines the challenges in today’s sense-amp design, presents the limitations of the most commonly used voltage sensing amplifier and explains how these limitations are overcomed with the use of current sensing amplifiers.

Introduction

Due to their great importance in memory performance sense amplifiers have became a very large class of circuits.[2] Their main function is to sense or detect stored data from a read-selected memory cell. Figure 1 shows a typical use of a sense amplifier.

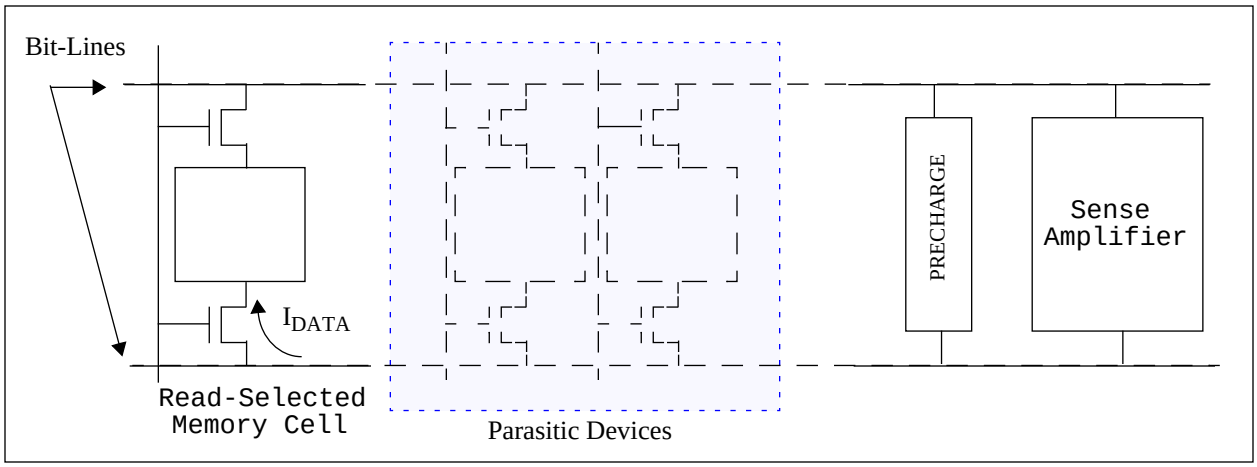

Figure 1 Typical use of a sense amplifier

The memory cell being read produces a current "I_{DATA}" that removes some of the charge(dQ) stored on the pre-charged bit-lines. Since the bit-lines are very long, and are shared by other similar cells, the parasitic resistance "R_{BL}" and capacitance "C_{BL}" are large. Thus, the resulting bit-line voltage swing (dV_{BL}) caused by the removal of "dQ" from the bit-line is very small $dV_{BL}=dQ/C_{BL}$. Sense amplifiers are used to translate this small voltage signal to a full logic signal that can be further used by digital logic.

The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Below are some of the effects of increased memory capacity and decreased supply voltage:

1) Increase in the number of memory cells per bit-line increases $C_{BL,}$ while an increase in length of the bit-line increases R_{BL}
2) Decreasing memory-cell area to integrate more memory on a single chip reduces the current I_{DATA} that is driving the now heavily loaded bit-line. This coupled with increased C_{BL} causes an even smaller voltage swing on the bit-line.
3) Decreased supply voltage results in smaller noise margins which in turn affect sense amplifier reliability.

In the next two sections two types of sense amplifiers will be presented and their ability to deal with these newly imposed operating conditions examined.

Voltage Sense Amplifiers

Voltage sense amplifiers have been known for a long time, the simplest voltage sensing amplifier being the differential couple[2]. Figure 2 shows a schematic diagram of a simple differential couple with its inputs and outputs labeled. During a read the input nodes (V_{IN}+ and V_{IN}-) would be pre-charged to VPRE causing the output nodes (V_{OUT}+ and V_{OUT}-) to stay at the same level. The read-selected cell would then be asserted and a small voltage swing would appear on the bit-lines. This small voltage swing would then be amplified by the differential couple and later used to drive digital logic.

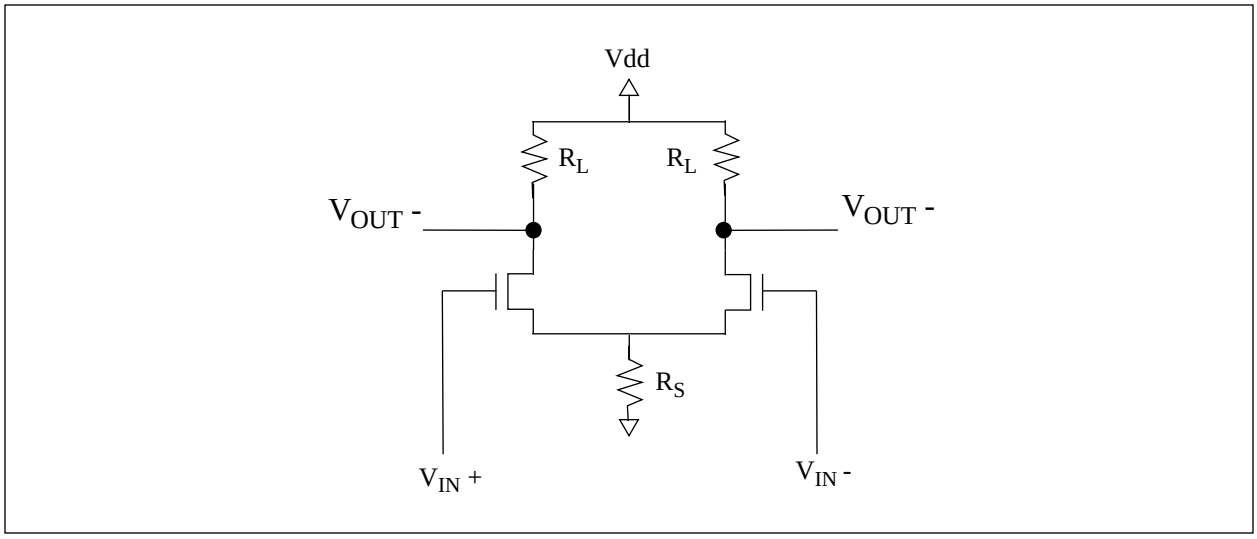

Figure 2. Differential couple

Another version of a voltage sense amplifier which has enjoyed a wide usage is the full complementary positive feedback differential sense amplifier. This voltage sense amplifier has a

very large differential gain and the added ability to automatically rewrite destructively read data[2]. Figure 2 shows the schematic diagram of the full complementary positive feedback amplifier.

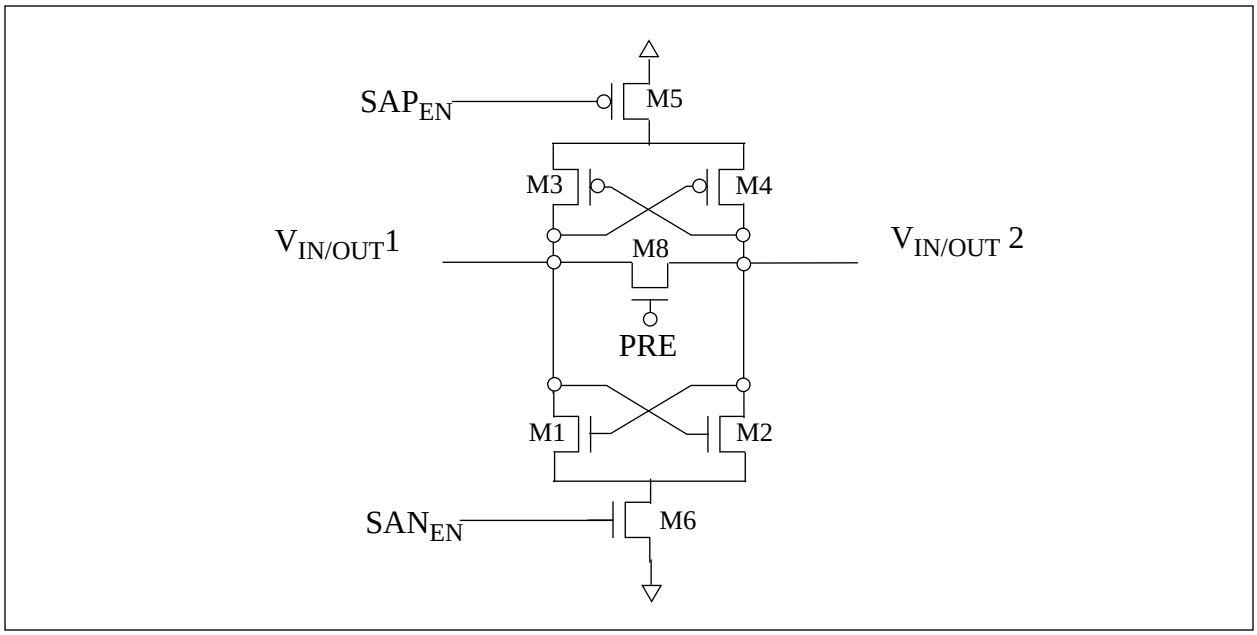

Figure 3. Positive Feedback Differential Voltage Sense Amplifier

The positive feedback amplifier has two data nodes $V_{IN/OUT}1$ and $V_{IN/OUT}1$ and three control nodes SAN_{EN}, SAP_{EN} and PRE. Nodes $V_{IN/OUT}1$ and $V_{IN/OUT}2$ act as both input and output to the sense amplifier. Its operation is as follows 1) the data nodes are equalized using PRE 2)the memory cell being read is asserted and a small voltage difference forms on nodes $V_{IN/OUT}1$ and $V_{IN/OUT}2$, 3) while MN1 and MN2 are biased to be operating in the saturation region MN6 is turned on by SAN_{EN}, 4)as both $V_{IN/OUT}1$ and $V_{IN/OUT}2$ are decreasing in voltage so is the difference between them 5) one of them decreases much faster then the other

and causes MN(1or2) to enter cutoff while the other starts operating in triode,6) at this point MP5 is turned on by SAP_{EN} which pulls the signals rapidly appart, 7) at this point since $V_{IN/OUT}1$ and $V_{IN/OUT}2$ are directly connected to the bit-lines the data is automatically written to the destructively read memory cell. Due to its positive feedback this voltage sensing amplifier achieves a very high differential gain.This high gain minimizes sensing time by being able to sense small voltage swings on the bit-line.

However, since the bit-line capacitance is growing along with memory capacity, the bit-line voltage swing is becoming smaller and more power expensive to produce. There also exists a practical limit to this decreasing voltage swing. When the bit-line voltage swing reaches the same magnitude as bit-line noise the voltage sense amplifier will become unusable. Therefore, to achieve the pre-set objectives of large memory capacity, high speed, and low power, a new type of sense amplifier is needed. The next section introduces the current-sensing amplifier which transcends the limitations of voltage sensing and meets the pre-set objectives for next generation sense amplifiers.

Current-Sensing amplifiers

The use of current sensing amplifiers has a number of benefits over voltage sensing amplifiers. The most important ones are significant reductions in bit-line voltage swing and major reductions in sensing delays[3]. These benefits translate to lower dynamic power consumption and increased sensing speed. The key to these improvements lies in the low input resistance of the current sensing amplifier. This becomes evident when examining the equivalent sensing circuit in Figure 4.

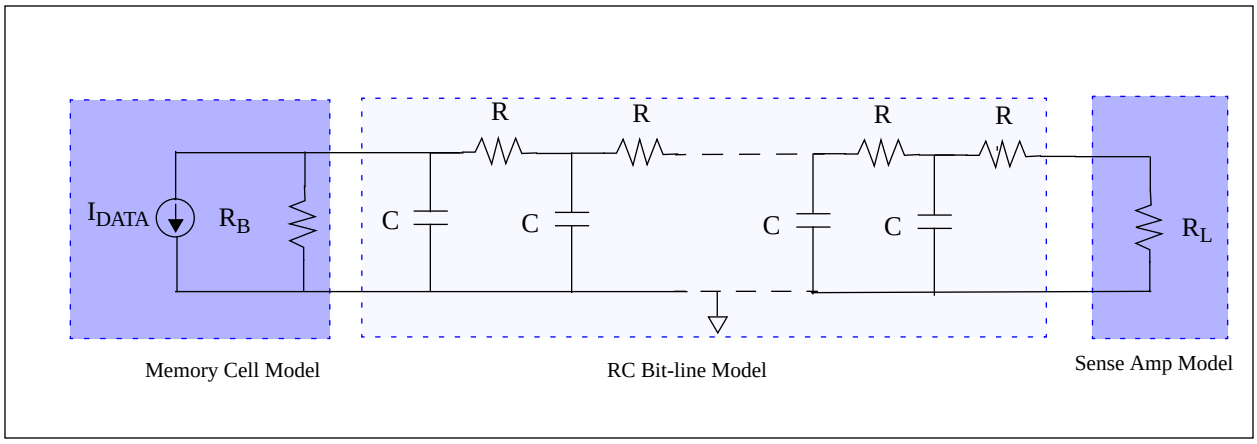

Figure 4 Equivalent sensing circuit

From the above model we can derive the delay transfer function as:

$$\delta t = \frac{(R_T \cdot C_T)}{2} \cdot \left(\frac{R_B + \frac{R_T}{3} + R_L}{R_B + R_T + R_L} \right) + R_B C_T \cdot \left(\frac{R_L}{R_B + R_T + R_L} \right)$$

where R_T and C_T are the total bit-line resistance and

capacitance[3]

Since voltage-sense amplifier has close to infinite input impedance while the current sense amplifier has a zero input impedance the above delay equation simplifies to the following two equations (a) voltage and (b) current sensing delays [2]

$$a)\quad \delta t = \frac{(R_T \cdot C_T)}{2} \cdot \left(1 + \frac{2R_B}{R_T}\right) \qquad b)\quad \delta t = \frac{(R_t \cdot C_T)}{2} \cdot \left(\frac{R_B + \frac{R_T}{3}}{R_B + R_T}\right)$$

For given parameters:

Rb=2500Ω R_T=258Ω C_T=400fF

the voltage sensing delay equals to **1ns** while the current sensing delay is **0.048ns**. This clearly shows the large speedup associated with the switch to current sensing amplifiers. The above current sensing delay equation also shows that the delay can be brought down to zero by reducing R_T. However, this is not the case and the lower limit becomes wave propagation which is on the order of pico seconds[3].

The next section examines an actual current sensing amplifier design.

Clamped Bit-line Current Sensing amplifier

A commonly used current mode sensing amplifier is the clamped bit-line sense amplifier shown in Figure 5. By clamping the voltage on the bit-line to a stable voltage (V_{REF}) the signal current produced by the cell can be transferred to an internal sense amp node without charging/discharging the large bit-line capacitance. As a result both sensing delay and dynamic power consumption are significantly decreased.

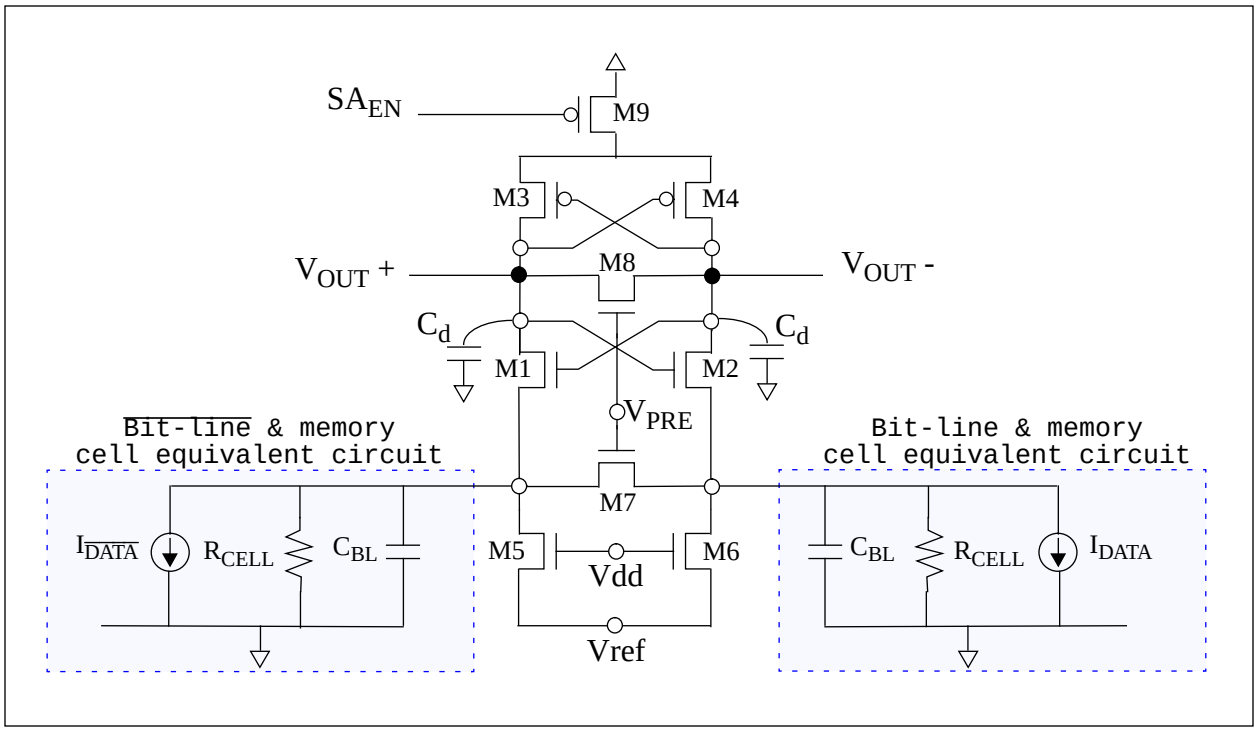

Figure 5. Clamped bit-line Current-sensing Amplifier

This sense amplifier uses three pre-charge and equalization transitors(M7,M8 and M9), two current sensing transistors (M5 and M6) and four back to back inverter configuration transistors for the voltage outputstage(M1, M2, M3, M4). Its operation

follows two stages pre-charge/equalization, and sensing. The following is the timing schedule 1) transistors M7,M8,M9 are turned on to pre-charge and equalize the sensing nodes, 2) transistors M7 and M8 are turned off and the memory cell accessed, 3) the current from the cell starts being sourced by one of the transistors M1 and M2 and a voltage difference starts forming on one of the output nodes, 4) this voltage is further amplified by the positive feedback amplifier until it reaches the latched state.

It has been shown that the time response of a latch formed by cross-coupled inverters is directly related to the AC small signal gain bandwidth (GBW) product of the inverters[3]. Maximizing GBW product maximizes the speed of the sense amplifier. By examining both small signal models for the positive feedback cross-coupled voltage sense amplifier and the clamped bit-line current sensing amplifier we can derive the following GWBs:(a) voltage sensing and (b) current sensing GWB

$$a)\ \mathrm{GBWvs} = \frac{g_m}{C_{BL}} \qquad b)\ \mathrm{GBWcs} = \frac{g_m}{C_d}$$

Since $C_d << C_{BL}$ it can be easily seen that the current mode sense amplifier enjoys a much higher speed. Another observation is that this amplifier is bit-line capacitance insensitive maintaining a constant speed over increased bit-line capacitance[3].

To recognize the power savings associated with the switch to current sensing amplifiers we need to examine the dynamic power dissipation of the voltage sensing amplifier.In voltage sensing, the bit-line are discharged and charged by dV_{BL}(close to 400mV) for every read operation. When this dV_{BL} is combined with both increasingly large bit-line capacitance C_{BL}, and read frequency "f_{read}" the energy following the below equation becomes large[4].

$$P = C_{BL} \cdot V_{BL}^2 \cdot f_{read}$$

The current sensing amplifier on the other hand has a very negligible voltage swing, thus nearly eliminating dynamic power dissipation. Furthermore, this bit-line voltage inactivity significantly decreases cross talk between bit-lines, and supply voltage drop associated with bit-line charge up[1].

Conclusion

This paper presented the sense amplifier design challenges imposed by the demand for increased capacity, higher speed, lower power CMOS memories. The most commonly used voltage sensing amplifier was analyzed, and its inability to cope with the future sense amplifier operating conditions exposed. As a replacement a current-sensing amplifier was introduced, and its ability to overcome problems associated with voltage sensing examined.

The clamped bit-line current sense amplifier shows large increase in speed, and significant decrease in dynamic power dissipation when compared to the positive feedback voltage sense amplifier. In addition, the current sensing amplifier provides a bit-line-capacitance-independent performance which is crucial to future memory capacity increases. By eliminating voltage changes on the bit-line the current sense amplifier also eliminates cross talk and voltage supply bounce.

To conclude, the current sensing amplifier outperforms the voltage sense amplifier and meets the pre-set objectives for increased capacity, high speed, low power CMOS memories.

References

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