Introduction

Field-Programmable Gate Arrays (FPGAs) have been a superb solution for rapid and reliable prototyping of digital logic systems at low cost for more than twenty years. Yet, many signal processing systems require both digital and analog circuits. To enable rapid development of analog circuits, an analog counterpart to the FPGA is essential. Nowadays, programmable analog circuits are most commonly named as Field-Programmable Analog Arrays (FPAAs) or Totally Reconfigurable Analog Circuits (TRACs), while these devices need to offer ease-of-use and flexibility features similar to those of FPGAs.

The major elements in a generic FPAA, as shown in Figure 1, include an array of configurable analog blocks (CABs), an interconnection network, and an on-chip shift register [1]. The CABs have programmable parameters to accommodate a range of user applications. The interconnection network connects signals to the CABs in a way that realizes the required application circuit. The on-chip shift register stores the configuration bits that are used to control the appropriate connections in the interconnection network.

Analog circuit design has a number of usual challenges such as linearity, noise performance, bandwidth specifications subject to process and environmental variations, and parasitic effects. Apart from these inherent challenges, the FPAAs have two additional obstacles, which are the configurable interconnection and the versatility of analog function blocks at different granularity levels. The interconnection should be designed without affecting the accuracy of the instantiated circuit, while the analog function blocks should provide a good variety of useful programmable functions. Together with the hardware development of programmable devices, CAD systems are

also developed to translate the analog circuits into a collection of configuration bits that instantiates the circuits in the programmable array.

This paper describes some of the previous work on the development of programmable analog circuits (or FPAAs in short), the current state of the art solutions that improve the accuracy and the reconfigurability, and the possible future development in this field.

Previous Development of Programmable Analog Circuits

As mentioned in the introduction of this paper, the two additional obstacles in FPAAs are the routing of the interconnection among blocks and the granularity levels of the CABs. For a given analog system, different circuit topologies can be used to implement the same function. Therefore designers of programmable analog circuits first need to determine the choice of CABs with high versatility, then to design the suitable routing and interconnection network. This section discusses the already developed approaches in CABs and interconnection network so far in the relative short history of programmable analog circuits, or FPAA.

Development of Configurable Analog Blocks (CABs)

The function and the implementation of the CABs depends on the granularity level at which the circuit blocks can be reconfigured. The granularity level may be ranged from low to high level. The lower the granularity level, the smaller and more functionally specific the CABs will be. In general, the lowest granularity level is the transistor level, while the highest is the sub-system level. Each sub-system block can be divided into

macro level blocks, which can be further divided into building blocks. Each building block is a composition of sub-circuits, which are made up of transistors. Table 1 shows the definition of analog circuits' granularity levels [2].

Table 1: Definition of granularity levels of general analog circuits.

LEVEL	GRANULARITY	DESCRIPTION	EXAMPLES
1	Transistor	Transistors	MOSFET, BJT, etc.
2	Sub-circuit	Simple circuits of specific function composed of few transistors.	Current mirror, different stage, output stage, etc.
3	Building block	Basic versatile stage for complex circuits	Opamp, transconductor, current conveyor, etc.
4	Macro block	Single versatile stage with passive elements	Integrator, Sample/Hold, etc.
5	Sub-system	Several versatile stage together	Filter biquad, VCO, ADC/DAC, etc.

From the breakdown of different block level, the building block level has become the most common choice for the CABs implementation in the development of programmable analog circuits, because this is the level with the highest versatility and that most circuit designers usually think of an analog system [2]. From the previous work on FPAA, operational amplifiers and transconductors have been two popular choices of the CABs. The choice of the CABs may affect the design of the interconnection network between them significantly. If there are many connections between CABs, the interconnection area may become huge and impractical with the presence of excessive parasitic effects. For the past few years, researchers from academies and industries have been dedicated in exploring an efficient routing and interconnecting scheme for the building blocks.

Development of Interconnection Network

The challenge of designing the interconnection network is illustrated in Figure 2. When a connection between the output of block A and the input of block B is made via the interconnection network, the corresponding wire segments and routing switches are activated by loading the configuration bits from the on-chip shift register. These routing switches are usually made use of NMOS pass transistors or CMOS transmission gates, and they will have parasitic non-linear resistance and capacitance, which will consequently affect the linearity and the frequency response of the desired analog circuit implemented. For example, a field-reconfigurable IC, primarily developed for synthesis and test of analog neutral-network architectures [3], has made use of CMOS transmission gates for the active switch elements to connect the programmable resources such as differential pairs and current mirrors.

The problem caused by the parasitic resistance of CMOS switches is illustrated in Figure 3. The On-resistance, R_{on} of the CMOS switch in the figure, causes a voltage drop in the routing of signal between the source block 1 and the load impedances of block 2. The impedances looking into the output of block 1 and block 2 are both finite and dependent on the configuration of the blocks, while the R_{on} is dependent on voltage, temperature and process variables. Therefore, the input voltage of block 2 will probably have a voltage and configuration dependent loss (see eqn.1) [4].

$$V_{in2}=V_{out1}\,[Z_{in}\,/(Z_{out}+R_{on}+Z_{in})] \qquad \text{(eqn.1)}$$

Switched-Capacitance (SC) technique has been employed to solve the switch's parasitic resistance problem by transmitting signals as charge, which is not subject to loss due to switch resistance. However, the switched-capacitance technique is a discrete-time

signaling technique that has an intrinsic disadvantage of limiting signal frequency bandwidth, because the signal frequency needs to be one order of magnitude below the clock frequency for correct operation. In general, switched-capacitance technique may be used in applications ranging from several kHz to 10MHz. Yet other approaches should be considered for applications with bandwidth of 10MHz or above. Since SC technique is a sampled-data technique that usually requires anti-aliasing and reconstruction filters. In additions, the circuit parameter programming is achieved by altering the capacitance values of the programmable capacitance arrays, which usually take up large area for implementation.

As a counterpart of the SC discrete-time approach, the transconductor approach [1] is a continuous-time approach that can be used as a programmable linear resistor, a signal controlled resistor, signal multiplier or a polarity change switch. Because of the continuous-time nature, a higher bandwidth is achievable by this technique. Figure 4a shows a MOS transconductor. This transconductor is classified as a triode transconductor because the transistors are operated in triode mode. The transconductance in the ON-state, G_{on}, is as the following:

$$G_{on} = (i_1 - i_2) / (v_1 - v_2) = \mu C_{ox} (W/L)(V_{g1} - V_{g2}) \qquad \text{(eqn.2)}$$

where the V_{g1} and V_{g2} are the control voltages and v_1, v_2 $\min[V_{g1} - V_T, V_{g2} - V_T]$. According to eqn.2, the G_{on} is directly proportional to $(V_{g1} - V_{g2})$, and the polarity of the differential current $(i_1 - i_2)$ is determined by the sign of $(V_{g1} - V_{g2})$. Also, the transconductor acts as a linear multiplier as the G_{on} varies linearly with the control voltage difference $(V_{g1} - V_{g2})$. With all the properties depicted from eqn.2, the transconductor not only acts as a switch for routing the interconnection network, but also

act as a polarity change switch, a linear variable resistor and a multiplier. This allows the transconductor to be used as an element in the programmed analog circuit instead of merely being a routing interconnection switch. Figure 4b illustrates how the MOS transconductor connects as a routing switch.

Since the transconductor switch can be used as a circuit component in the FPAA, the granularity level of the CABs should then be defined to accommodate this. With this technique, sub-circuit level CABs may be used because linear resistances are always necessary for implementing analog circuits. Sub-circuit level CABs include simple transistor level circuits that perform only one specific function such as current mirror, output stage, and differential stage. The disadvantage of the transconductor technique is the allowable voltage range being limited by the transconductor linearity, since the linearity is sensitive to the process and temperature variations.

Present State of the Art Techniques for Programmable Analog Circuit

This section of the paper discusses some of the work being done on the improvement of interconnection network, and the performance of programmable analog circuits. Alternative approaches have been recently proposed for different routing technique and different building blocks. The main objective is to achieve higher bandwidth and area efficiency while maintaining good performance accuracy.

Improvement on switch parasitic effects in routing and interconnection

In the previous section, the SC technique and the transconductor-based technique have been discussed as examples of discrete-time and continuous-time configuration approaches respectively. Each of them possesses its advantages and disadvantages. For

the most recent development of programmable analog circuits, improved techniques are desired to combine the benefits of both switched capacitor and transconductor approaches that have been mature and well understood. The new techniques for configuration and interconnection should bring the following benefits:

- Resistive voltage drop is avoided or cancelled by proper circuit design.
- The function accuracy depends on device matching.
- Signal information is carried by continuous-time voltages.

A newly proposed approach to eliminate configuration switch parasitic error is called buffered switching by Looby and Lyden [4]. Two types of buffered switch are required for signal inputs and signal outputs, which are shown in Figure 5a and 5b. As shown in Figure 5a, continuous-time voltage signals are routed using CMOS transmission gates or MOS pass transistors into high impedance MOS input nodes of the unity-gain configured amplifier. The unity-gain configured opamp maximizes linear voltage range and input impedance while its low output impedance means it is insensitive to loading. By buffered switching using opamp, the current flow in the switches will be eliminated, and the main cause of inaccuracy in the internal nodes will consequently be eliminated.

For signal outputs, a buffer is only needed for every active output. By inserting a switch in the feedback loop of a unity-gain configured opamp, output switching is provided. This is called the force-sense buffered switch as shown in Figure 5b. The resistive voltage drop of the force switch is within the feedback loop and it does not affect the overall transfer function. The sense switch allows the output to be multiplexed to several other buffers. For both input and output buffered switches, the node buffers are

necessarily designed to have excess bandwidth compared to other circuit elements to ensure that they do not limit performance.

Improvement on bandwidth specification

Since high bandwidth is always desirable in analog signal processing circuit, programmable analog circuits are no exceptions. To date, many of the published FPAA designs have limited their operating bandwidth under 1MHz. However, this bandwidth is insufficient for video applications, which normally require up to 10MHz or more. In order to increase bandwidths of FPAA, new architectures need to be developed to avoid the bandwidth limitation by the frequency response of conventional opamp based design. From recent researches, current conveyors [5] are proposed to replace the use of opamp in configurable analog building blocks.

A current conveyor, as shown in Figure 6, is a analog building block of the same granularity level as an opamp. Hence, just like opamp, it can be used to implement analog macro systems such as integrators, sample-and-hold, and amplifiers, etc. According to Figure 6, the Y node is an "infinite" impedance node with nearly no current flowing into it. If a voltage is applied at node Y, the same voltage will be obtained at node X, which behaves like a virtual short circuit. If a current is injected into node X, the same current will be obtained at node Z. The bandwidth performance can be improved when the reconfigured circuit is implemented using current conveyors, because they are operated in continuous-time basis. Current conveyors are designed to achieve high gains at high frequencies without feedback, unlike the case of using opamp with feedback. Also, current conveyors can be used to build amplifiers that achieve constant bandwidth

independent of gain. Figure 6b shows how a configurable analog block is built based on the current conveyor approach.

Other New Concepts

Last but not least, a new concept of dividing up the configurable building blocks has been proposed, which is about applying computational design methodology to analog signal processing [6]. The new concept is to use a set of operands for the available building blocks in a Totally Reconfigurable Analog Circuit (TRAC), instead of merely using one or two versatile CABs. By computation approach, analog signal processing includes six basic operations, each of which is easily built electronically. The six operands are “ADD”, “NEGATE”, “LOG”, “ANTILOG”, “DIFFERENTIATE”, and

On the other hand, the “LOG” operand is used to realize functions such as multiplication, division, and raising to a power. The mathematical derivation of these three additional operations is illustrated in Figure 7. Hence, in practice most signal processing operations can be described in a combination of any of these six basic operands, and this allows a higher level circuit description to be used in programmable analog circuit design, and even in CAD software development.

Future Work on Programmable Analog Circuits

The future development of programmable analog circuits can possibly follow a number of directions, which in general aim for improved circuit performance and accuracy, improved supporting software design tools, and increased levels of integration.

Researches will definitely continue in the investigation of routing and interconnection techniques, which eliminate errors effectively. Easy-to-use CAD tools should be necessary for designers to optimize the performance of the circuit embedding. Because a programmable analog IC essentially contains large amounts of digital control circuitry, improvements in digital density can free up silicon area for more and more analog circuitry. In additions, most analog systems usually interface with digital systems, so that mixed-signal programmable circuit will very likely be brought up and incorporated into the development of programmable analog circuit in the future [7].

Conclusion

Programmable analog circuits offer an efficient way to improve the turnaround time for analog circuit design. Field-Programmable Analog Arrays (FPAAs) and Totally Reconfigurable Analog Circuits (TRACs) have widely been accepted commercially. A FPAA basically contains three major components: Configurable Analog Blocks (CABs), interconnection network, and on-chip shift register. Operational amplifiers and transconductors have been two popular choices of CABs for the FPAAs available nowadays. Discrete-time and continuous-time techniques have been proposed for the interconnection between CABs, and the examples are the switched-capacitor technique and the MOS transconductor technique respectively. More recent improvements have been published on the design of the CABs and the routing switches. Current conveyors seem to be a favorable replacement of operational amplifiers according to recent investigations. Computational methodology has also been used to define the programmable building blocks from the perspective of signal processing. It can be

foreseen that the demand of programmable analog circuits will continue to rise in the future, while more advanced techniques for improvements of bandwidth and accuracy will continue to be investigated.

Figures references

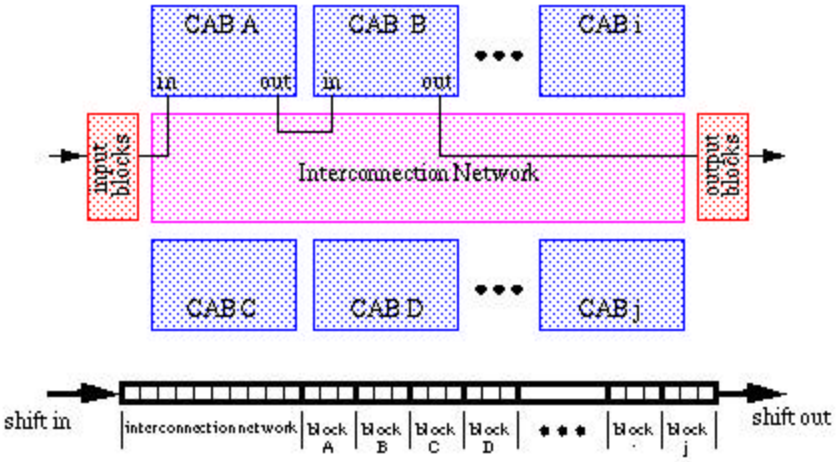


Figure 1: A outline of the components in a generic FPAA

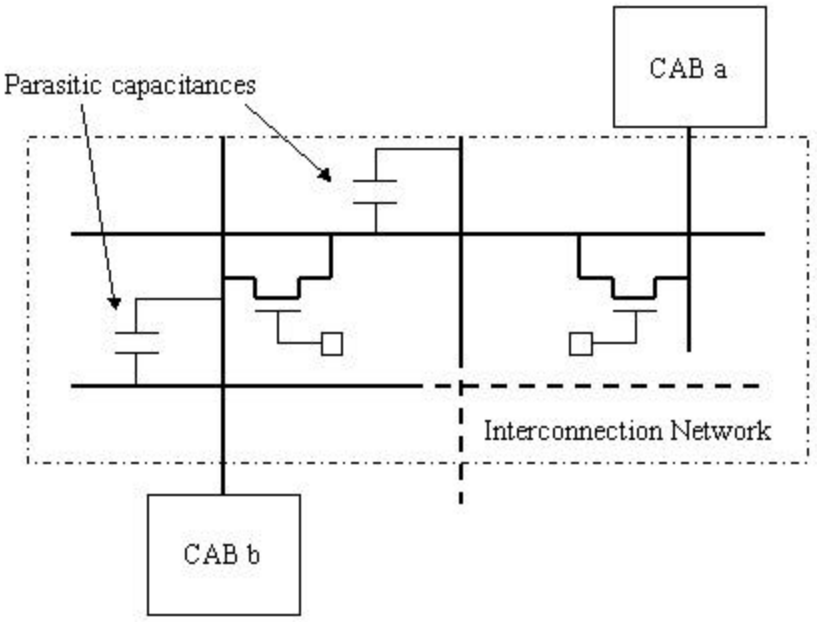


Figure 2: Parasitic effects due to the interconnection switches

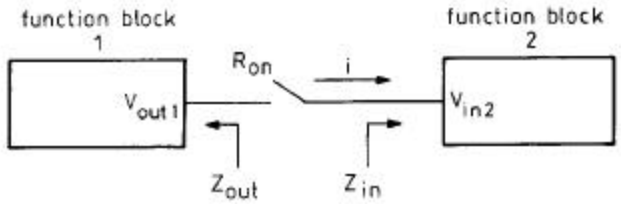


Figure 3: Illustration of the interconnection switch problem

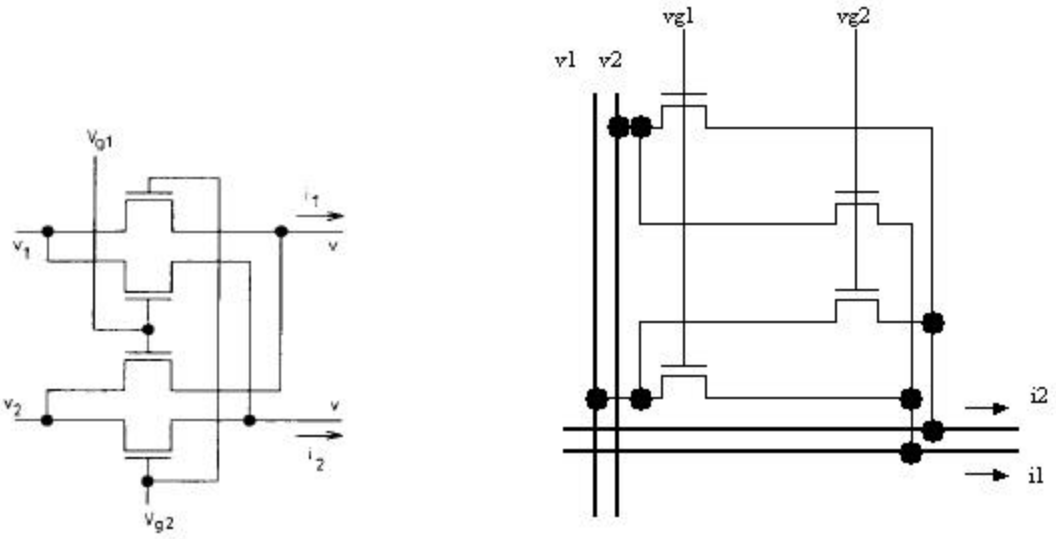


Figure 4: a) MOS Transconductor b) Connection of Transconductor for routing

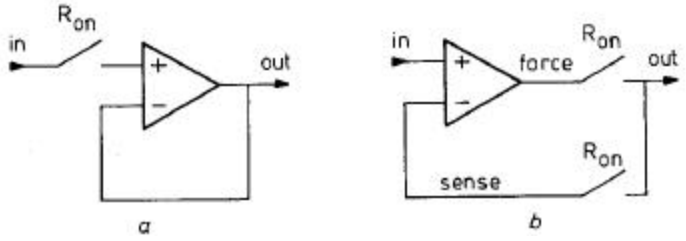


Figure 5: a) Buffered input routing switch
b) Force-sense output routing switch

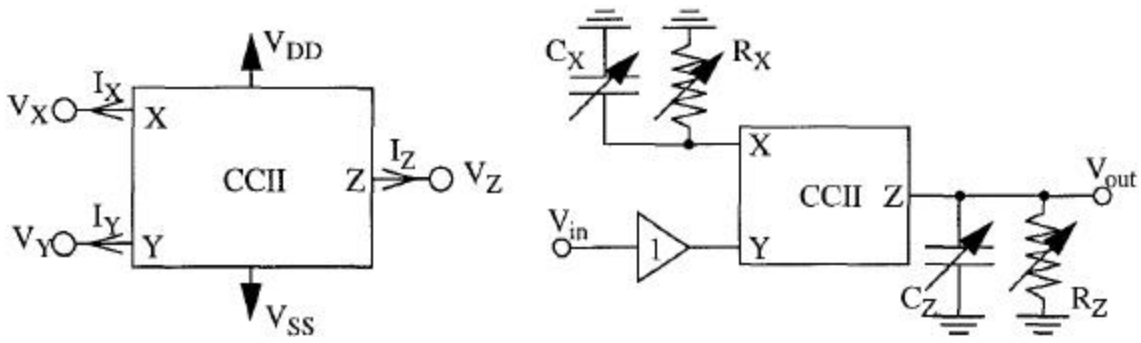


Figure 6: a) Current conveyor symbol b) Current conveyor-based CAB

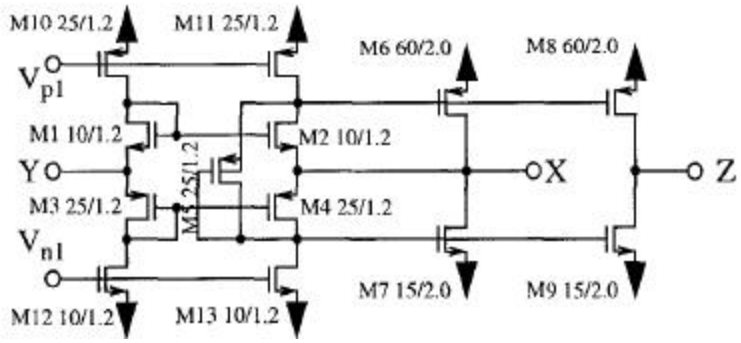
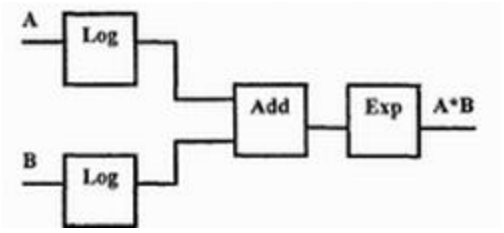


Figure 6: c) Current conveyor schematic



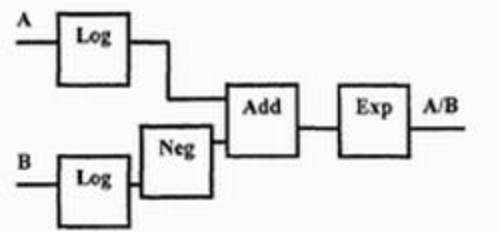


Figure 7: a) Multiplication b) Division

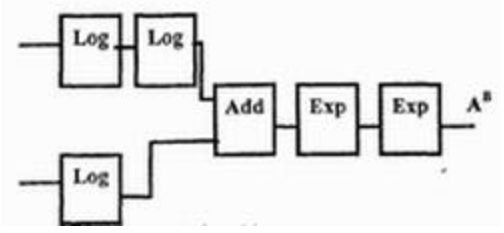


Figure 7: c) Raising to a Power

References

[1] E.Lee and G.Gulak, “Transconductor-Based Field-Programmable Analog Array”, ISSCC Digest of Technical papers, Feb.1995, pp.198-199.

[2] E.Lee, “Field-Programmable Analog Arrays Based on MOS Transconductors”, PhD thesis, Department of Electrical and Computer Engineering, University of Toronto, 1995.

[3] M.Sivilotti, “A Dynamically Configurable Architecture for Prototyping Analog Circuits”, MIT VLSI Conference, 1988, pp.237-258.

[4] C.A.Looby and C.Lyden, “Op-amp based CMOS field-programmable analogue array”, IEE Pro-Circuits Syst., Vol147. No.2, April 2000.

[5] V.C.Gaudet and P.G.Gulak, “CMOS Implementation of a Current Conveyor-Based Field-Programmable Analog Array”, Signals, Systems & Computers, 1997. Conference Record of the Thirty-First Asilomar Conference, Volume 2, 1997, pp. 1156-1159.

[6] A.Buxton, “"Totally reconfigurable analog circuit", concept and practical implementation”, Circuits and Systems, 2000. 42nd Midwest Symposium, Volume 1, 2000, pp. 292 –295.

[7] P.G.Gulak, “Field-Programable Analog Arrays: Past, Present and Future Perspectives”, Microelectronics and VLSI, 1995. TENCON '95., IEEE Region 10 International Conference on , 1995.