SOI VS CMOS FOR ANALOG CIRCUIT

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Abstract – This paper reviews the basic circuit issues of silicon-on-insulator (SOI) technology for metal-oxide-semiconductor (CMOS) circuits. The superior features of SOI in low power, high speed, high device density and the effect of floating body particularly in partial depletion (PD) SOI device are addressed. Analog and RF circuits are considered and their performances are compared with those reported in bulk CMOS.

1. INTRODUCTION

Silicon-on-insulator (SOI) technology has long been used in many special applications, such as radiation-hardened or high-voltage integrated circuits. It is only in recent years that SOI has emerged as a serious contender for low-power high-performance applications [1], [2]. The primary reason is the power consumption of scaled bulk complementary metal-oxide-semiconductor (CMOS) technology. With the bulk CMOS 0.15um technology, the effective channel length does not work satisfactorily within the power constraints of the intended low-voltage applications [2], [3]. Having the feature that the circuit elements are isolated dielectrically, SOI technology significantly reduces junction capacitances and allows the circuits to operate at high speed or substantially lower power at the same speed. The device structure also eliminates latch up in bulk CMOS, improves the short channel effect and soft error immunity. However, despite these advantages of the SOI technology, this technology faces some key challenges in process and manufacturing availability, devices and circuit design issues. At the process level, neither bonded nor separation by implanted oxygen (SIMOX) SOI are mature enough for mass production of low-cost, low-defect-density substrates [2]. At device and

circuit level, the floating body effect in partially depleted devices poses major challenges for large-scale design.

In this paper, we review some fundamentals and basic circuit issue of the SOI technology and compare the performance of SOI circuits with bulk CMOS circuits. Section 2 discusses the SOI device structures, the cause of high speed, low power and high device density, the kink effect results in the floating body and the possible solution to eliminate the kink effects. Section 3 will compare the performance of a SOI op amp and bulk CMOS op amp. RF circuits and their performance comparisons between the SOI and bulk CMOS technology are discussed in Section 4. The conclusion can be found in Section 5.

2. DEVICE STRUCTURE AND CHARACTERICSTICS

2.1 High Speed, low power and high device density

Figure 1 shows the cross section of the bulk and SOI MOS devices.

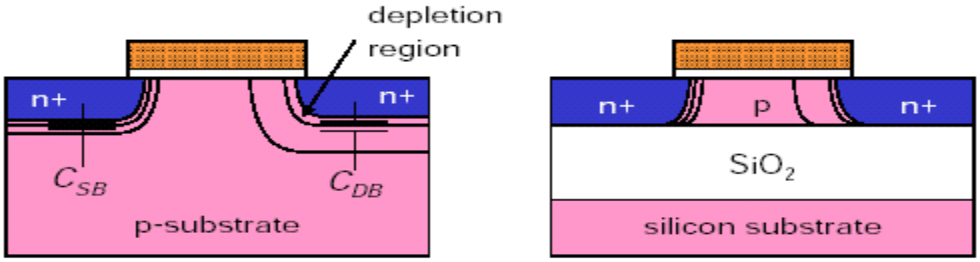

Figure 1: Cross section of bulk and SOI MOS devices

As shown in Figure 1, SOI can reduce the capacitance at the source and drain junctions significantly by eliminating the depletion regions extending into the substrate. This results in a reduction in the RC delay due parasitic capacitance, and hence a higher speed

performance of the SOI CMOS devices compared to bulk CMOS particularly at the downscale power supply voltage.

Owing to the buried oxide structure, the source/drain regions of the SOI NMOS/PMOS devices can be placed against each other without worrying about the possibility of latch up. Therefore, SOI CNOS devices may have a much higher device density. Figure 2 shows the layout of a CMOS inverter circuit using SOI and bulk technologies [4]. As shown in Figure 2, since wells are not needed to separate the N+ region from the P+ region, the smaller layout area of the SOI CMOS circuits leads to smaller leakage current and smaller parasitic capacitances. Since SOI devices do not need the reverse biased junctions and well isolations, their device density can be even higher. As a result, a higher speed at smaller power consumption can be obtained from the SOI CMOS circuits. Consequently, SOI CMOS devices are appropriate to integrate low-power circuits.

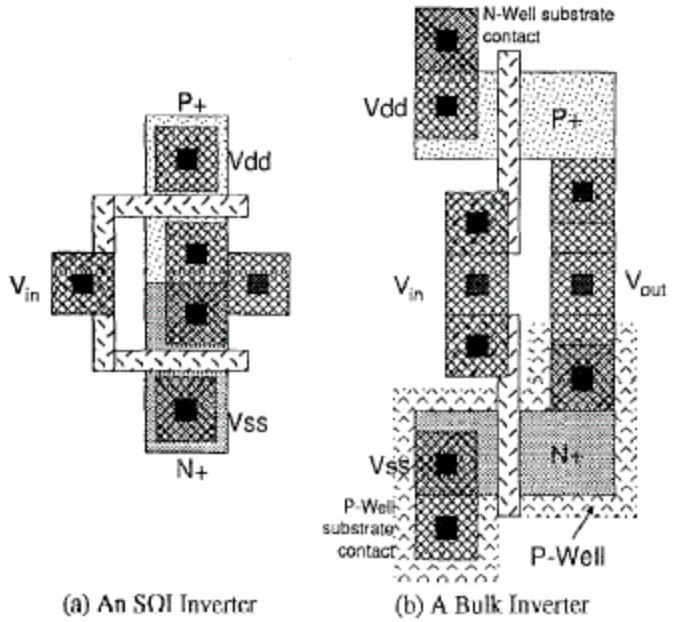

Figure 2: Layout of a CMOS inverter circuit using SOI and bulk technologies.

2.2 Floating Effect and its consequences.

Although the SOI technology provides a low power, high speed and high device density solution to circuit design, it poses structural problems. The MOS device is always accompanied by a parasitic transistor connected in parallel as shown in Figure 3. Unlike the case in bulk silicon, the base of the bipolar transistor is not connected to ground and is floating. When the MOS transistor is biased in the saturation region and the drain voltage exceeds a certain value, the bipolar transistor turns on where the drain current suddenly rises with a discontinuity in the drain current on the IV curves as shown in Figure 4a [5], this is called the kink effect. Kink effects worsen the differential drain conductance of the device as shown in Figure 4b [5] and are strongly dependent to the operating speed, which affect the performance of analog circuits. For an amplifier, the gain at low frequency is substantially degraded with the kink effect. Kink effects are unique in the partial depletion (PD) SOI devices, which means when the body of the device is not depleted fully.

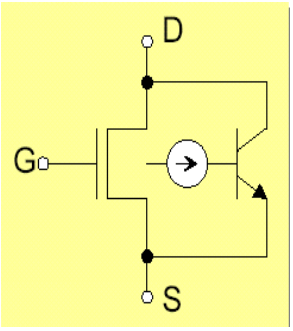

Figure 3: SOI device symbol

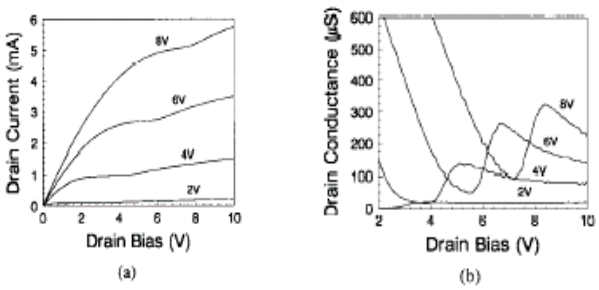

Figure 4: Id and V_{be} vs V_{drain} of a PD SOI NMOS

In order to reduce the kink effect, a method is to provide a body contact for the device, but this will increase the area of the circuit and loss the feature of high device density and small parasitic capacitance. Another method is to via both sides of the channel width

direction. However, this method contributes a large body contact resistance. When this resistance is >100kohm, a substantial amount of holes are accumulated in the body and will trigger the kink effects [8]. As a result, the DC transfer curve becomes worse due to the worsened kink effects.

3. SOI CMOS ANALOG CIRCUIT

SOI CMOS technology has been used to integrate analog circuits. In this section, SOI CMOS op amp is discussed. Then, the performance comparison of op amps using bulk and SOI CMOS technologies is presented.

3.1 Analysis on SOI CMOS Op amp

Figure 5 shows an SOI CMOS single stage op amp with a symmetrical topology. This circuit has a good capability to drive a large capacitive load because of the small threshold voltage [6], and therefore, it is suitable for high-speed operation of the op amp. In addition, the small parasitic capacitances at the source and drain may also help realization of the SOI CMOS op amps for high-speed operation.

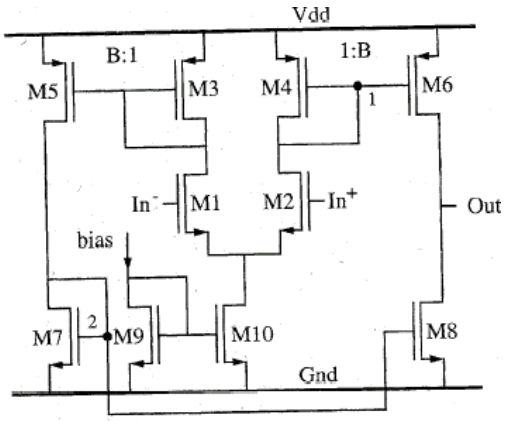

Figure5: SOI CMOS single stage op amp with a symmetrical topology

The analysis of the frequency response is described below. The dominant pole at the output node should contribute to the overall frequency response, and it should not be affected by the poles due to the internal nodes. To achieve this, the nondominant poles due to the capacitance at internal node 1 and 2 need to be several time larger than the transition frequency. The transition frequency (f_T) can be found from equation:

$$f_T = [(W/L)_6 * gm1] / [(W/L)_4 * 2\Pi C_L] \qquad [9]$$

and the frequency of nondominant pole from node 1 is $\omega_{p1} = g_{m4} / C_1$.

C_1 is the total capacitance at the internal node 1. It is equal to

$C_{gs4} + C_{gs6} + C_{gs04} + C_{gs06} + C_{gd06} + C_{bd4} + C_{bd2} + C_{gd02}$

where C_{gs} is the intrinsic gate-source overlap capacitance. C_{gs0} is the gate-source overlap capacitance, C_{gd0} is the gate-drain overlap capacitance and C_{bd} is the body-drain capacitance. Similarly, the frequency of nondominant pole from node 2 is $\omega_{p2} = g_{m7} / C_2$.

C_2 is the total capacitance at the internal node 1 and is equal to

$C_{gs7} + C_{gs8} + C_{gs07} + C_{gs08} + C_{gd07} + C_{bd5} + C_{bd8} + C_{gd08}$

As mentioned in Section 2.1, the buried oxide structure of the SOI devices eliminates the drain-substrate capacitance. Therefore, the capacitor C1 and C2 for the above circuit is very small, which results in the nondominant poles at very high frequency.

3.2 SOI versus bulk CMOS op amp

In this section, the performances of the op amp using SOI CMOS and the bulk CMOS are compared. Figure 6 shows the single stage op amp with symmetric topography that is being compared with different technologies, and Figure 7 shows the plot of g_m/I_D versus $I_D/(W/L)$ [7].

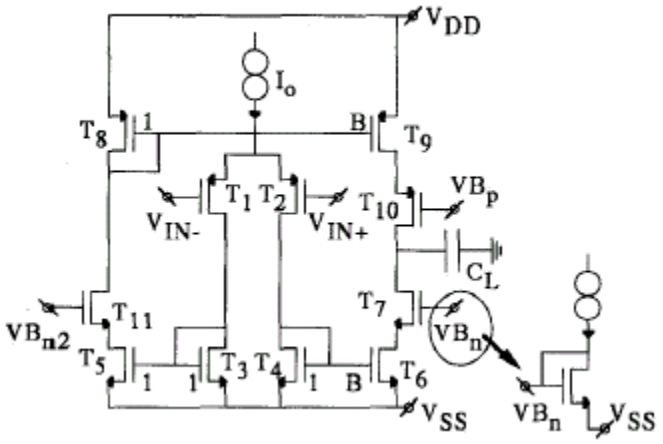

Figure 6: Single stage op amp

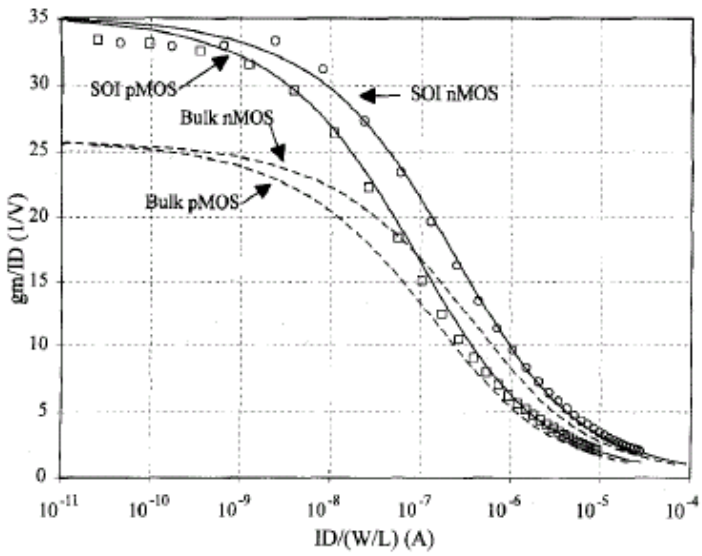

Figure 7: g_m/I_D versus $I_D/(W/L)$

The g_m/I_D ratio is a measure of the efficiency to translate current (hence power) into transconductance [7]; i.e. the greater the ratio value, the greater the transconductance is obtained at a constant current value. As can been seen in Figure 7, the transconductance ratio are maximized in the sub-threshold region and the ratio with SOI is much better than the one with bulk process. However, the ratio decreases as the current increases. The SOI technology degrades at a faster rate than the bulk technology. Therefore, the SOI circuit has a higher gain than bulk CMOS when the circuit is operating at low current

level. At high current biasing, the gain of SOI circuit is only a little much better bulk CMOS. Also, since transit frequency increases with increase transconductance, there is a bigger trade off for the gain and frequency in the SOI circuit compare to the bulk CMOS. Figure 8 shows the performance of the single-stage op amp with an identical transition frequency, using bulk and SOI CMOS devices for various op amp designs with same channel length [7].

	Bulk	SOI1	SOI2	SOI3
$(g_m/I_D)_1$ (1/V)	19	28	27	19
$(g_m/I_D)_2$ (1/V)	17	30	27	17
A_0 (dB)	95.6	103.9	102.7	95.6
Itot (μA)	2.9	2	2	2.9
PM (°)	72.9	72.0	79.0	84.0
ΣW.L (μm^2)	2628	4900	2881	1808

Figure 8: SOI and bulk CMOS op amp performance comparison

The four designs from the above table were optimized to achieve the same transition frequency. The results show that with the same phase margin as bulk, SOI1 implementation has a 45% decrease current consumption and the gain is about 8dB higher. In order to maintain the same gm, the Id of SOI decreases and hence the transconductance ratio increases. Also, the SOI1 transistor need to have a bigger size in order to have the same parasitic capacitance to keep the phase margin equals. Therefore, the die size for the SOI1 is larger than the bulk op amp. Nevertheless, with about the same area size of the bulk and SOI2 op amp, the SOI2 implementation provides a much higher gain with reduced power dissipation and increased phase margin than the bulk implementation. The design SOI3 shows that with the same performance as bulk op amp, the die area is reduced by about 40% without taking into account the area savings due to

the absence of wells in SOI technology. These results show that the op amp circuits do benefit from the advantages of SOI technology as expected.

4. RF CIRCUITS

RF circuits are the key component for a wireless communication system. As the wireless system having more applications, higher bandwidth are used. The performance of the RF circuit, therefore, becomes crucial for such a system. Owing to the low parasitic capacitances in source/drain, high tranconductance, excellent buried oxide isolation and high resistivity substrate, SOI CMOS technology has been used to integrate RF circuits.

In this section, a comparison of suitability between bulk and SOI technology for RF circuits is made. After that, one of the components in RF circuit, low-noise amplifier implemented on SOI and bulk substrates is discussed followed by the performance of another RF circuit component, mixer, using SOI and bulk CMOS technology.

4.1 Suitability for RF circuits using bulk and SOI technology

For implementing RF circuits in a wireless communication system, a few technologies are available. The 0.18um CMOS and 0.35um SOI CMOS technologies are studied here.

Function	Si CMOS, 0.18 u	SOI CMOS, 0.35 u
F_{max} (GHz)	30	60
Linearity	Good	Best
NF_{min} (@2GHz)	<0.8	<0.8
RF Switches	Poor	Best
Low power dig.	Yes	Yes
Passives integration [9]	Poor	Good
A/D; D/A	Yes	Yes
3 V swing	No	Yes
EEPROM/Flash	No	Yes
Isolation	Poor	Good-best
Cost	Best	Good

Figure 9 Availability features for the bulk and SOI process

Compared to the bulk CMOS, SOI technology not only have a higher maximum frequency and better linearity which is necessary for wireless system to share use of the others, it can also provide capabilities for realizing low-voltage digital logic circuits and analog circuits with a large voltage swing. In addition, the buried oxide layer of the SOI CMOS devices lowers the substrate coupling such that the quality factor of the passive element such as inductor and the self-resonant frequency can be enhanced [8]. This results a new solution to the RF integrations. On the other hand, bulk CMOS has limitation on the maximum voltage for mixed signal and non-volatile memory functions. Besides, its substrate limits integrated passive performance and has poor isolation to other technologies such as BiCMOS [9]. The bulk CMOS is not as ideal as the SOI technology for RF circuit integration.

4.2 SOI vs. Bulk CMOS low-noise amplifier (LNA)

LNA is an important component in the RF circuit. In this section, a 4- GHz tuned amplifier is studied. Figure 10 shows the schematics of a 4-GHz tuned amplifier [10].

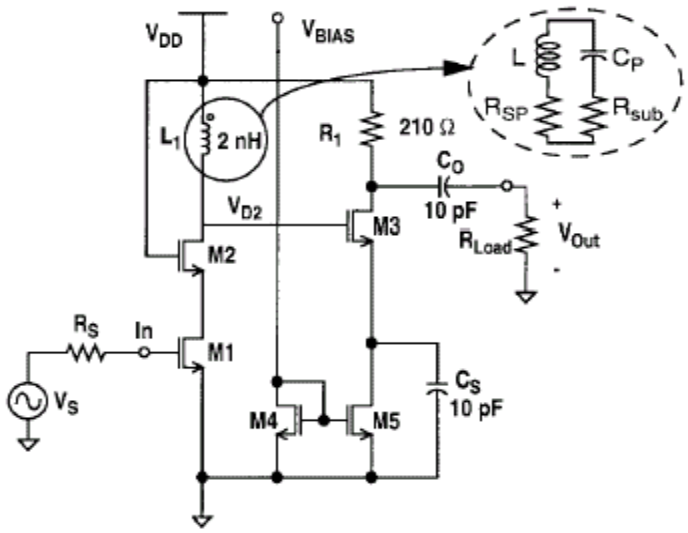

Figure 10: schematics of a 4-GHZ amplifier

The circuit is similar to a 900 MHz LNA implemented in a 0.8 um CMOS process [13]. The design of the tuned amplifier shown in Figure 10 uses a first stage cascode amplifier to determine the gain and the resonant frequency, ω_0, of the tuned amplifier. The second stage is a common source amplifier that drives the 50Ω output load. The resonant frequency is found by:

$\omega_0 = 1/\text{sqrt}\,(L_1 C_T)$ where C_T is the total resistance seen by L_1

C_T is composed of the gate-source capacitance of M3, the gate-drain and drain sub-substrate capacitance of M2, and the equivalent parasitic capacitance of the spiral inductor. Owing to the small drain-substrate capacitance from the SOI devices, the tuned amplifier implemented using SOI technology should provide a good performance. Figure 11 shows the performance of this 4- GHz amplifier using bulk and SOI technology [10].

Substrate	BULK	SOI
Resonance frequency (GHz)	4.1	4.3
Gain (S_{21}) (dB)	14	11
Isolation (S_{12}) (dB)	≤ -38	≤ -38
50-Ω Noise figure (dB)	5.5	6.1
F_{min} (dB)	4.5	-
P_{1dB} (output) (dBm)	-16	-19
IIP3 (output) (dBm)	-	-
Power consumption (mW)	28	28.5
Power supply (V)	1.5	1.5

Figure 11: Performance summary

As shown in Figure 11, the resonance frequency using SOI is higher than using bulk CMOS. This is due to the lower drain-substrate capacitance in the SOI technology. Although the SOI has a higher resonance frequency, the gain and noise characteristic does not perform any better than bulk CMOS as expected. The smaller gain is believed to

caused by parasitic capacitances from metal1, metal2, and transistor and capacitor to the back gate (substrate under the oxide layer in the device). The presence of this parasitic capacitance that assumed to be non-existed is due to the relatively thin oxide layer between metal 1 and the back gate (~0.7um) and the floating body present in the device. Simulation results show that inclusion of these parasitic capacitances reduces the gain for the SOI amplifier by 8dB [14]. This reduction in gain also consequently leads to an increase in the noise figure. Therefore, the parasitic capacitance needs to be eliminated in the SOI technology in order to have a better performance for this circuit.

4.3 SOI vs. bulk CMOS mixer

In addition to LNA, mixer is also important in the RF circuits. A mixer is used with a local oscillator (LO) to convert the input RF signal into intermediate frequency (IF) signal for further processing. In this section, a balanced active chopping mixer and its performance is discussed. The circuit of this mixer is shown in Figure 12 [15].

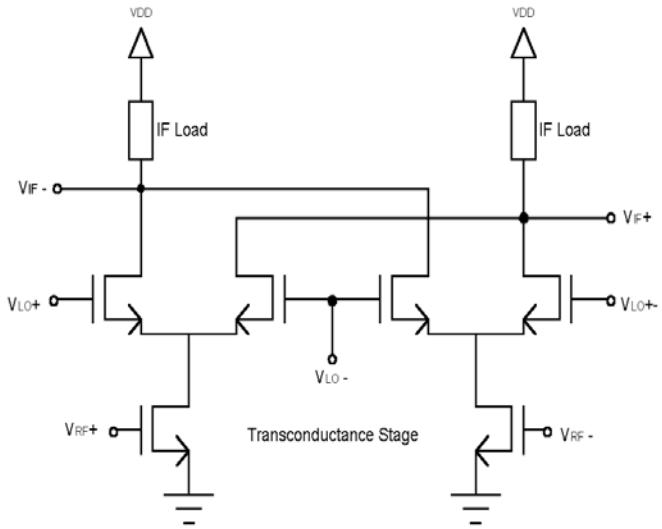

Figure 12: Balanced active chopping mixer

The intermodulation of two neighbouring RF signals was characterized by measuring the third-order intermodulation intercept point IIIP3 at the IF frequency. For LO level equal to 10dBm at 1.8GHz and the IF frequency equal to 5 MHz, the above mixer using the SOI technology operating at 3 V has an IIIP3 of 16.5dBm [15]. The bulk CMOS mixer with a LO frequency equal to 1GHz at the same operating voltage level has an IIIP3 of 8dBm [16]. As a result, the SOI technology provides more than 10dBm of input power level than the bulk CMOS. These measurements results confirm that CMOS technology enables higher frequency of operation than conventional bulk CMOS with the same power supplied.

5. CONCLUSION

The unique device structure and characteristics of SOI device has been reviewed in this paper. Some of the Analog and RF circuits are also analyzed and compared between the performance of using SOI and bulk CMOS. SOI technology has demonstrated to offer high performances, high integration and lower power consumption at low voltage. This makes SOI a very attractive approach for circuits that dedicated to low voltage, low power and high speed. Nevertheless, the unique floating body effect has made design difficult. Ways of dealing with the floating-body effect demand added process steps or circuit area, thus reducing the benefits from SOI. Besides, the volume of production of SOI circuits has been limited by the material availability and hence higher cost is needed. Future of this technology will depend on the availability of new approach for high volume production of SOI wafers with good quality and low cost at the process level. At circuit level, accurate models that deal with the floating- body effect are required to

develop for design purpose. Also, new circuit topologies are needed to overcome the floating- body effect more efficiently. If the cost and floating body issues can be solved, not only the Analog and RF circuits, but also a large range of other applications such as radiation- hard circuits, smart power, MEMS, high temperature electronic and integrated optics can profit from the unique SOI structure, and SOI will become a standard technology for the IC industry.

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