Technology Review of Charge-Coupled Device and CMOS Based Electronic Imagers

Kevin Ng, Student number: 991093945

Abstract – This paper reviewed the technologies that enable Charge-Coupled Device based and CMOS photodiode based image sensors. The advantages and disadvantages of the two types of sensors were presented. It was concluded that in the near future, both types of sensors would continue to play a role in the imaging industry. High image quality applications would continue to demand Charge-Coupled Devices based imagers. Consumer applications that require many features and low power consumption will demand CMOS based imagers. Finally, it is believed that with the constant efforts in the industry to improve CMOS technologies, the performance of CMOS imagers will eventually equal that of their CCD counterparts, if not surpasses them.

1 <u>Introduction</u>

In today's world, the use of electronic imagers can be found in our every day life. They are used in photocopiers, fax machines, and more recently, in digital video and still cameras. For the past 30 years, Charge-Coupled Devices (CCD) based electronic imagers have dominated the industry. The popularity of CCD imagers arises due to the good sensitivity and image uniformity that can be achieved using CCD devices based pixel arrays. In contrast, back in the days when CCD technology was actively pursued, the fabrication technology of CMOS hasn't been fully developed. The immature fabrication technology leads to wide variations in threshold voltages and imperfections at the silicon-to-oxide interface of the CMOS devices. As a consequence of these poor devices, CMOS based imagers have significantly worse performance compared to their CCD counterparts. However, the fabrication technology of CMOS has improved dramatically over the last 10 years due to the high popularity of its use in modern electronics. This revived research interests in CMOS based electronic imagers and designers now claim that the performance of CMOS and CCD based imagers are comparable.

This paper will present the theories of operation of both CCD and CMOS based electronic imagers. A study of the advantages and disadvantages for different applications of each design will be presented. A discussion on the future of electronic imagers will also be given. In the subsequent sections of

this paper, a background on the fundamentals of semiconductor based optical sensors will first be presented. This will be followed by a study of general image system applications and the evaluation criteria used to gauge the performance of such systems. A detailed discussion on CCD based sensors will be provided next, followed by a study of CMOS based sensors. Finally, a discussion on the future of electronic imagers will be given.

2   Background: Image Sensor Fundamentals

In order to appreciate how CCD sensors and CMOS sensors are designed, it is important to understand the fundamentals of silicon based optical transducers. This section provides a brief discussion on the principles of optical transducers.

3   Principles of Optical Transducers

In the design of optical transducers, the ultimate goal is to have a sensor with an electrical output that is proportional to the intensity of illumination on the sensor itself. It is well known from the studies of electrical properties of materials that when a photon with energy greater than the bandgap of the incident semiconductor, the generation of electron-hole (e-h) pairs occurs. This generation of carriers is termed as optical absorption. Ideally one would like to have an abrupt absorption spectrum in which as soon as the energy of the photon is greater than the bandgap, e-h pairs are generated. However, the situation becomes complicated when one is dealing with silicon based optical transducers. This complication results from the fact the silicon is an indirect bandgap material. Recall that for indirect bandgap materials, the crystal momenta k at the minimum energy separation between the conduction band (E_c) and the valence band (E_v) are not equal. Therefore, a difference in momenta, Δk, exists from the intrinsic property of silicon. For incidence photons, their momenta is negligibly small compared to that of the electrons. Hence, the optically induced transitions are for Δk approximately equals to 0. However, in the study of materials, phonons (quantized unit of lattice vibration) exist and their momentum is similar to that of the electrons. Thus, for phonons, Δk is significant. Therefore, for indirect bandgap material like silicon, in order for the incident photon to create an e-h pair, the assistance of a phonon is required. This need for phonon is undesirable since it reduces the transition probability and induces temperature dependence for the optical absorption of the material (since phonons are temperature dependent).

An alternative view to represent to optical absorption of a material is through the use of the absorption coefficient. It was found that when absorption occurs, the intensity of light is given by [1]:

$$I(x) = I_o \exp(-\alpha \cdot x)$$

Here, I_o is a constant based on material property, x is the depth traversed along the material, and α is the absorption coefficient. The penetration depth is defined as 1/ α. From this equation, it is obvious that the penetration depth of photons into a material is wavelength dependent. This dependency can be easily seen, as one knows that the electron transition probability is dependent on the energy of the photon, which is in turn dependent on the wavelength. Recall that the visible wavelengths range from 400nm (blue) to 750nm(red). Therefore, from the absorption coefficient equation, it can be seen that the penetration depth of blue light is less than that of red light. Typically, blue light penetrates about 0.2μm while red light penetrates more that 10μm. This difference in penetration depths can be utilized for the design of color sensors by stacking charge collection layers at different depths into the sensors.

To design a sensor based on the principles of optical absorption, it is necessary to collect the optically generated electrons (or holes). It is well known that in semiconductor devices, recombination of e-h pairs occurs and that is proportional to the number of free electrons and holes. Therefore, to collect the photo-generated carriers, one needs to separate these photo-generated e-h pairs to minimize recombination and then drain these carriers to a contact so that the signal could be read. The use of an electric field to move the photo-generated carriers accomplishes the above goal. Naturally, one would want the location in which the photo-generated carriers to take place at where the electric field is applied. As will be shown later, the use of a built-in electric field forms the basis of CMOS photodiode based sensors and that the use of an externally applied electric field forms the basis of CCD devices.

It was found that in typical illumination levels in a room, the photocurrent that results from the collection of the photo-generated e-h pairs is small, as it is on the order of a few Pico-Amps [1]. It is extremely difficult to read such a small current in practical circuits, which are subjected to noise. Therefore, a practical optical sensor must be able to store up photo-generated charge over a period of time such that a usable signal can be read out. The time required to collect the charge is often termed as integration time in optical sensors designs.

3.1 Evaluation of Imaging Systems

The configuration of a typical imaging system is depicted in Figure 1. The functionality of each block is divided as follows: An array of image sensors forms the pixels of the imaging systems. Timing control circuitry is required to supply the clock necessary to read out the data collected by the optical image sensor. Signal conditioning is then required to shape the signal such that it could be digitized by an Analog-to-Digital Converter (ADC). Finally, memory and Digital Signal Processing units are required for post-processing of the collected image for the application at hand. To evaluate the suitability of different image sensors for different applications, one typically examine the following parameters [2]:
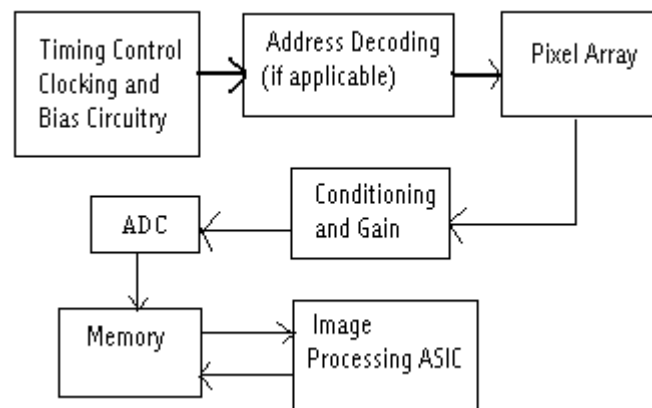

Figure 1 Typical imaging system

3.1.1 Responsivity

This parameter specifies the amount of signal the sensor delivers per unit of the input optical energy.

3.1.2 Dynamic Range

This parameter specifies the range of signals that sensor is capable of outputting. It is ratio of a pixel's saturation level to the minimum resolvable signal in the presence of noise.

3.1.3 Uniformity

This parameter specifies the uniformity of the response of each sensors of the pixel array under the same illumination level. The noise that results from non-uniformity can be generally classified into 2 types.

When offsets in the response of the pixels across the array exist, a Fixed Pattern Noise (FPN) results and it is the root-mean-square (rms) variation of pixel outputs when the sensor array is exposed to zero illumination. On the other hand, when gains of each pixel across the array exist, then Photo-Response Non-Uniformity (PRNU) arises, and it is the rms variation of pixel outputs under uniform, but non-zero illumination.

3.1.4   Shuttering

This parameter specifies the ability to arbitrarily start and stop exposure to the sensor. This ability is particularly important when the imaging application involves the scanning of moving objects. This is an important feature in the image sensor since improper shuttering leads to temporal artifacts in the captured image.

3.1.5   Speed / Throughput

This parameter specifies the rate at which captured image data can be produced.

3.1.6   Image Access

This parameter measures the ability to randomly access the captured image data. This is sometimes called windowing, since it measures the ability to read out a portion of the captured image.

3.1.7   Anti-blooming

This parameter measures the ability to drain the charges captured in overly exposed pixel so that this saturated pixel does not spill signals to neighboring pixels. The spilled over signals would create signal-level artifacts in the captured image and this would contribute to the PRNU of the sensors.

3.1.8   Fill Factor

This parameter measures the percentage of the pixel that is sensitive to light. Larger pixels have more parasitic capacitances and it limits the photo-generated signal that can be read out of the sensor. Therefore, this is a measure of the resolution and Signal-to-Noise Ration (SNR) achievable by the image array

3.1.9   Quantum Efficiency

This parameter is a ratio of the number of electrons (or holes) generated per incident photons. This measures the ability of the sensor to convert incident photons to electrons. For the designers of image sensors, a quantum efficiency of 1 is desirable.

Biasing and Clocking

This parameter measures the system complexity on the imaging system. Depending on the type of image sensors chosen, the required bias and clock circuitry to support the image capture and readout of the system is different.

3.1.10   Reliability

This parameter measures the reliability of the image sensors operating under different expected environmental conditions.

3.1.11   Cost

This parameter measures the cost of the manufacturing the entire imaging system.

4   Theory of Operation of CCD Devices

The concept of the CCD image sensor revolves around the operation of a MOS capacitor. An analogy that is often used to describe the operation of CCD device is that of transferring water using buckets. If one thinks of a single bucket as 1 pixel based on a CCD device and that the water is analogous to the photo-generated charge, then CCD based image sensors operates by pouring these charges from 1 pixel over to the next pixel until it reached a certain read-out point for further signal processing. The operation of the pixel sensor itself will first be discussed, followed by the discussion on the read-out process of CCD image pixel arrays.

4.1   MOS Capacitor as a Photo-sensor

Familiar to all CMOS circuit designer, the MOS structure forms a capacitor when inversion occurs. When a positive voltage is applied at the gate of the MOS capacitor, at equilibrium, the positive charge on the gate is balanced by the negative charge in the conduction channel due to inversion and the negative

exposed ions in the depletion layer. The operation of a CCD based sensor relies on the fact that it takes time to reach this equilibrium. When the gate voltage is first applied, mobile holes are depleted from the semiconductor. To balance the positive charge, the deletion width grows such that the exposed negative ions are equaled to the positive charge. The structure then slowly collects the thermally generated electrons within the depletion region and shrinks the depletion width as more of these electrons are collected. The time it takes to collect enough electrons inversion of the MOS capacitor to occur is on the order of several seconds at room temperature [3]. The steps to reach equilibrium is depicted in Figure 2 below [4]:
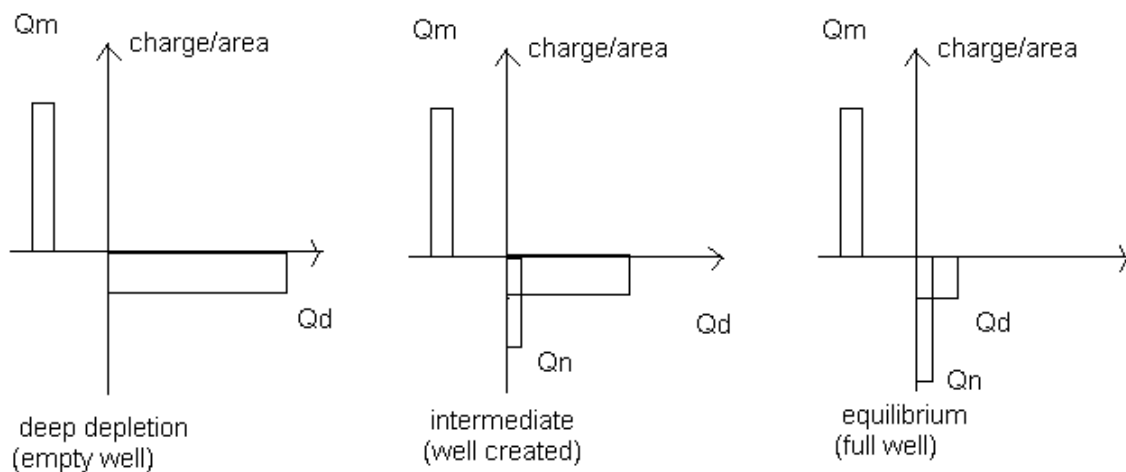

Figure 2 MOS capacitor transient to reach equilibrium when gate voltage is applied

It is during the time to reach this equilibrium (the intermediate step Figure 2) in that the MOS capacitor contains a potential well that is available to collect photo-generated electrons, and hence, making it into an optical sensor. Recall the concept of penetration depth and photo-generated charge collection discussed before. In the case of a MOS capacitor sensor, ideally one would like the incident photons to be absorbed within the depletion width and collected by the built-in electric field there. However, due to different penetration depths of different wavelengths, many photons will be absorbed deeper in the substrate. The collection of these carriers would rely on diffusion of these electrons back into the depletion region, and, hence, there is a dependency on the efficiency of the diffusion length of the device [4].

4.2 CCD Read-Out Techniques and Array Architectures

There are two common approaches in the design of pixel arrays. Linear array is an architecture where a 1-dimensional array of pixels is used as the imager sensor. Using the linear array, it is possible to obtain a 2-dimensional image by scanning across the object of interests. Alternatively, an area array is a 2-dimensional array of pixels and it can capture a 2-dimensional image simultaneously. Architectures of CCD area array typically fall in 4 types [5], namely the full frame transfer, frame transfer, split frames transfer, and interline transfer. The configurations of the architectures are illustrated in Figure 3. In short, full frame architecture requires the image to be directly transferred to the read-out register. With the transfer is in progress, the pending rows are still exposed to illumination and so offsets could result in the captured image. Full frame transfer attempts to correct the above problem by using a light-shield storage area that is of the same size of the pixel array. Therefore, after the integration period, the image is quickly transferred to the storage area. The storage area is then shield from further illumination with the use of shuttering and its content is transferred to the read-out register. Leveraging on the full frame transfer idea, split frame transfer simply splits the storage area in two halves that correspond to the upper and lower section of the image array. This is done to essentially cut the time it takes to transfer the charge from the pixel array to the storage array by half. Finally interline transfer is an architecture that takes the split frame transfer idea to its extreme and divides the imaging array up into alternate columns of photosensitive elements and light shield storage registers. After integration, each column is transferred to the adjacent light shielded storage register. The column storage register is then transferred to the read-out register. Note that for the architectures that attempt to improve offset and read-out time from the full frame architecture, the fill factor of each pixel is sacrificed since more storage components are used.
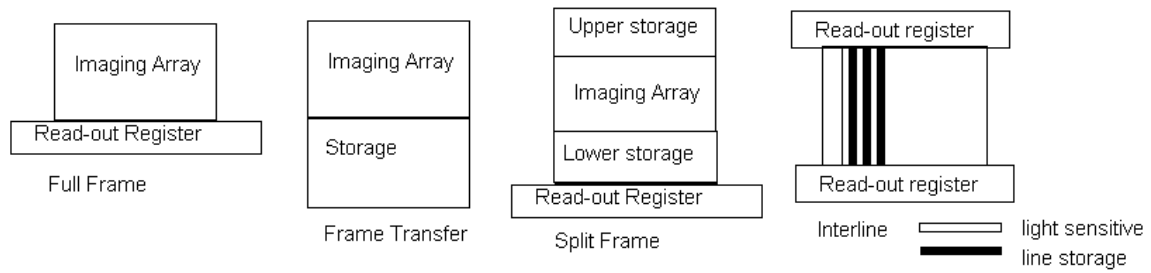
Figure 3 CCD area array architectures

The different architectures were proposed to improve read-out time and to minimize the FPN in the captured image. However, the principles of the read-out scheme can be adequately illustrated using the full frame architecture and it is shown in more details in Figure 4.
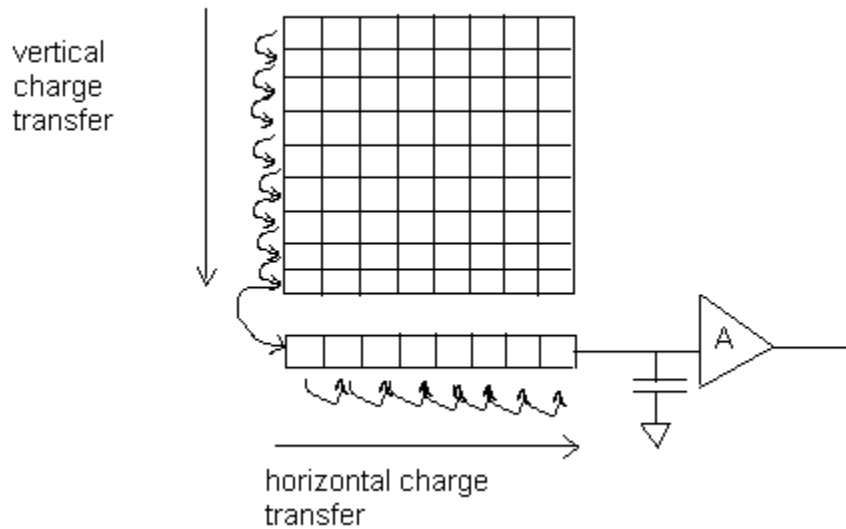

Figure 4 Read out of CCD area array

As shown in Figure 4, for a 2-dimensional pixel array, the charge collected in each pixel after integration time (exposure time to the image) first transfer vertically from row-to-row into a read-out register that holds the value of the entire row. The value of each pixel that represents the column of the row stored in the read-out register is then horizontally shifted out of the register. The direction of the arrows dictates the direction of charge transfer. It is because of this charge pouring process that the name Charge-Coupled Devices came about. The conversion at the end of the read-out register is straight forward as it is implemented by a capacitor that utilizes the charge/voltage relationship of V=Q/C. To initiate the charge

pouring process from pixel to pixel, the use of multi-phase clocking is required. Conceptually, this multi-phase clocking scheme can be thought of as dividing each pixel into multiple phases. It was found that 3-phase clocking achieves high yield and high process tolerance [5]. Using a 3-phase clocking scheme, the process of charge transfer is illustrated in Figure 5
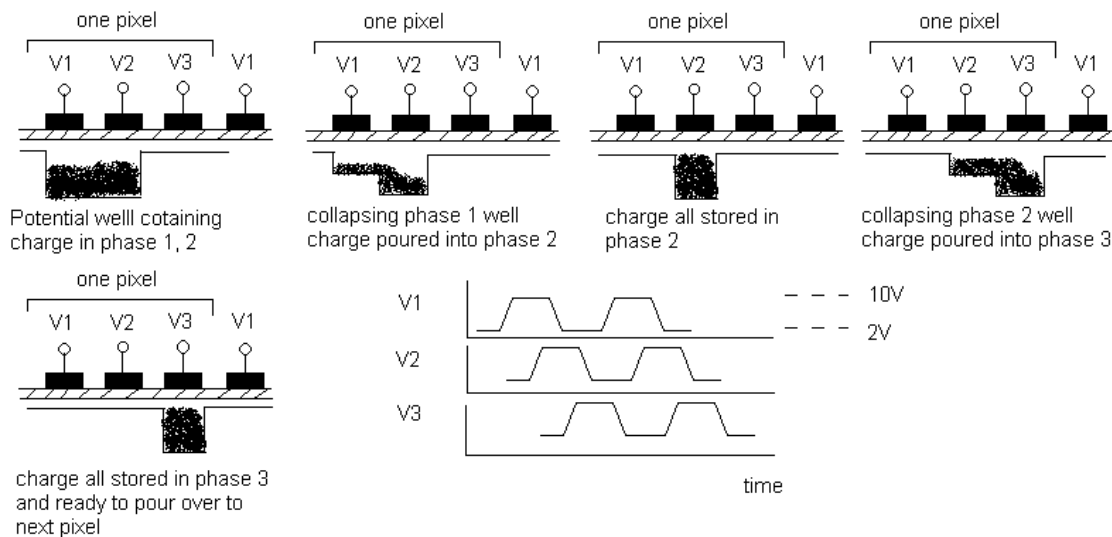

Figure 5 CCD charge transfer sequence

With reference to Figure 5, the charge transfer sequence occurs as follows: first during integration time, phase 1 and 2 are put in charge holding mode by applying a high voltage (the high value of the clock signal which is typically around 10 to 15 Volts) to the gate of the MOS capacitor sensors. This phase corresponds to the time in which both clock signals V1 and V2 are high. This allows photo-generated carriers to be stored in phase 1 and 2 of the pixels. During this time, phase 3 is put in charge blocking mode by applying a low voltage at the gate (the low voltage of the clock which is typically around 0 to 2 Volts). This corresponds to the clock signal V3 being held low. Secondly, phase 1 is put in charge blocking and this force the charge in phase 1 to flow into phase 2. Then, phase 3 is put in charge-holding mode to allow the charge to distribute evenly between phases 2 and 3. This corresponds to the time in which V2 and V3 overlaps at logic high. Finally, phase 2 is put in charge-blocking mode to allow all the charge to flow into phase 3. The above sequence of clocking repeats until the value of the pixels from the furthest row of pixels is now loaded in the readout register. As explained before, the value of each pixel is then horizontally

shifted out of the read-out register and it could be passed to conditioning circuitry before being digitized by an ADC. It was cited in the literature that switched-capacitor supercascode amplifiers have been used to interface with CCD area arrays to provide programmable gain and level shifting for processing by standard CMOS circuits [6]. The detailed operation of these circuits are beyond the scope of this paper but it is worthwhile to note that in order for modern CMOS circuits to process CCD array signals, it is necessary to level-shift the signal down from a high voltage of around 10V to 3.3V. The high voltage of 10V is required in CCD devices in order to provide a large full capacity potential well to hold the photo-generated carriers collected during integration time.

4.2.1 Implications of CCD Read-out Techniques

Recall that in a CCD area array, the furthest pixel from the read-out register needs to be transferred many times before it gets to the read-out register. As a consequence, the charge transfer efficiency becomes an issue. In reality, not a 100% of the charge is transferred from each pixel. The main reason for this non-ideality is that charges might be trapped in defects at the Si and SiO_2 interface or simply the readout does not provide enough time for full charge transfer to occur. In any case, the left behind charge serve as an offset for the image captured on the next integration cycle and this forms the basis of FPN for CCD based imagers. To improve charge-transfer efficiency, additional constraints are placed on the CCD fabrication process. The result of these constraints is that the CCD fabrication process is quite different from standard CMOS process and that it makes it impractical to include integrated electronics into a CCD process. This limitation results in a higher cost of CCD based image systems since additional components must be purchased to provide the signal processing functions. On the up side, the CCD read-out scheme achieves high uniformity across the array since variations between MOS capacitors affects the well capacity but not the signal charge stored. In a sense, it does not matter if 10% variation of well capacity results from fabrication imperfections if only half the well capacity is used for the desired application.

4.3 CCD Fabrication Requirements and Advanced CCD Devices

As mentioned before, it is important to have charge-transfer efficiency close to 100%. The high charge transfer efficiency places constraints on the fabrication process. Generally, charge transfer is

achieved by carrier diffusion and carrier drift. Charge transfer by diffusion is improved with short gates and high diffusion coefficient [3]. Carrier by drift can be assisted by careful design of the MOS gates that are responsible to transfer the charge. Closer and shorter gates could achieve a fringing field that sweeps carriers into the next well of the CCD pixel array. In practice, overlapping gates are created to help create a useful fringing field [3]. The use of overlapping gates implies that at least two separate layers of poly-Si gates and appropriate isolation processing are required in a CCD process. Finally, charge-transfer efficiency degrades as a result of imperfections at the Si and SiO_2 interface. These imperfections manifest themselves as traps at the interface and they from the basis of 1/f noise in MOS based devices [7]. The best method to avoid these traps is to eliminate the interface all together. This idea leads to the creation of the buried channel CCD [3]. Essentially, a buried channel device uses extra implants to move the depletion region of the device away from the oxide interface. However, the trade-off in using buried channel CCD is that the total charge handling capability of the device is reduced [4].

In the literature, other advanced CCD devices have been built to alleviate the problems of anti-blooming and color image capture using CCD devices. Vertical anti-blooming CCD device structure has been used to provide a graceful way to drain away charges when a pixel is saturated. The essence of the vertical anti-blooming device is that a non-uniform p-implant is used in the device. The non-uniform implant provides a weak spot for the drainage of carriers in the saturated pixel. Recall that the penetration depth of different wavelengths light is different. Traditional CCD devices have the problem of obstructing the image photons when they are passed through the polysilicon electrodes and gets absorbed before it reaches the depletion region of the MOS capacitor. This obstruction degrades the quantum efficiency of the CCD sensor. To alleviate this problem, back illuminated CCD devices were proposed where illumination is incident on the back surface of the device, away from the polysilicon electrodes. Together with the use of anti-reflective coating, quantum efficiency as high as 90% has been reported [8].

5   Theory of Operation of CMOS Sensors

Over the years, several CMOS based image sensors have been proposed. The devices proposed include charge injection devices, charge modulation devices, and photodiode based devices [9]. Of these, the CMOS photodiode technique is the most popular. Therefore, this paper will only describe imaging arrays utilizing CMOS photodiode devices.

5.1   CMOS Photodiode

Photodiode used in popular CMOS imagers could be the well-understood P-N diode or for more advanced imagers, the P-I-N which is specifically adapted for imaging applications [10]. The operation of the P-I-N diode is beyond the scope of this paper. The P-N based photodiode is faced with the similar problem of a small photo-generated current that haunts CCD devices. Therefore, similar to CCD sensors approach, an integration time in which the sensor collects enough photo-generated carriers such that a practical signal can be read is required. The resulting photo-generated current is typically converted to a voltage using a capacitor. The conversion capacitor is usually the diode's self-capacitance plus the peripheral capacitances of the connecting devices. The general operation of CMOS photodiode sensor is illustrated in Figure 6.
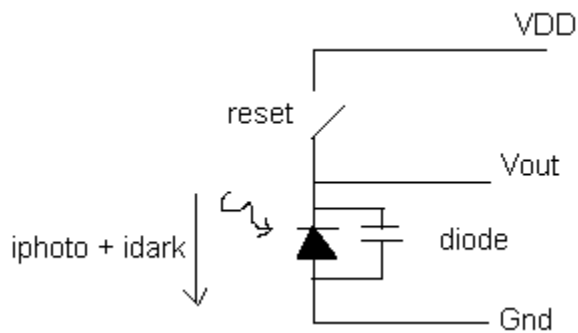

Figure 6 CMOS photodiode sensor

The operation is as follows: the diode is initially reset to a known reverse bias and then the diode is isolated. Over time, the photo-generated current and dark current (the thermally generated current) discharges the capacitor across the diode. Therefore, the voltage across the diode is an indication of the amount of illumination the diode received. It is worth mentioning that the maximum capacity of the capacitor represents the theoretical maximum collectable charge of the photodiode based sensor. In practice, this is an overestimate because the voltage across the diode typically does not reach the full swing of the reset voltage and ground. Therefore, the saturation of the photodiode sensor is usually determined by the voltage swing of the output amplifier that connects to the diode. Another worthwhile note is that dark current densities are typically small (on the order of 500 to 1000 pA/cm^2). With such a small current, it takes typically 20s for the dark current alone to drain the charge of the capacitor [11]. Therefore, typical

integration time of photodiode based sensors is around 100ms in order to keep the contribution from the

dark current insignificant. It was found that the quantum efficiency of photodiode could be expressed as

[9]:

$$\eta = 1 - \frac{\exp(-\alpha\ W)}{1 + \alpha\ Lp}$$

Here, η is the quantum efficiency, α is the absorption coefficient, W is the depletion width of the diode

and Lp is the diffusion length for holes. Note that α is a material property and nothing can be done.

However, W is design dependent as it is dependent on the doping levels in the diode and the reverse bias

voltage used. For integrated CMOS photodiodes, it is typical to use n+-p diodes since they fit well with the

standard CMOS process and Ln > Lp to improve quantum efficiency.

5.2   CMOS Photodiode Read-Out Techniques and Array architectures

The array architecture of CMOS photodiode sensors can be classified into two types, namely, the passive

pixel sensor array (PPS) and the active pixel sensor array (APS). These architectures are illustrated in
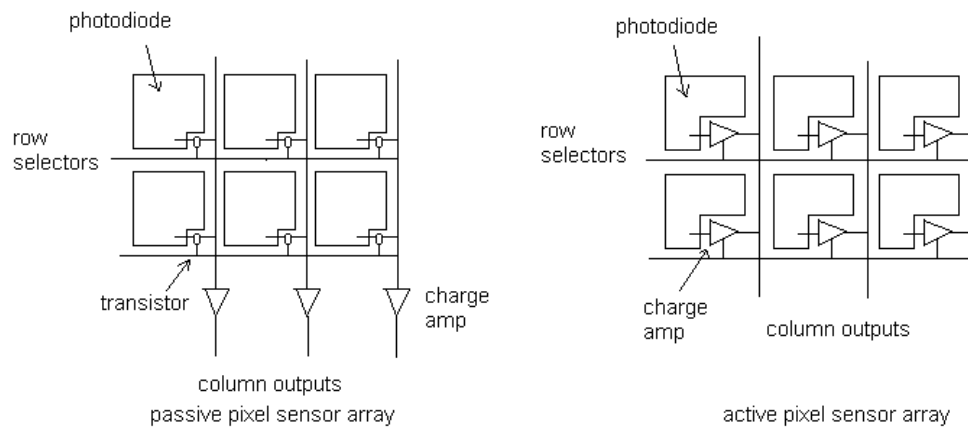
Figure 7.

Figure 7 CMOS photodiode array architectures

Passive pixel arrays are structured such that only transistors used for row and column addressing are part of the pixel. Charge amplifiers are placed at the bottom of each column. On the other hand, active pixel architecture places a charge amplifier in every pixel. Clearly, the fill factor of APS is worse compared to PPS architectures. Due to the fact that transistors have to be placed with the pixel regardless of the chosen architectures, photodiode arrays have fill factors that are worse compared to CCD based arrays. It was reported in the literature that attempts to improve fill factor involved the use of micro-lens to focus the incoming illumination onto the light sensitive part of the pixels [12]. Naturally, the use of micro-lens increased system complexity and thereby increased system cost.

The read-out process for both the PPS and APS architectures are identical. It involves first addressing the row of the array so that the each pixel's charge can be transferred to the charge amplifiers for the column outputs. The addressing scheme is similar to that used for memories in digital devices. The output of the column amplifiers are then loaded in to a read-out register, and the value of each column is horizontally shifted out of the register, much like the technique used for CCD based arrays. The ability to address the rows and columns of the array gives CMOS sensors a distinct advantage in that a portion of the image could be read out for processing at any given time.

5.3   Passive Pixel Sensor Array Read-Out

The design of charge amplifier designed for PPS and APS array architectures read-out has evolved throughout the years Improvements to the original technique reported by G. Weckler were proposed in the literature [13]. The evolution of the design is the beyond the scope of this paper. The interested reader is referred to [13]. Here, the modern implementation of charge amplifier is reported. The key challenge in the design of the charge amplifier lies in the fact that one requires the charge to reset the photodiode to come from the charge amplifier alone. The goal is the minimize the contributions from charges stored in parasitic capacitances stemming from the data lines since this is a capacitance that is not well controlled. Modern implementations for PPS arrays use 1 charge amplifier per column to reduce the capacitance problem. Consider the circuit for a PPS array as shown in Figure 8 [14]
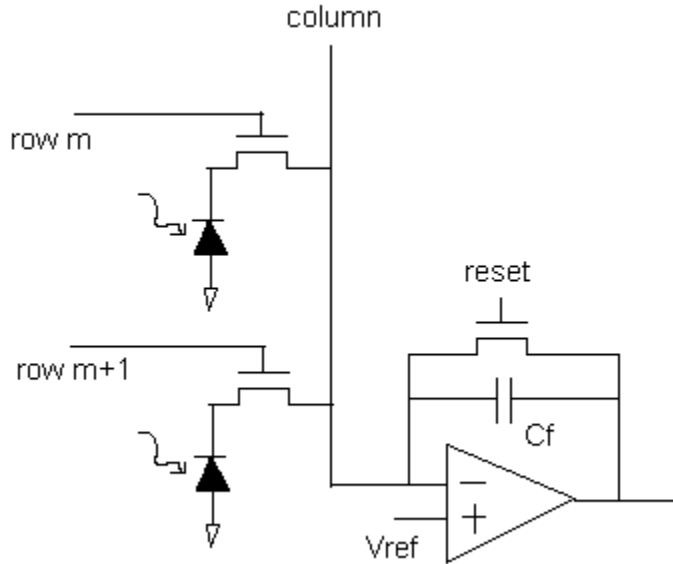
Figure 8 Modern PPS charge amplifier design

The amplifier is configured as an integrator. When the row address transistor is turned on, a current flows through the resistance and capacitance as determined on the column bus. The voltage that creates this current flow comes from V_{ref} - V_{diode}. The total charge required for the reset cycle is integrated by the capacitor C_f and output as a voltage. Therefore, in this configuration, the final column bus and diode voltages are returned to V_{ref} by the charge amplifier. When the address FET is turned off, the voltage across C_f is removed by turning on the reset FET. Using this configuration, the parasitic resistance and capacitance on the bus is still a concern since it affects the speed at which the pixel can be read out. In addition, these parasitics affect the noise associated with the readout. Therefore, modern PPS arrays are limited to small size array to keep these parasitics small. In addition, slow read out speed is typical of PPS systems. It was reported that read-out of PPS system is about 1/10 of a similarly dimensioned CCD system [10]. In addition to slow read-out speed, the use of only 1 charge amplifier per column leads to uniformity problems due to differences between amplifiers. To put these concerns into perspective, it was reported that for typical 0.5 μm process, due to parasitic capacitances, only 90% of the charge to reset the photodiode comes from the integrating capacitor [10]. This is a significant loss of sensitivity. In an attempt to create CMOS photodiode systems with higher resolution and faster read-out speed at the expense of sacrificing fill factor, the idea of active pixel sensor array comes into play.

5.4   Active-Pixel Sensor Array Read-Out

Recall that APS uses one amplifier per pixel. In the early days of CMOS sensors, this configuration posed problems in achieving high uniformity across the array. It was an issue in early CMOS processes since variations between individual diodes and MOSFETS were significant. However, with the recent rapid improvements in CMOS fabrication technology as driven by the computer industry, APS systems become attractive again, despite the fact the uniformity of modern APS systems are still not as good as CCD systems. Read-out of APS systems can be classified into two modes, namely linear integration mode and logarithmic mode [15].

5.4.1   APS Linear Integration Mode

The circuit topology used in APS linear integration system is shown in Figure 9. In this topology, the read-out circuit consists of three transistors.
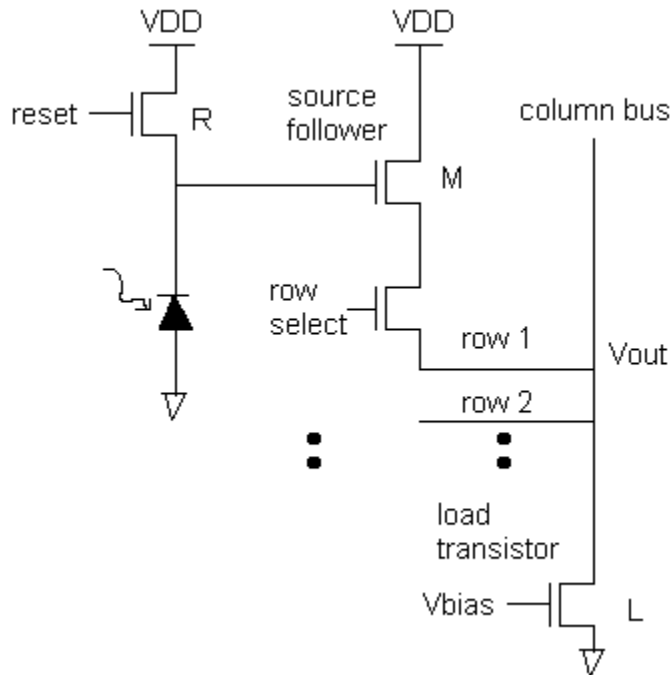

Figure 9 APS linear integration mode read-out circuit

The main concept here is that the sensing capacitance only includes the diode self capacitance, the source of the reset transistor, and the parasitic capacitance of the source follower, M. Note also, that the source follower M acts as a voltage buffer that drives the output independently of the diode. At the end of

each column, there is a single load transistor. The transistors used in APS are mostly NMOS since they are more space efficient, as they do not need a separate device well. However, the savings in silicon real estate is achieved at the cost of losing the range of reset voltage on the photodiode to a value of VDD - V_{TM}, where V_{TM} is the threshold voltage of the source follower M [15]. This constraint limits the dynamic range of the sensor. Analysis of the readout circuit has shown that the range of output voltage achievable is given by $V_{bias} - V_{TL} < V_{out} < V_{DD} - (V_{TM} + V_{TR})$ [15]. Here, V_{TL} and V_{TR} are the threshold voltages of the load transistor and the reset transistor R, respectively. It was reported that typical dynamic range of 75dB has been achieved using linear integration mode [15].

5.4.2   APS Logarithmic Mode

The design of the read-out circuit of APS operating in the linear integration mode has the undesirable effect that the dynamic range of the sensor is limited by the voltage swing of the sensing circuit rather than being constrained by the full-well capacity of the photodiode itself. The motivation of the logarithmic mode is that a logarithmic encoding of the photo-generated current allows a significant improvement in the dynamic range of the sensor. The sensing circuit used for logarithmic mode is shown in Figure 10.
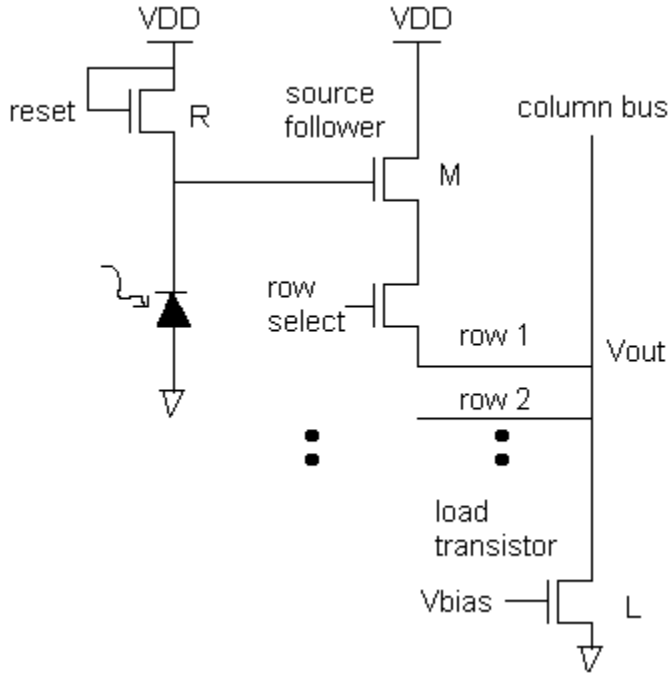
Figure 10 APS logarithmic mode read-out circuit topology

Notice the configuration of the circuit is very similar to that of the APS sensing circuitry used in linear integration mode, with the minor change in the reset transistor. The idea here is that the photo-generated current, i_{photo}, is very small in magnitude, and thus, the resistance looking in to the photodiode is really large. Therefore, the voltage at A is slightly lower than VDD, allowing $i_{DS} = i_{photo}$. The configuration of the reset transistor R is such that the FET is now turned off and operates in the sub-threshold mode of operation. It was found that in this configuration, the output voltage is determined by [16]:

$$V_{OUT} = V_D - \frac{kT}{q} \ln \frac{i_{photo}}{i_O}$$

Here, i_O, is a constant that incorporates the thermally generated leakage current of the diode and kT/q is the thermal voltage term. Clearly, in this mode of operation, as the illumination increases linearly, so do i_{photo} but the output voltage decreases logarithmically. In other words, although the voltage swing of the sensing circuit remained the same, the range of illumination that can be detected has greatly increased. It was reported that improvements of 5 orders of magnitude is achievable with logarithmic mode over linear integration mode and resulting in a dynamic range of about 100dB [16].

5.5   Comparison of APS Linear Integration and Logarithmic Mode

The obvious advantage of using the logarithmic mode over the linear integration mode is the significant improvement in the dynamic range of the sensor. In addition, the logarithmic mode does not require a reset line and so the timing control circuitry of the sensor is simpler and that the fill factor is higher. Moreover, since the photocurrent in this case is directly measured, there is no integration time associated with the logarithmic mode, a truly randomly pixel access system is achieved. However, there exist significant drawbacks in the use of logarithmic APS systems. First of all, the sub-threshold operation of MOSFET is susceptible to process variations. Secondly, the kT/q term in the equation of V_{out} implies that there is high temperature dependence. Moreover, the main challenge comes about because of the small swing of the voltage output signal. The swing is around 0.15V for 5 orders of magnitude swing in illumination. In comparison, even with modern CMOS processes, MOSFET thresholds can vary within 0.1V. This is on the same order of magnitude as the recorded signal [16]. As with other APS systems, the variations in the CMOS process manifest itself as FPN in the captured image. However, for the case of logarithmic APS, the FPN is so severe that additional circuit is required to subtract this built-in background noise signal from the captured image. This increases complexity and cost. Finally, the small magnitude of the photocurrent is hard for practical circuits to detect it in the presence of noise.

6   Future of CCD and CMOS Electronic Imagers

After an in-depth study of both CCD based and CMOS photodiode based sensors, it is now time to re-visit the image system evaluation criteria given in earlier sections. Table 1 below evaluates CCD based and photodiode based sensors under the given evaluation criteria [2].

Table 1 Comparison of CCD and CMOS Photodiode Imagers

Evaluation Parameter	CCD	CMOS Photodiode
Responsivity		Marginally Better
Dynamic Range	About 2x Better	
Uniformity	Better	
Shuttering	Better	

Speed		Better
Image Access / Windowing		Better
Anti-Blooming		Better
Fill Factor	Better	
Quantum Efficiency	Better (Back illuminated CCD)	
Biasing Clocking		Significantly Better
Reliability		Better
Cost		Better

Each type of sensors has its own distinct advantages and disadvantages. The generally accepted state of the sensors is that as of today, CCD still provides higher quality for the captured image. Therefore, CCD based imaging system are particularly favored in high resolution and demanding applications such as scientific, industrial, and medical image processing applications. On the other hand, due to the fact that CMOS photodiode based sensors can be fabricated on standard CMOS processes with processing circuitry placed on the same substrate as the pixel array, commercial applications would continue to demand the use CMOS sensors in the future. Such commercial applications would include digital still camera and security surveillance cameras. The main reason for the use of CMOS in these applications is to keep the camera system small and compact. In addition, biometrics applications such as finger print reader, facial recognition applications would also favor CMOS imaging systems since the image quality required is not high, but the post processing function requirements are high. CMOS sensors allow tight integration of post processing circuitry with the pixel array itself. It is also important to realize that CMOS imagers have much lower power consumption compared to CCD systems. This is a result from the fact that CCD systems need high gate voltages to create a large potential well to hold photo-generated carriers. Typical CMOS power supply voltages are much smaller, hence, lower power consumption. This feature again makes CMOS suitable for consumer electronic applications.

In determining the future trends for both CCD and CMOS imagers, it is worthwhile to note that the cost advantage of CMOS based system might not hold as CMOS imagers move into high image-quality applications. The reason being is that the standard CMOS process for digital and/or analog mixed signal

process is not fine-tuned for photosensitivity. It is predicted that in order for CMOS imagers to reach the image quality of their CCD counterparts, it is required to build a fine-tuned optical CMOS process [17]. Here, the use of a specialized process cuts in on the cost saving advantage that CMOS imagers have over CCD. However, it is unarguable that system integration provides better cost savings for CMOS imagers. Emerging space observation applications would also favor the use of CMOS imagers since they are more compact and are much more robust compared to CCD devices in the presence of radiation.

In the industry, there are proposals to develop a combined CMOS/CDD process. As of today, there are test CMOS/CCD processes but the yield was reported to be low [19]. The main drawback here is that the combined process is neither standard CMOS nor standard CCD, so it requires extensive development expenses. This idea of a combined process has not taken off yet due to fact that few companies in the industry has to resources to have to access to both sets of fabrication facilities and design experience.

In summary, the author believes that in the near future, both CCD and CMOS sensors will continue to have a role in the industry. CCD sensors will be favored by high demand applications that require high image quality. CMOS sensors will be favored by consumer applications that require low power consumption and compact designs. With the constant drive from the computer industry to improve circuits built on standard CMOS process, the author believes that going forward, heavy research and development efforts in CMOS imagers would allow CMOS imagers with quality that are similar to their CCD counterparts, if not, better than them.

7   References

[1] Gregory, T.A. Kovacs, "Micro Machined Transducer Source Book", McGraw-Hill. 1998.

[2] Dave Litwiller,"CCD vs. CMOS: Facts and Fiction", Photonics Spectra, January 2001.

[3] J.Beynon and D. Lamb, "Charge-Coupled Devices and Their Applications". McGraw-Hill, 1980.

[4] A. Theuwissen, "Solid State Imaging With Charge-Coupled Devices", Kluwer Academics Publishing, 1995.

[5] Stuart A. Taylor, "CCD and CMOS Imaging Array Technologies: Technology Review", Technical Report EPC 106, Xerox Research Centre Europe, 1998.

[6] K. Y. Kim and A. A. Abidi, "A CMOS Interface IC for CCD Imagers", Proceedings of International Symposium on VLSI Technology, Systems, Applications, pp. 227-281, May 1993.

[7] Hui Tian and Abbas El Gamal, "Analysis of 1/f noise in CMOS APS", Information Systems Laboratory, Stanford University.

[8] George M. Williams et. al, "Back-Illuminated CCD Imagers for High Information Content Digital Photography", PixelVision Inc.

[9] H-S Wong, "Technology and device scaling considerations for CMOS imagers", IEEE Trans. on Electron Devices, vol. 43, pp. 2121, 1996.

[10] E. Fossum, "Active pixel sensors: Are CCDs dinosaurs?", Proceedings of SPIE, vol 2, pp. 1900, 1993.

[11] R. Dyck and G. Weckler, "Integrated arrays of silicon photodetectors for image sensors", IEEE Trans. on Electron Devices, ED-15, 1968.

[12] G. R. Allan et. al, "High-speed, high resolution, color CCD image sensor", DALSA Inc.

[13] G. Weckler, "Operation of p-n junction photodetectors for CMOS imagers", IEEE Trans. on Electron Devices, vol. 43, pp. 2131, 1996.

[14] Paul Suni, "Advanced design creates single-chip image systems", Laser focus World, pp. 73, 1997.

[15] N. Tu et al., "CMOS Active Pixel Image Sensor with Combined Linear and Logarithmic Mode Operation", University of Waterloo, 1998.

[16] Muahel Tabet et al., "Modeling and Characterization of Logarithmic CMOS Active Pixel Sensors", University of Waterloo.

[17] A. Theuwissen et. al., "Building a Better Mousetrap: Modified CMOS processes improve sensor performance", SPIE's OE Magazine, pp. 29 – 32, January 2001.

[18] C . Matsumoto, "Startup develops CCD-CMOS hybrid", Electronic Engineering Times, January 1997.