

# **ECE1352 Analog Integrated Circuits**

## **Reading Assignment:**

### **Phase Interpolating Circuits**

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## 1 Introduction

A critical area of development in present high-speed electronic systems is high-speed inter-chip signalling. There are two main domains of interest: i) low-latency, parallel links such as memory busses and processor interconnection busses and ii) high-latency, serial communication links, for example, backplane interconnections in a large system.

The memory-processor interconnection in modern processor architectures has been a bottleneck for a significant number of years, often referred to as the von Neumann bottleneck, and has spurred much of the research into high data rate inter-chip signalling. Also, the domain of parallel computing has gained widespread adoption in recent years, furthering interest in decreasing the latency of interprocessor communication and increasing the communication rate.

Low-latency channels often include an explicit clock signal along with the parallel data and thus the main receiver problem is to use the clock to sample the incoming data at the optimal point. In serial-links, the clock is usually implicit in the data stream and a joint clock and data recovery (CDR) circuit is used to recover the clock from the input stream and use it to sample the data.

Many of the timing problems related to high-speed signalling are mitigated through the use of phase-interpolating circuits to generate precise clock phases as standalone circuits or as part of a phase-locked loop (PLL) or delay-locked loop (DLL) architecture. Phase interpolators are becoming critical components in many implementations. The required behaviour of phase interpolators and prevailing architectures and their strengths and limitations are examined in this report.

## 2 Phase Interpolation

The general functionality of phase interpolating circuits and their role in various subsystems is described in this section.

## 2.1 Phase Interpolation

The basic operation of a phase interpolator is straightforward. Following [1], the most general form of a phase interpolator has two periodic input signals (herein called clocks)  $\phi'$  and  $\psi'$ , usually with the same period of oscillation and derived from the same source, and a control input. The control input specifies the interpolated phase mixing requirement and is often a digital signal that indicates the interpolation weighting factor. An interpolated output signal  $\Theta$  is produced as well as delayed versions of  $\phi'$  and  $\psi'$  called  $\phi$  and  $\psi$ , respectively. A block diagram of a phase interpolator, adapted from [1], is displayed in Figure 1. The functionality of the phase interpolator can be described as follows. Consider

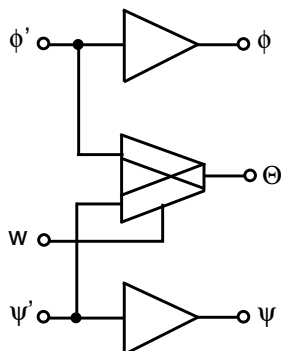


Figure 1: Block diagram of a phase interpolator.

the above system with two inputs having absolute phase  $\phi'$  and  $\psi'$  and a digital weighting factor,  $w$ , that can vary from 0 to  $W$ . The outputs  $\phi$  and  $\psi$  are delayed versions of  $\phi'$  and  $\psi'$  respectively. A control value of  $w = 0$  causes a signal with phase  $\phi$  to be output and  $w = W$  causes a signal with phase  $\psi$  to be output. The general form of the output phase is

$$\Theta = \frac{w}{W}\phi + \frac{W - w}{W}\psi$$

with all phase values taken modulo  $2\pi$  in radians. The inputs to a phase interpolator are usually no more than  $90^\circ$  out of phase and  $45^\circ$  is more common.

Figure 2 shows a simplistic implementation of a phase interpolator, with accompanying waveforms. The control signal  $w$  sets the variable current sources that are in turn switched into the signal path by transistors controlled by the input signals. The weighted currents

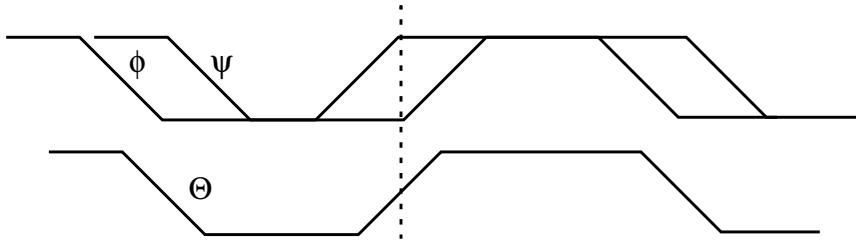


Figure 2: Phase interpolation output waveforms.

are converted into an output voltage across resistor  $R$ . This general method of interpolation can be viewed as a form of phase blending.

A plot of the ideal transfer function of a phase interpolator is displayed in Figure 3. The input variable is the weighting function and the output variable is the phase of the output signal. The plot was constructed assuming the phase interpolator inputs have a phase difference of  $45^\circ$ . The control input varies in discrete steps from 0 to 15 for the

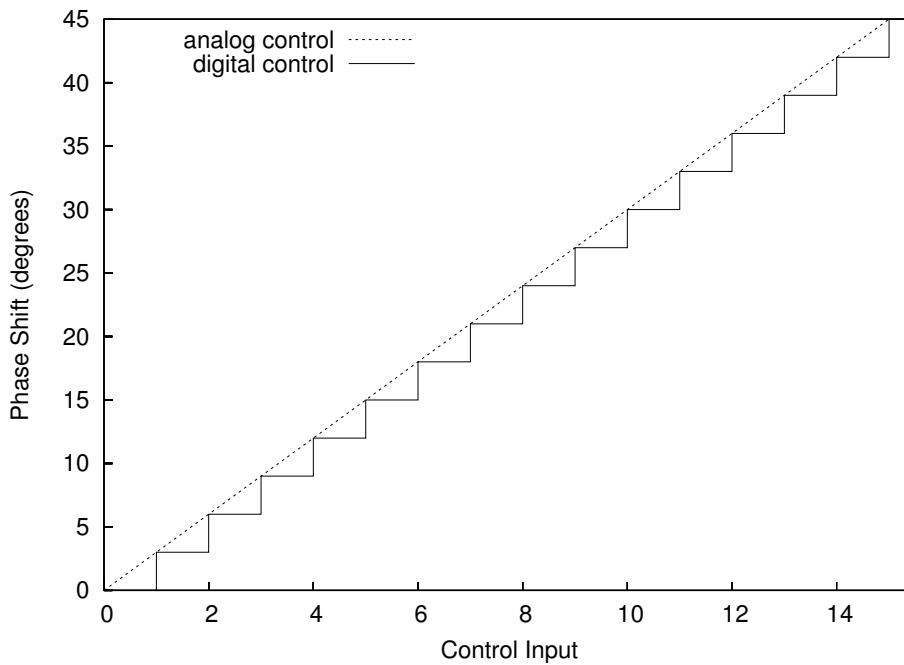


Figure 3: Plot of phase interpolator transfer function.

digital plot. The analog transfer characteristic is shown, however, the  $x$ -axis for the analog

plot would be an analog voltage rather than a digital number.

There are several desirable properties for the behaviour of phase interpolating circuits. They include:

1. A monotonic transfer characteristic.
2. A linear transfer characteristic.
3. Maximum rejection when the control input is set to the minimum or maximum value (i.e. only one input waveform should affect the output). This is referred to as the *seamless boundary* requirement in [1].
4. Insensitivity to input waveform risetime and falltime.
5. Insensitivity to delay between inputs.
6. Insensitivity to process, temperature, and supply voltage variation.

The relative importance of each property varies with the specific application. For example, in [1], it is noted that monotonicity and insensitivity to process, temperature, and voltage variation are paramount.

## 2.2 Applications of Phase Interpolation

Phase interpolating circuits are required in high-speed signalling circuits [2] to generate precisely aligned clocks. In links where no explicit clock is transmitted a PLL-based CDR system is often used. The PLL generates a clock with a voltage-controlled oscillator (VCO) [3] which is used to generate four or eight phases of a clock. In order to have a higher phase granularity, a phase interpolator can be used to interpolate between the four or eight VCO phases. It is usually impractical to generate more than eight phases directly from the VCO since the a ring oscillator is used to generate the clock. As the number of stages in a ring oscillator increases, thus providing more phases, the frequency of oscillation decreases. It is thus difficult to generate a high frequency clock with a large number of phases. An examples of a PLL design that incorporates a phase interpolator is presented in [4].

In low latency, parallel communication links where the clock is distributed with the data, it still often necessary to generate a clock of different phase from the source clock to allow for precise data sampling alignment. In this case, the input clock is fed into a series of buffers that generate multiple phases (again, usually four or eight phases) and a phase interpolator is used to derive intermediate phases. This precisely aligned clock is then



used to sample the incoming data. Often, this system is implemented using a DLL and the delay chain is called voltage-controlled delay line (VCDL). An example of a DLL design that incorporates a phase interpolator is presented in [1, 5].

## 3 Implementations

### 3.1 Overview

All techniques presented below are variations on the same basic architecture. First, the weighting signal and its complement\* are transformed into weighted currents. These currents are then mixed based on the input waveforms  $\phi'$  and  $\psi'$ . The basic architectural difference in phase interpolating systems is the method that is used to transform the phase-mixed current mode signal to an output voltage. The predominant approach is to convert the current to a voltage by using an output load. The actual loads used vary from resistors to different forms of active loads. The second approach to current-to-voltage to conversion is to differentially charge and discharge two capacitors. This method is a current integration approach. A comparator is used to sense the differential voltage on the two output capacitors and to convert it to an output waveform with high slew rate.

The main development in phase interpolating circuits has been with respect to the loading and biasing circuitry rather than in the basic architecture. Two significant improvements are the use symmetric loads and the use of replica biasing.

### 3.2 Differential MCML Buffer-Based Design

The first approach of phase interpolator implementation, phase blending with output loads, is exemplified by the design in [1, 5]. The phase interpolator design is based on a MOS current mode logic (MCML) differential buffer [6] displayed in Figure 4. The MCML buffer generates a differential output signals,  $V_{OUT+}$  and  $V_{OUT-}$ , based on differential inputs  $V_{IN+}$  and  $V_{IN-}$ . A differential source-coupled pair is used to convert the input voltage to a current. The bias current in the differential pair is provided by the NMOS pulldown resistor controlled by the bias voltage  $V_{BIAS}$ . A generic differential load is shown in the

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\*The digital form of the complement of  $w$  is  $W - w$ , for analog control a differential signal is usually supplied so the complement of  $V_{C+}$  is  $V_{C-}$ .

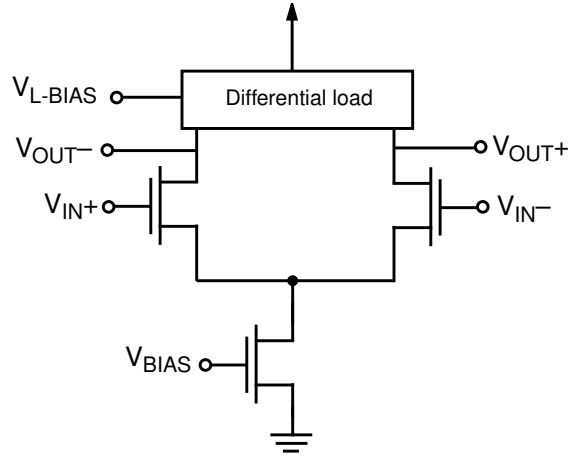


Figure 4: MCML differential output buffer schematic.

figure which, in general, may require a bias input. The differential load converts the differential currents to output voltages across the loads. A selection of possible loads for the MCML circuits [7] are displayed in Figure 5. The signal swing of MCML circuits is usually small compared to full-rail complementary CMOS logic.

The simplest load is a pair of resistor loads, displayed in Figure 5(a). Resistor loads are somewhat impractical considering that accurate resistors are usually difficult to manufacture using on-chip components. Alternative and popular differential loads that mimic resistive loads using active devices are displayed in Figure 5(b). Called symmetric loads, each load consists of a diode-connected PMOS and a parallel PMOS transistor biased in the triode region. The combination of the diode and triode regions result in an extremely linear  $I-V$  characteristic over a large range of voltages. A plot of the  $I-V$  characteristic of a symmetric load in  $0.13\ \mu\text{m}$  CMOS technology is displayed in Figure 6. The third type of load shown is the differential load using diode connected PMOS transistors shunted with cross-coupled PMOS loads. This configuration provides a very high differential impedance although must be taken to avoid introducing hysteresis into the circuit. No reported phase interpolators have used this last set of differential loads.

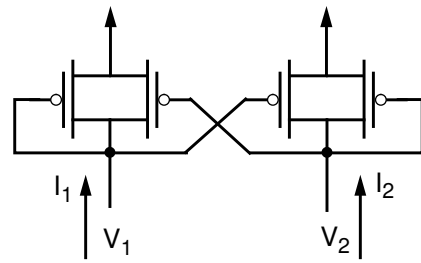
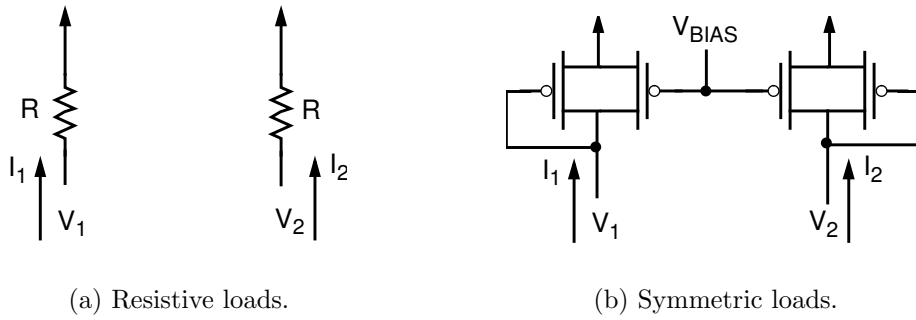


Figure 5: Possible MCML loads.

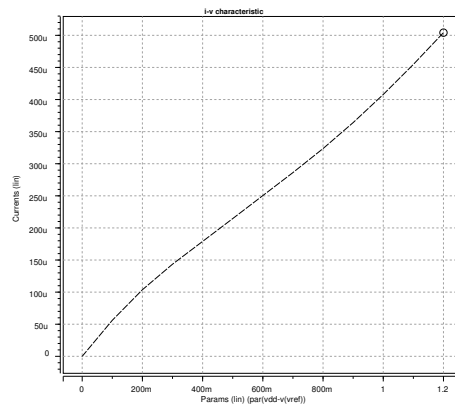


Figure 6: I-V characteristic of symmetric loads.

### 3.2.1 Replica Biasing

In the design reported in [1, 5] symmetric loads are used. The biasing network is described in detail in [8]. A replica-bias circuit is used to generate the bias voltages for the NMOS current source and the symmetric PMOS loads of the MCML loads. It is noted in the reference that using the replica-bias technique to generate the NMOS bias voltage results in a high static supply rejection. The replica-bias technique further allows for high dynamic supply noise rejection by the symmetric loads. It is noted that performance similar to a cascoded loads is achieved without the loss in voltage headroom. A schematic for the

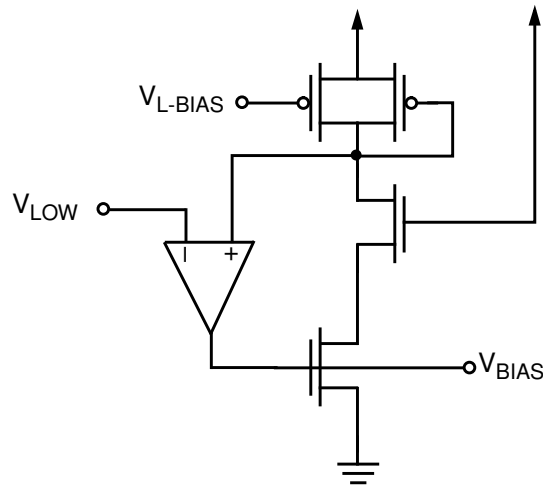


Figure 7: Replica-bias circuit.

replica-bias circuit used in the phase interpolator is displayed in Figure 7 and is adapted from [8] and [7]. The circuit consists of a replica of half of the MCML differential buffer in the ON state (i.e. with the NMOS differential pair transistor input tied to the high voltage). The voltage  $V_{LOW}$  is the target low signal swing of the MCML gate. The output voltage  $V_{BIAS}$  is used to bias the NMOS current source such that the drain voltage across the symmetric load close to  $V_{LOW}$  (due to the virtual short at the inputs of the amplifier). In general, this the feedback loop may require compensation for stability. The replica-bias circuit actually used is modified as shown in Figure 8 to additionally generate the bias voltage for the symmetric loads. A second, buffer stage is added to the replica bias circuit to generate the output voltage  $V_{L-BIAS}$ . The output  $V_{L-BIAS}$  is nominally equal to  $V_{CTRL}$ .

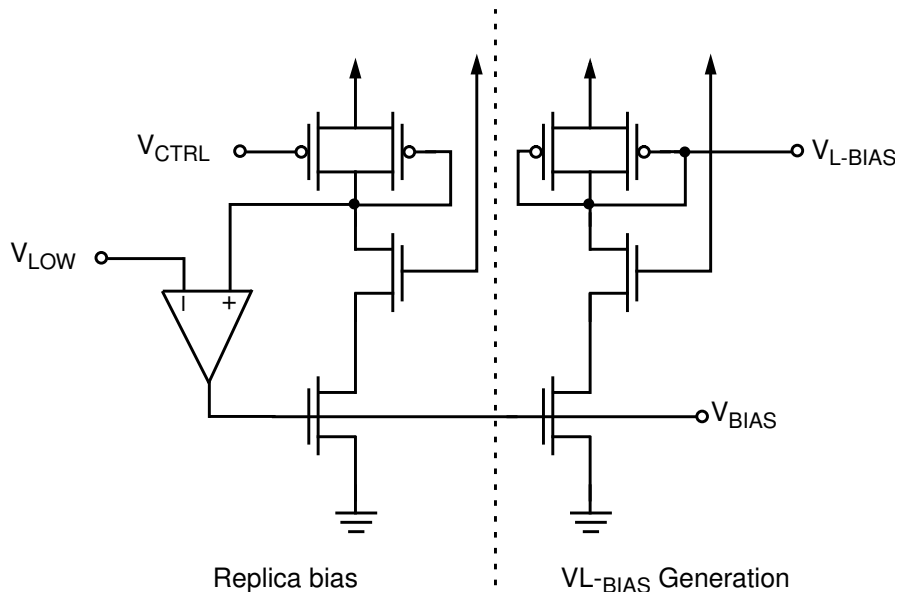


Figure 8: Replica-bias circuit with  $V_{L-BIAS}$  generation.

### 3.3 MCML-Based Phase Interpolator

Two similar architectures for phase interpolators are described in [1, 5]. The first implementation is displayed in Figure 9 which is similar to a differential MCML OR/NOR gate. The phase interpolator differential inputs  $\phi+$ ,  $\phi-$  and  $\psi+$ ,  $\psi-$  control when the weighted current sources are switched into the  $\Theta+$  or  $\Theta-$  signal path. The  $\phi$  branch current sources and the  $\psi$  branch current sources are broken up into  $n$  separate current sources all controlled by bias voltage  $V_{CN}$  generated from the replica-bias circuit described earlier. Each current source is connected to the source of the appropriate differential pair through transistors operating as switches controlled by  $I_{CTL}$  signals\*. Symmetric loads are used to convert the current mode signal to a differential output voltage. This implementation is referred to by the author as a type I implementation. A drawback of this implementation is the violation of the seamless boundary requirement described earlier. When one of the differential pairs is supposed to be inactive because the weighting control has been set to all zeros or all ones, the inactive input has an affect on the output. This effect is due to

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\*Note that only the total number of ones and zeros, called the weight of the input, matters (i.e.  $I_{CTL} = 0011$  would have the same effect as  $I_{CTL} = 1100$ ).

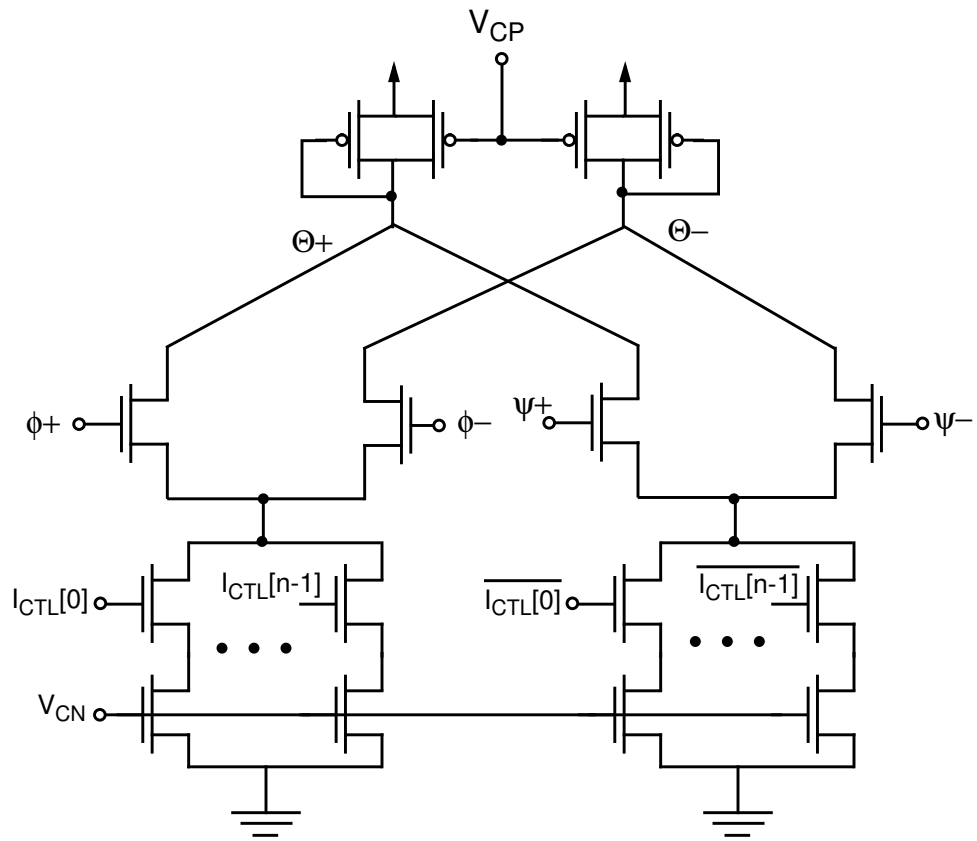


Figure 9: Phase interpolator implementation, type I.

the gate-drain coupling capacitance in the NMOS differential input transistors.

To alleviate this problem, an alternative, albeit very similar, implementation is proposed which is displayed in Figure 10, with the *unitCell* block shown in detail in Figure 11. This

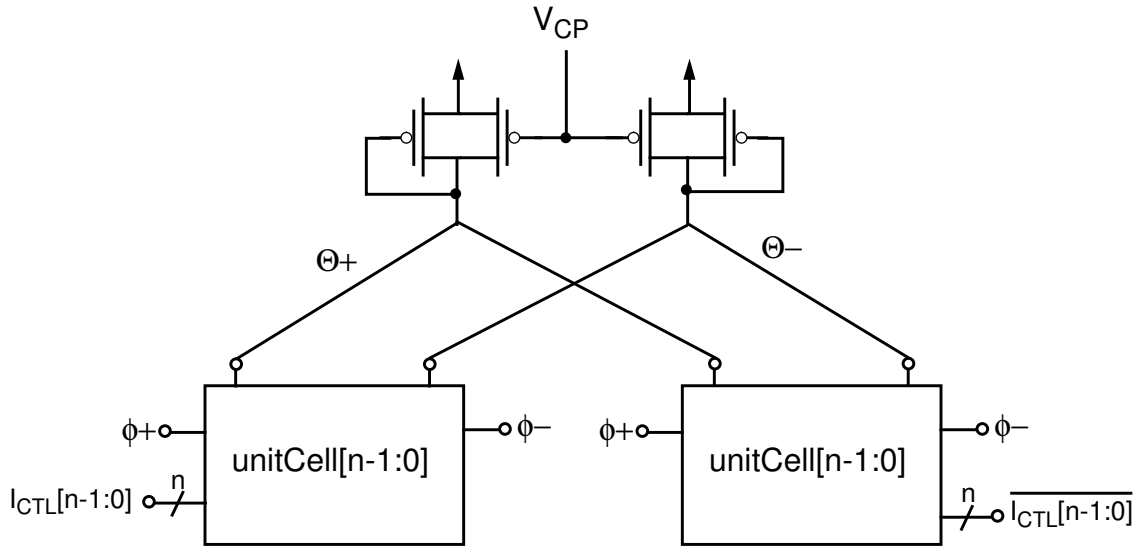


Figure 10: Phase interpolator implementation, type II.

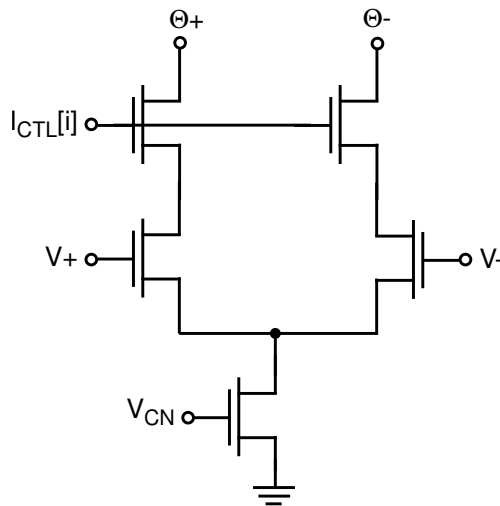


Figure 11: Unit cell of type II phase interpolator.

type II implementation moves the bias control switches up the stack. As a result the

differential pairs are duplicated as well as each current source. This is in contrast to the type I circuit where only one set of differential pairs is used. The gate-drain coupling capacitance of the NMOS transistors is not connected to the output nodes  $\Theta+$  and  $\Theta-$  when the associated control switches are turned off, thus meeting the seamless boundary requirement. The trade-off is that the transfer characteristic of this implementation suffers from non-linearity. This non-linearity is due to the effect of data-dependent loading of the phase interpolator on the previous stage. The effect of the changing weight control is to distort the inputs waveforms causing a non-linear response.

The random variation of the threshold voltage of the in the differential pairs and the various current sources and control devices also affects the linearity of the response.

Another limitation of this design, noted in [9] is that the linearity of the waveform is strongly dependent on the input waveforms' rising and falling edges overlapping. If the input waveforms are phase difference results in a rising or falling edge spacing greater than the  $RC$  time constant of the interpolator, then the output waveform is a poor approximation of the desired waveform. The  $RC$  the first-order time constant of this circuit is set by the resistance at the output node which due to the load resistance of the symmetric loads in parallel with the load resistance of the differential pair NMOS, and the capacitance,  $C$ , is set by the parasitic capacitances at the output node and the input capacitance of the next stage.

### 3.4 Current Integration Architectures

A second type of architecture is based on current integration using capacitors and comparator sensing of the differential voltage on the capacitors. Two similar implementations use this approach: [10] and [9]. The basic structure of the phase interpolator in the first design is displayed in Figure 12. A differential control inputs  $V_{C+}$  and  $V_{C-}$  are converted to weighted currents using the differential input pair. The total current in the differential pair is  $I_{BIAS}$  as set by the current source connected to ground. Thus a total current of  $I_{BIAS}$  is directed into the phase comparator block. The current in each branch feeding the phase mixer is weighted based on the differential input voltage  $V_C$ . The input waveforms are to be interpolated are fed into the phase mixer block and control switches that switch the current from the external bias sources. The currents are steered into the load



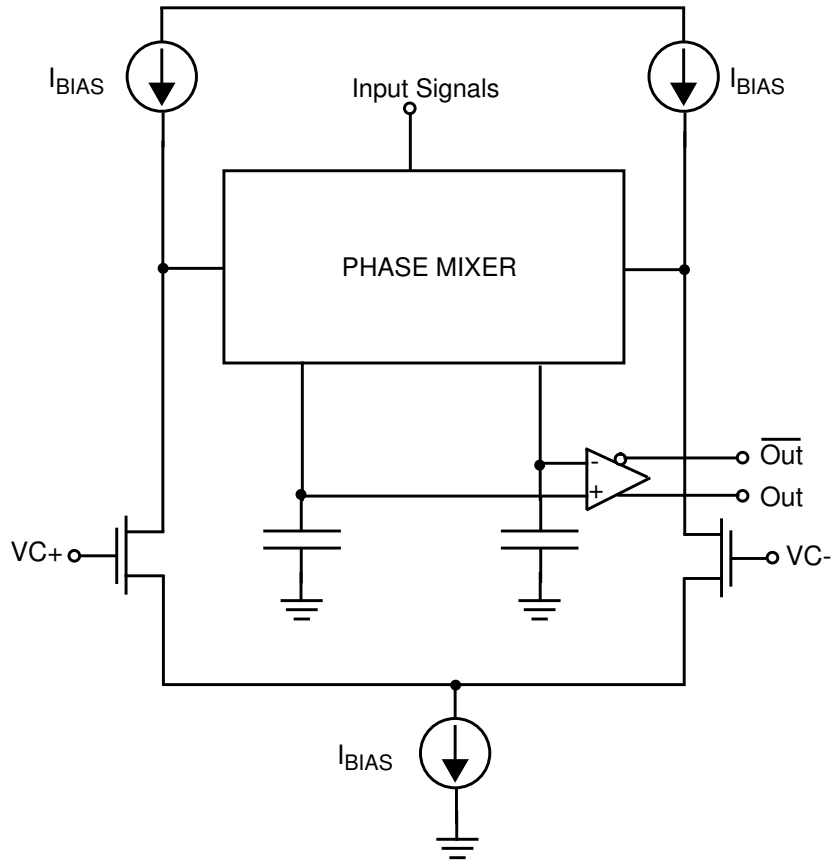


Figure 12: Simplified schematic of current integration phase interpolator

capacitors, which integrated the current and are in turn sensed by a comparator.

The detailed schematic is displayed in Figure 13. This phase interpolator is part of a system that generates an arbitrary phase shift of an input signal. The input signal is first buffer in a delay line to create  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$  phases. Two of these phases are fed into the phase interpolator based on which phase quadrant the desired output phase is situated. Thus the inputs  $I$ ,  $Q$ ,  $\bar{I}$ , and  $\bar{Q}$  are the  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$  phase signals, respectively. The  $I_{sel}$ ,  $\bar{I}_{sel}$ ,  $Q_{sel}$ ,  $\bar{Q}_{sel}$  active lows signals control which two of the inputs are phase mixed. Essentially, the four two transistors which are controlled by  $I$  and  $\bar{I}$  (and similarly for the  $Q$  and  $\bar{Q}$  transistors) form a pair of differential pairs. The difference between the pairs is polarity of the connections. Only one of each pair is enabled at any one time as controlled by  $I_{sel}$  and  $\bar{I}_{sel}$ . If the select inputs  $I_{sel}$  and  $Q_{sel}$  are chose and fixed, one can see that the phase mixing circuit is similar to the above phase mixer based on differential MCML logic. In this circuit, rather than use a resistive-type load to convert the mixed current to an output voltage, current integration is used. The differential pair outputs are used to charge capacitors and each differential pair is loaded by a current mirror. Thus any current used to charge one of the capacitors is mirrored and use to discharge the other capacitor. And by superposition the opposite is also true. Thus the voltages on the capacitors are differential. These differential voltages are sensed by a comparator which sets the risetime and falltime of the output waveform because it is slewing for most of the output time.

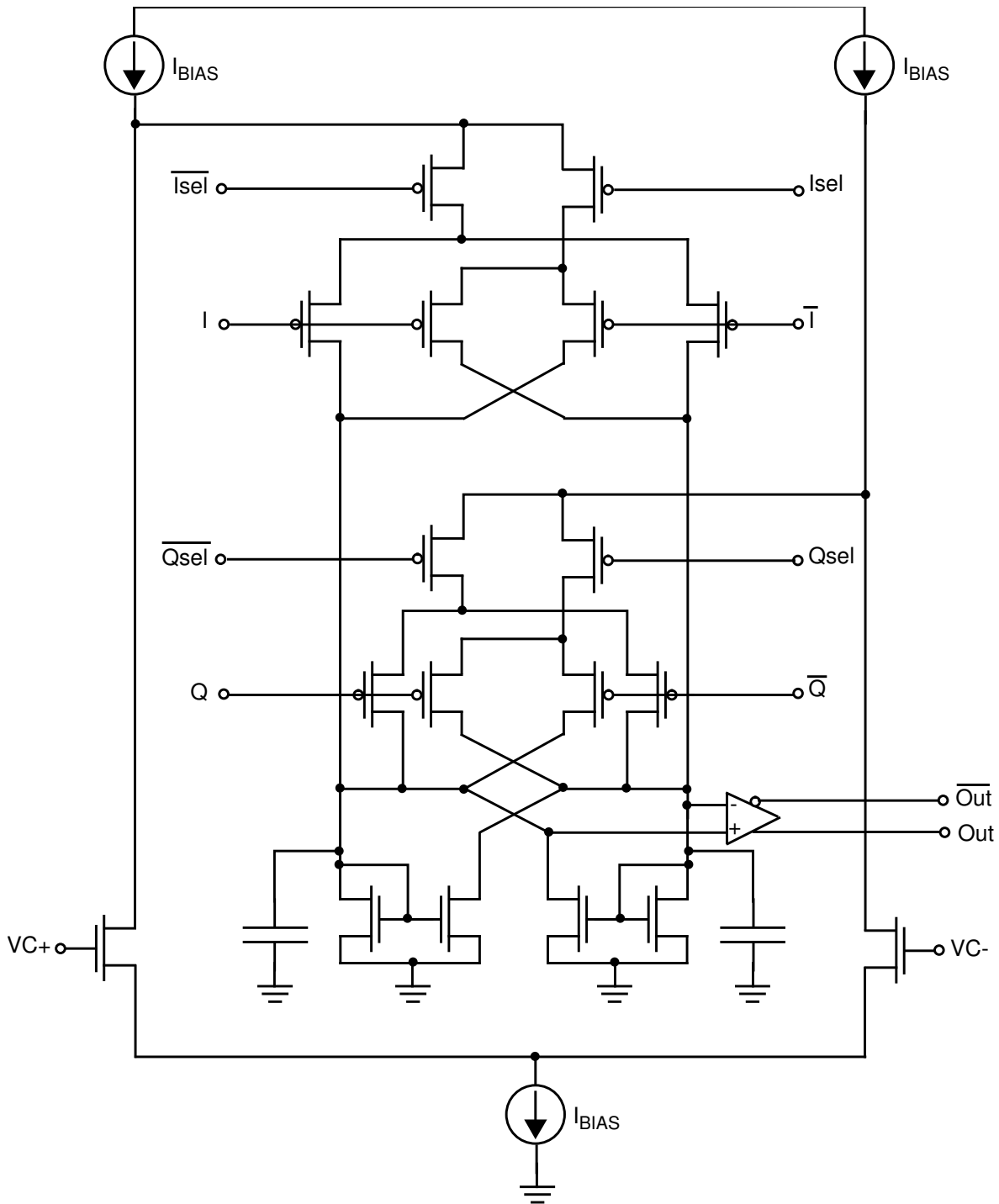


Figure 13: Current integration phase interpolator

## 4 Conclusion

Many papers and reports about designs that use phase interpolators often spend little or no space discussing the actual implementation of the phase interpolator. They seem to be an afterthought. In [2] it is observed that there is no fundamental limit to signalling rates other than Shannon's capacity limit. Thus, investigation into signalling circuitry has a high probability of positive results. As is evident from the list of references, much of the information was culled from registered patents, indicating that there is need for phase interpolating circuits. It is expected that phase interpolating circuits will be studied in more detail in both academia and in industry in the future in because as the field of high-speed signalling progresses, the performance gain from the phase interpolator will become a critical component of the overall performance.

## References

- [1] Stefanos Sidiropoulos. *High-performance inter-chip signalling*. PhD thesis, Stanford University, 1998.
- [2] Mark Horowitz, Chih-Kong Ken Yang, and Stefanos Sidiropoulos. High-speed electrical signaling: overview and limitations. *IEEE Micro*, 18(1):21–24, January-February 1998.
- [3] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, Toronto, 2001.
- [4] Patrik Larsson. A 2-1600-MHz CMOS clock recovery PLL with low-V<sub>dd</sub> capability. *IEEE Journal of Solid-State Circuits*, 34(12):1951–1960, December 1999.
- [5] Stefanos Sidiropoulos. A semidigital dual delay-locked loop. *IEEE Journal of Solid-State Circuits*, 32(11):1683–1692, November 1997.
- [6] Masayuki Mizuno, Masakazu Yamashina, Koichiro Furuta, Hiroyuki Igura, et al. A GHz MOS adaptive pipeline technique using MOS current-mode logic. *IEEE Journal of Solid-State Circuits*, 31(6):784–791, June 1996.

- [7] William J. Dally and John W. Poulton. *Digital Systems Engineering*. Cambridge University Press, 1998.
- [8] John G. Maneatis and Mark Horowitz. Precise delay generation using coupled oscillators. *IEEE Journal of Solid-State Circuits*, 28(12):1273–1282, December 1993.
- [9] Jared L. Zerbe, Grace Tsang, and Clemenz L. Protmann. Phase interpolator with noise immunity. US Patent 6,111,445, August 2000.
- [10] Thomas H. Lee, Kevin S. Donnelly, and Tary-Chyang Ho. Voltage controlled phase shifter with unlimited range. US Patent 5,554,945, September 1996.