University of Toronto

Department of Electrical and Computer Engineering

Prof. K. Phang

ECE 1352 Reading Assignment

On-Chip Image Reject Techniques for Wireless Receivers

By:

Nora Yan

Nov 12, 2001

1 Introduction

Wireless receivers can generally be divided into two categories according to their architectures. The two categories are commonly known as homodyne receivers and heterodyne receivers. In a homodyne receiver, the desired signal is first selected by a bandselect filter and then amplified by a LNA. It is then frequency translated by a mixer to DC before other baseband operations are performed on the signal. In the more popular heterodyne architecture, the signal goes through a similar receiver chain except that it is frequency translated to a lower but non-zero intermediate frequency (IF) where signal processing operations are performed. Each type of architectures has its own characteristics and presents different challenges to the designers.

This paper is a study on a number of on-chip techniques for resolving an inherent problem in heterodyne architectures. This inherent problem is referred to as image. To understand how the problem of image arises, consider the operation of a mixer as illustrated in Figure 1. A mixer can be viewed as a simple analog multiplier.

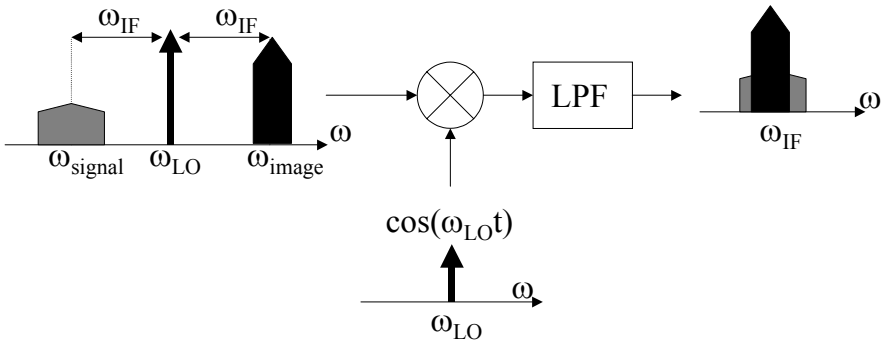

Figure 1: Operation of a mixer in a heterodyne receiver.

As shown in Figure 1, the desired band and the image band, which are located at an equal distance from either side of the local oscillator (LO) frequency, are translated to the same IF frequency. This is because the mixing operation does not preserve the polarity of the difference between its two input frequencies. In other words,

$$\cos(\omega_1 - \omega_2)t = \cos(\omega_2 - \omega_1)t \qquad \text{Equation 1-1}$$

The problem of image could cause serious distortions to the desired signal since the power of the image signal may not be regulated and can be much higher than that of the desired signal. Hence proper image rejection must be performed before the mixer stage in the receiver chain.

Different wireless standards have different specifications for image rejection but they all fall in a common range of 60 dB to 90 dB. The traditional approach for image rejection is to place an image reject filter before the mixer. Because of the high Q-factor requirement for image reject filters, off-chip Surface Acoustic Wave (SAW) filters are the conventional choice for this application. However, the use of SAW filters imposes two restrictions to a receiver design. Firstly, the LNA must drive a 50 ohm input impedance of the filter, this leads to more difficult tradeoffs between gain, NF, stability and power dissipation in the amplifier [1]. Secondly, it is an impediment to the development of fully monolithic transceivers, which are highly encouraged, as consumers of wireless products are constantly demanding for more compact systems with lower costs.

In the following sections, different on-chip image rejection techniques, at both the circuit and system levels, will be discussed.

2 Image reject mixer structure

Image reject mixers, namely the Hartley architecture and the Weaver Architecture are the most well known methods for implementing image rejection structures. Although they have been introduced decades ago, the achievable image rejection ratio for these architectures has been limited to 30 to 35dB. This is because, these structures are highly sensitive to mismatches in the circuit.

Before studying these two different architectures, it is important to understand a 90-degree shift operation, since this is used in both architectures. A 90 degree shift operation, in the time domain, converts sinωt to -cosωt and cosωt to sinωt. In the frequency domain, this operation is equivalent to multiplying the spectrum by G(ω) = -j sgn(ω). Figure 2 shows an illustration of such an operation in both the time and frequency domain for a sinωt signal. It is shown that for a real signal, the shifted version remains real but different phase changes are experienced at negative and positive frequencies.

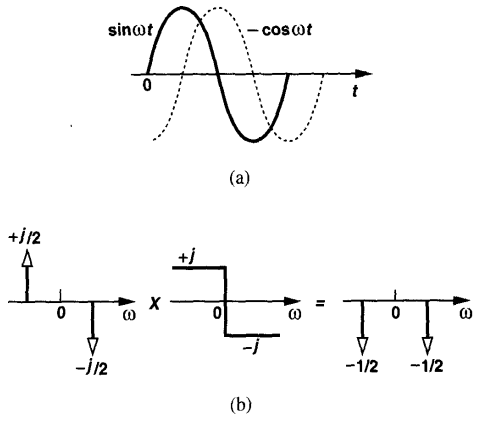

Figure 2: 90° shift operation on sin(ωt) in (a) time domain and (b) frequency domain[1].

Shown in Figure 3 is a RC-CR network that is often utilized for a 90-degree shift. For a sinusoidal input with frequency ω, the phase shifts of $V_{out1}(t)$ and $V_{out2}(t)$ are equal to $\pi/2 - \tan^{-1}(RC\omega)$ and $-\tan^{-1}(RC\omega)$ respectively. Hence, $V_{out1}(t)$ and $V_{out2}(t)$ have a phase difference of 90 degree at all frequency.

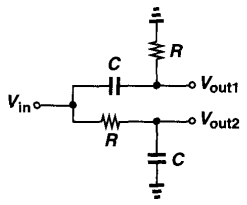

Figure 3: RC-CR network for a 90° shift operation[1].

2.1 Hartley Architecture

A Hartley image-reject structure is illustrated in Figure 4. The RF input signal is first mixed with the quadrature phases of the local oscillator, $\sin\omega_{LO}t$ and $\cos\omega_{LO}t$. It is then low pass filtered. One side of the signal then experiences a 90 degree shift, the signals from both branches are subsequently added together.

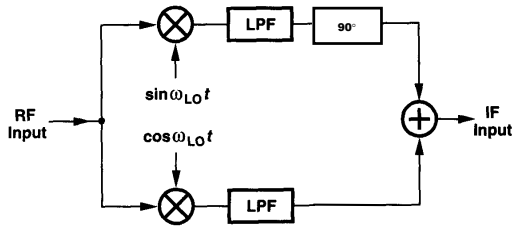

Figure 4: Hartley image-reject architecture [1].

The idea behind this structure is to distinguish the signals at positive and negative frequencies. Hence when the signals from the two branches are added together, the unwanted signal is cancelled and the wanted signal is maintained. In reality, the Hartley structure is often implemented as in Figure 5, where the signals after the low pass filter at the two branches experience a +45 and -45 phase change.

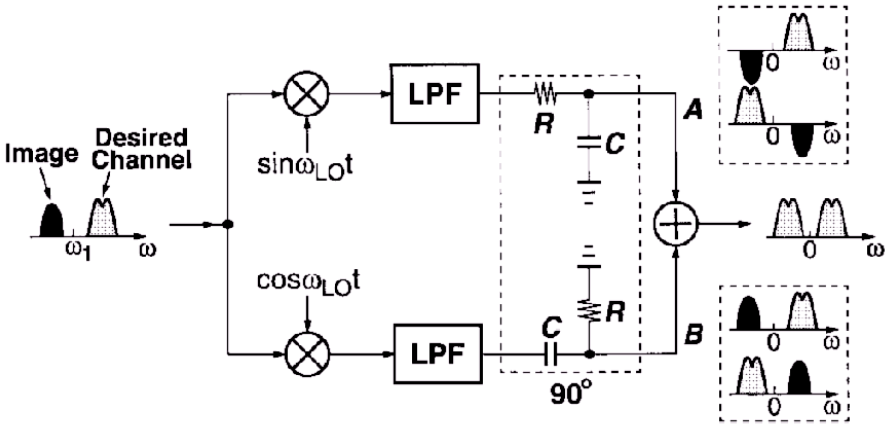

Figure 5: Practical implementation of a Hartley image reject structure [2].

A major drawback of the Hartley structure is that it is very sensitive to mismatches in the gain and phase of the two signal paths. Also, mismatches between the quadrature phases of the LO can strongly degraded the effectiveness of the image reject structure. In [1], a relationship between the image rejection ratio (IRR) and the phase and gain mismatches between the LO quadrature signals is given. IRR is defined as

$$IRR = \frac{P_{im}}{P_{sig}}\bigg|_{out} * \frac{A^2{}_{sig}}{A^2{}_{im}}\bigg|_{in} \qquad \text{Equation 2-1}$$

$$IRR = \frac{(\Delta A / A)^2 + \theta^2}{4} \qquad \text{Equation 2-2}$$

Where P_{im} and P_{sig} are the average power of the image and desired signal; A^2_{im}/A^2_{sig} is the image-to-signal ratio. $\Delta A/A$ is defined as the relative gain mismatch and θ is the phase imbalance in radian of the LO quadrature signals. Although $\Delta A/A$ and θ are derived using only the gain and phase mismatch of the LO signals. It may also include small mismatches in the mixers, low pass filters, the two ports of the adder, and additional mismatches due the 90 degree shift operation. In [1], it is also shown that

$$\frac{\Delta A}{A} \approx \frac{\Delta R}{R} + \frac{\Delta C}{C} \qquad \text{Equation 2-3}$$

Where $\Delta R/R$ and $\Delta C/C$ denote the relative gain mismatch between the resistors and the capacitors respectively in a RC-CR network.

Figure 6 shows the relationship of image rejection versus amplitude and phase errors in quadrature signals. It can be seen that for an image rejection of 40dB, the amplitude and phase mismatch must be kept within 0.1dB and 1° respectively.

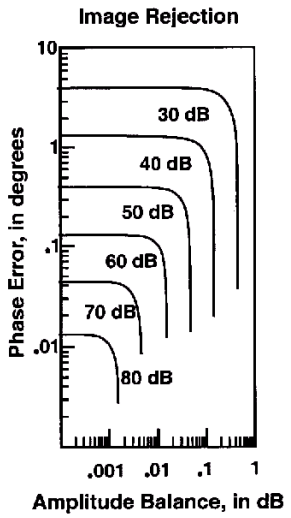

Figure 6: Image rejection vs. amplitude and phase mismatches in quadrature signals [3].

2.2 Weaver Architecture

Figure 7 shows a Weaver image-reject mixer. The main difference from the Hartley architecture is that the 90-degree shift stage is replaced by a second quadrature mixing stage in the Weaver architecture.

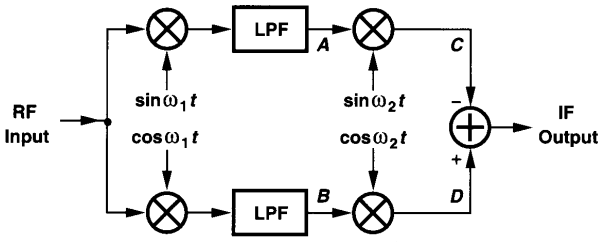

Figure 7: Weaver image reject architecture [1].

Refer to Figure 8 for a graphical analysis of the Weaver architecture. In the Weaver architecture, the signals after the second mixer from both branches are subtracted from each other. The reason for this is apparent from Figure 8.

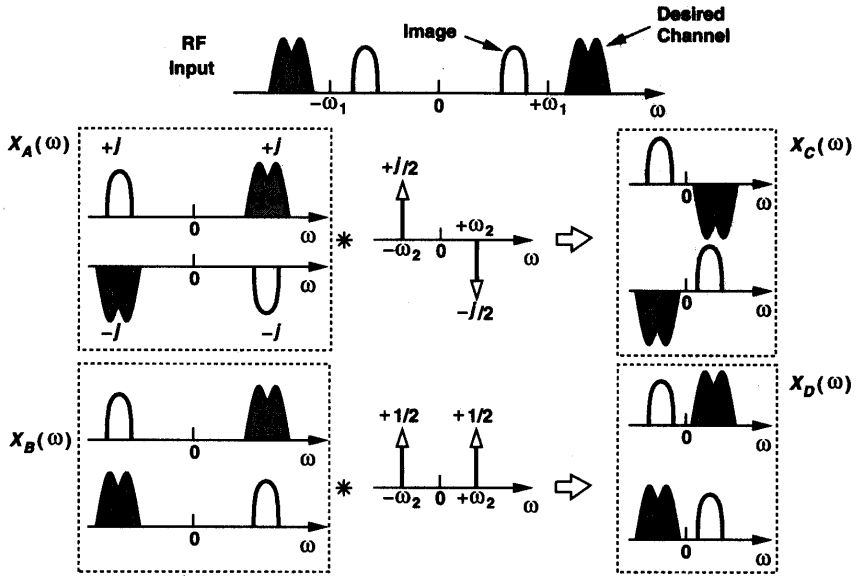

Figure 8: Graphical analysis of the Weaver architecture [1].

By replacing the RC-CR structure, the Weaver architecture is not susceptible to IRR degradation that may arise from gain imbalances in the RC-CR structure. However, it introduces the problem of a secondary image, if the second mixer translates the spectrum to a nonzero frequency. Figure 9 explains the problem of secondary image in Weaver architecture.

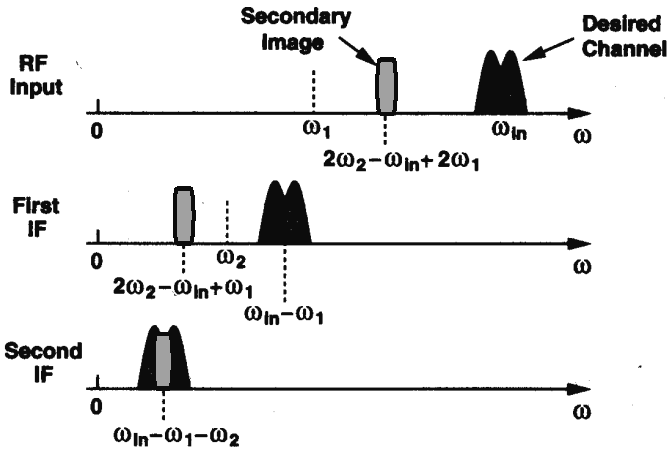

Figure 9: Secondary image in Weaver architecture [1].

Similar to the Hartley architecture, the Weaver architecture is also sensitive to mismatches in phase and gain of the LO quadrature signals.

3 On-Chip notch filter

As discussed in Section 2, image reject mixers can typically provide an image rejection ratio of 30-35dB, which is still far from the 60-90dB of image rejection required by the different wireless standards. This implies that, off-chip image reject filters are still needed in conjunction with the above image-reject mixer structures to enhance image rejection. Therefore, in order to build fully monolithic receivers, on-chip image-reject filters or more advanced image-reject techniques must be developed.

3.1 Active notch filter

In [4], a monolithic active notch has been designed for the purpose of image rejection. The design of this circuit has been made possible by the availability of monolithic inductors. This notch filter can provide an image rejection of more than 50dB and is suitable for integration with an LNA and a mixer. It can also be utilized in conjunction with an image reject mixer as discussed in Section 2, to obtain a decent 80dB of image rejection.

The design of this active notch filter is based on a series resonator, whose resonant frequency is tuned to that of the image frequency. Figure 10 shows the series resonator circuit.

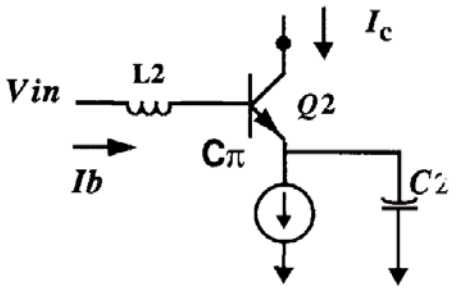

Figure 10: Series resonator [4].

The impedance looking into the base of Q2 is given by [4]:

$$Zb = \frac{1}{j\omega} * (\frac{1}{C\pi} + \frac{1}{C2}) - \frac{g_m}{w^2 * C\pi * C2} \qquad \text{Equation 3-1}$$

Where Cπ and g_m is the emitter-base capacitance and the transconductance of Q2 respectively. From Eq 3-1, it can be seen that the input impedance of the series resonator is:

$$Zin = Zb + j\omega L2 \qquad \text{Equation 3-2}$$

L2 is a monolithic inductor with a Q of 5 at 2GHz. The series resonator is formed by L2 and the series combination of Cπ and C2. Hence the notch frequency is expressed as:

$$fnotch = \frac{1}{2\pi\sqrt{L2 * \frac{C\pi * C2}{C\pi + C2}}} \qquad \text{Equation 3-3}$$

One attractive characteristic of this active filter is that its Q factor can be tuned by the DC current flowing through Q2. This can be noted from the last term in Eq 3-1, this term can be viewed as a negative resistance that compensates for the resistive losses of inductor L2. Hence the Q factor of this notch filter can be made very high, resulting in a high rejection ratio.

Figure 11 shows the series resonator integrated with a cascode amplifier made of Q1 and Q3. The amplifier is tuned to the carrier frequency of 1.9GHz using the LC tank. The series resonator is tuned to the image frequency of 2.5GHz by using the appropriate L2 and C2 value. As a result the image signal sees almost zero impedance at the emitter of Q3. Therefore, rejecting the image signal since the entire image signal current from Q1 is shunted.

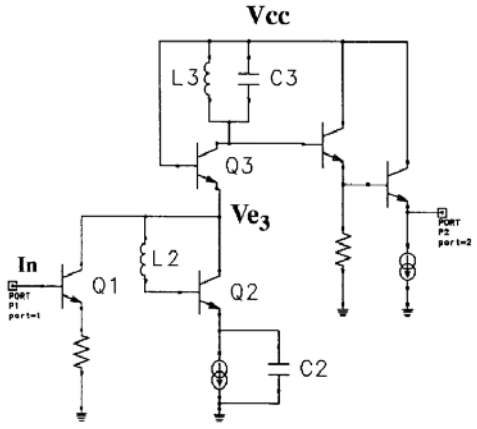

Figure 11: Active image reject filter with cascode amplifier [4].

In [5], an improvement to the above circuit is made. This improvement allows the image reject filter to have a tunable resonant frequency range of 230MHz by using a varactor with a control voltage of 0 to 3V. This tuning capability is beneficial because it can be used to offset the drift in the notch frequency due to process variation of elements and unavoidable parasitic.

3.2 Passive notch filter

In [6], a notch filter using only passive elements has been developed for the purpose of image rejection. Figure 12 shows a schematic of this passive notch filter.

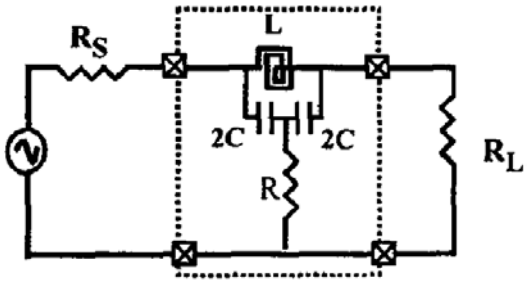

Figure 12: Passive notch filter [6].

The circuit in Figure 12 is also a resonator, whose components have been implemented using Metal-Insulator-Metal (MIM) capacitors and on-chip inductor with a Q factor of 10. This circuit has been fabricated using a matured bipolar process. One main advantage of this passive notch filter, as compared to the active notch filter in Section 3.1, is that it does not impose additional tradeoff between linearity and gain, since the filter itself is highly linear. However, also due to its passive nature, it introduces insert loss into the signal band, which can be translated into a NF degradation for a receiver.

Similar to the active notch filer in Section 3.1, the quality factor of this passive notch filter is also tunable. This is done using the resistor R in the filter. At or near the resonant frequency of this notch filter, the filter looks like Figure 13, assuming the MIM capacitors are lossless.

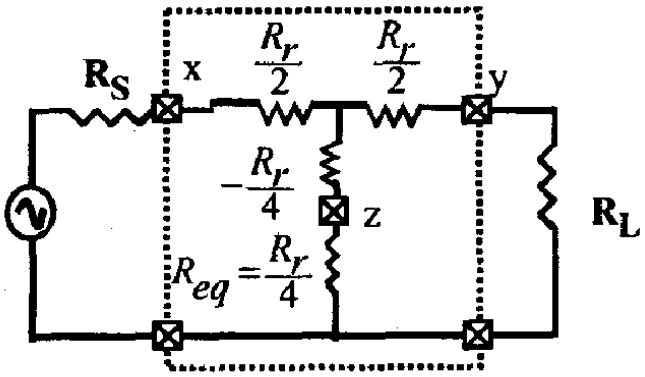

Figure 13: Equivalent notch filter near resonant frequency [6].

In Figure 13, $R_r = R_S(1+Q^2_L)$, where R_s and Q_L are the series resistance and the Q-factor of the Inductor. R_r is the resistance of the parallel LC tank at resonance. Therefore, if R is made equal to R_r, a notch with infinite rejection can ideally be achieved even with finite Q on-chip inductors. However, in a non-ideal integrated circuit, the depth of the notch can be limited by the additional inductance introduced by the connection of R to ground. Figure 14 demonstrates how the value of R can be used to tune the Q factor of this notch filter. With appropriate tuning, this filter can achieve an image rejection of over 60 dB.

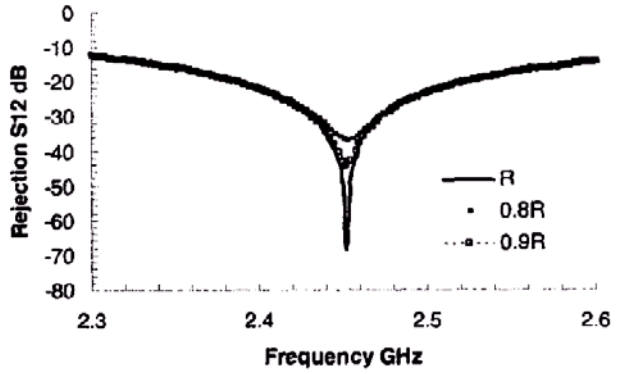

Figure 14: Depth of notch as a function of R [6].

Also, the actual notch frequency of this filter can be affected by process variation of the MIM capacitors and parasitic substrate capacitance of the components. Figure 15 shows the effect of variation of the MIM capacitors on the notch resonant frequency.

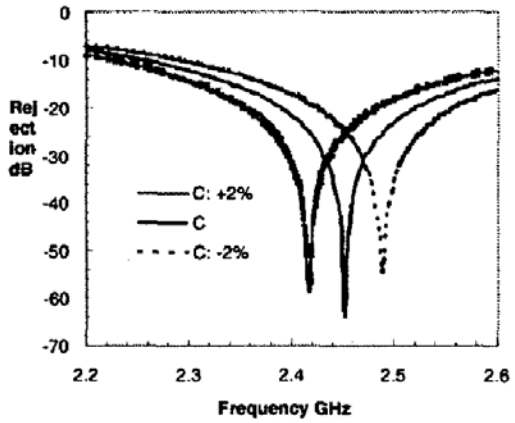

Figure 15: Notch rejection frequency as a function of capacitance values [6].

4 System level techniques

In Section 2 and 3, circuit level techniques for image rejection have been explored. In this section, an image rejection technique that is based on insightful frequency planning is discussed.

In [7], image-reject architecture achieving a 62-dB image rejection has been proposed. The novelty of this technique lies in its frequency planning, in which the IF (2.6GHz) is made equal to half of the carrier frequency (5.2GHz). This implies that the LO frequency is also equal to half of the carrier frequency and that the image lies around zero hertz. This image-reject architecture is shown in Figure 16. There are two mixing stages in this structure, after the first mixing (RF mixer), the IF signal experiences a second mixing (IF mixer) with the same LO frequency in a quadrature phase manner. This will eventually bring the signal down to zero frequency.

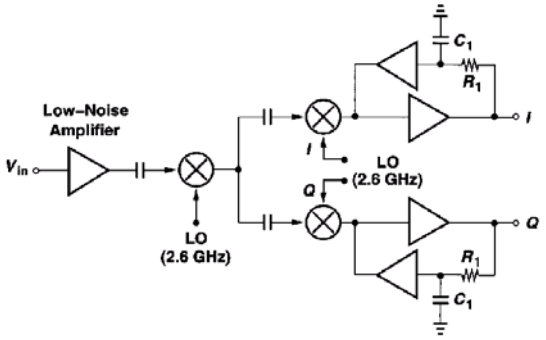

Figure 16: Image-reject architecture [7].

This architecture offers several advantages over that of conventional heterodyne or image-reject architectures. Firstly, the image band lies around the zero frequency; hence it is highly suppressed by the antenna and the RF front end. This eliminates the need for an explicit image-reject filter. Secondly, the frequency synthesizer operates at half of the input frequency, therefore imposing less stringent requirements on its oscillator and frequency divider. As a result, it can potentially generate more balanced quadrature phase LO signals. Furthermore, in this structure, one needs not to worry about LO leakage to the antenna in the 5.2 GHz band since the LO is more than 2GHz away. Finally, this architecture does not require extremely accurate phase and gain matching.

The design of the architecture in Figure 16 must indeed deal with three major issues. The first issue is due to the fact that the image frequency of the first mixing lies around the zero frequency. Although zero frequency band signal from the external world will be rejected, but the architecture is still susceptible to flicker noise (1/f noise) generated by transistors in the LNA and in the input stage of the RF mixer that is up-converted to IF. To overcome this problem, the circuit topology in Figure 17 is employed.

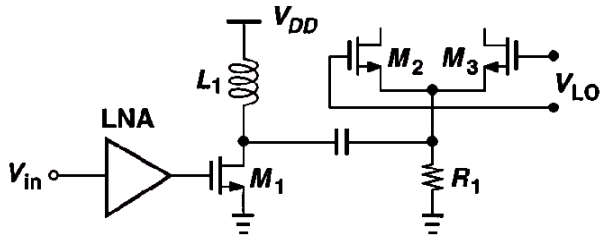

Figure 17: Circuit topology for reducing the up-conversion of flicker noise [7].

In Figure 17, a capacitor is used to couple the LNA together with the mixer's input voltage-to-current converter (M1) to the switching devices (M2, M3). Such coupling prevents the up-conversion of flicker noise from the LNA and M1 to the IF frequency.

The second issue is the LO-IF feed-through of the first mixer. This is a problem because the LO and the IF are in the same band and hence cannot be filtered by a low pass as in a conventional

heterodyne receiver. This issue, however, can be easily resolved by utilizing a double-balanced mixer.

The third issue is related to the linearity of the second mixer. Because of the high IF, it is not possible to perform channel-selection filtering at the IF (a very high Q filter is needed). As a result, high linearity is required in the second mixer. Figure 18 shows the IF mixer and baseband amplifier of the receiver.

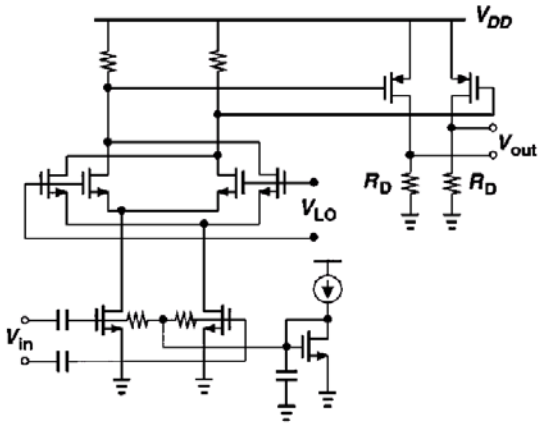

Figure 18: Schematic of the IF mixer and the baseband amplifier [7].

In this design, the gain of the baseband amplifier is traded with its linearity. It has a high linearity of +18dBm, which limits its gain to 15dB in a 2.5V supply. Tradeoff between the linearity and the gain of this P-MOS differential amplifier stage can be studied by noting the following relationships:

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}} \qquad \text{Equation 4-1}$$

$$R_D = \frac{V_{RD}}{I_D} \qquad \text{Equation 4-2}$$

Where V_{RD} is the voltage drop across R_D. Combining Eq 4-1 and 4-2 gives:

$$g_m R_D = \frac{2V_{RD}}{V_{GS} - V_{TH}} \qquad \text{Equation 4-3}$$

In Equation 4-3, a relationship between gain (g_mR_D), linearity (V_{GS}-V_{TH}) and voltage headroom (V_{RD}) is developed. It can be clearly seen that for high linearity (large V_{GS}-V_{TH}) and a larger head room (small V_{RD}), the gain must be made small.

Although this architecture has demonstrated a promising image rejection of 62-dB without the explicit use of an image reject filter, the design of this architecture is faced with numerous challenges. In addition to the three major issues discussed above, this structure needs to resolve the problem of offset, which is a common issue in homodyne receivers. The offset problem is due to the self-mixing of the LO in the IF mixers and the LO-IF feedthrough in the RF mixer. The amount of offset can add up to tens of millivolts, which could significantly degrade the linearity of the baseband amplifier and other subsequent stages. Hence, offset cancellation circuits have been put into place to improve the offset issue, which adds to the complexity of the receiver.

5 Conclusion

In this paper, it is demonstrated that the techniques for image rejection in heterodyne receivers have been constantly evolving. This evolution is strongly urged by the tremendous success and extensive popularity of wireless products in recent years. On-chip image rejection techniques are not only important for smaller and less expensive wireless products, they are also essential for the advent of exciting technology like System-On-Chip (SoC).

Three groups of image-rejection technique are discussed: 1) image reject mixer architectures 2) active and passive on-chip notch filter structures, and 3) system level and frequency planning for reduced image corruption. Each group of techniques has its own advantages, drawbacks and is subject to different tradeoff conditions.

Among the various techniques, the on-chip notch filters might become the choice for future image rejection scheme. This is because as semiconductor process advances, high Q-factor

inductors and tight process controlled MIM capacitors might become available. These advances are all in favor of on-chip notch filter development. Moreover, the passive notch filter is very attractive for it has a very simple structure and does not cost any linearity tradeoff and circuit overhead. However, it must be noted that for both active and passive notch filter structures, tuning of the Q-factor and the notch frequency will be needed. This will increase manufacturing cost.

Another potential implementation for image rejection in the future, is a combined usage of a Hartley or Weaver architecture with an on-chip notch filter.

The architecture in [7] has shown promising result; however, it requires too much circuit overheads. Hence, it may not be the choice of future image rejection technique.

Reference

[1] B. Razavi, *RF Microelectronics*, Upper Saddle River: Prentice Hall, 1998.

[2] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2178-2185, December 1998.

[3] J.P. Maligeorgos and J.R. Long, "A Low-Voltage 5.1 - 5.8-GHz Image-Reject Receiver with Wide Dynamic Range", *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1917-1926, December 2000.

[4] J. Macedo, M. Copeland and P. Schvan, "A 2.5GHz Monolithic Silicon Image Reject Filter", *IEEE 1996 Custom Integrated Circuits Conference*, pp. 193-196, 1996.

[5] J.A. Macedo and M.A. Copeland, "A 1.9-GHz Silicon Receiver with Monolithic Image Filtering", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 3, pp. 378-386, March 1998.

[6] B. Ray, J.S. Hamel, T. Manku and J.J. Nisbet, "A Highly Selective Passive Band Reject Filter with Low-Q Lumped Elements in a Si Bipolar Process", *IEEE BCTM*, 2000.

[7] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection", *IEEE Journal of Solid-State Circuits*, vol. 36, no. 5, pp. 810-815, May 2001.