Noise Analysis of Phase Locked Loops and System Trade-offs

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ABSTRACT

This report analyzes phase locked loops from the noise point of view and discusses the different trade-offs in designing low noise PLLs. Beginning with a first order loop, the importance of loopbandwidth is explained. It is shown that the loopbandwidth basically acts as a threshold when the VCO noise begins to dominate over the input noise. Higher order loops are also analyzed to show that two basic PLL parameters: the charge pump gain and the resistance in the loop filter can be varied for reducing the noise level at the output. However, variation of these parameters disturb stability and frequency spectrum of the PLL. Trade-offs in varying these parameters are discussed and a step by step PLL design procedure is described that improves the noise performance of the PLL while maintaining good stability and reduced reference spurs in the output power spectrum.

1.0 Introduction

Phase locked loops (PLL) [1] are used to maintain a well defined phase and hence frequency relation between two independent signal sources. Due to their versatility, PLLs are usually preferred over other methods of maintaining phase lock, such as injection locking [2]. Monolithic phase locked loops have been used in data communication circuits for clock recovery generation, in microprocessors to generate a low skew/jitter clock across the chip and in RF applications as frequency synthesizers to produce a digitally controlla-

ble stable high frequency source from a low frequency reference such as a crystal oscillator.

Fig. 1 shows a general PLL consisting of a phase detector (PD), a loop filter with transfer function H(s), a voltage controlled oscillator (VCO) and a frequency divider denoted as 1/N. The PD generates an output proportional to the phase difference between its two inputs. The first input, Vin, is usually generated by an external oscillator, while the second input is directly related to the output of the VCO, Vout. Under locked condition the negative feedback adjusts the dc value of the VCO control voltage in such a way that the two inputs of the phase detector have a constant phase difference and hence are exactly at the same frequencies. This occurs when the VCO output frequency, *fo* is N times the input frequency.

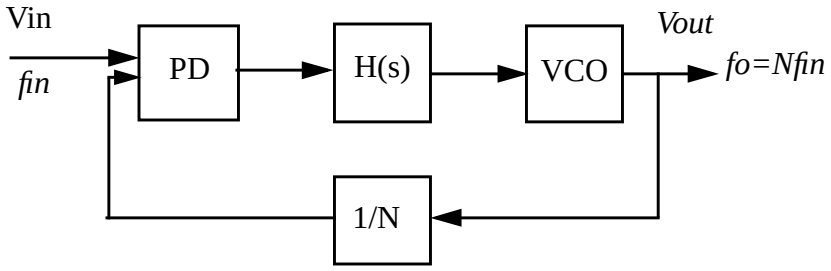

FIGURE 1. Block diagram of typical phase locked loop.

Although proper choice of PLL parameters will ensure that the PLL locks to an integer multiple of the input frequency, noise sources in the circuit cause perturbations in the VCO control voltage, resulting in variations in output frequency. Hence the output power spectrum will contain other frequency components in the vicinity of fo. This phenomenon is shown in Fig. 2(a), where the output spectrum exhibits ‘skirts’ around fo. The ratio of

the output power at a frequency offset Δf to the power at *fo* is defined as *phase noise*. In the time domain, the noise sources disturb the regularity in zero crossings of the output signal causing it to exhibit jitter. Due to negative feedback, the PLL inherently corrects the drift in output frequency thus limiting the jitter. As a result, the jitter cannot increase definitely with time as in open loop oscillators. However, noise sources at different points in the PLL dominate at different offset frequencies, thus complicating the PLL design for low noise.

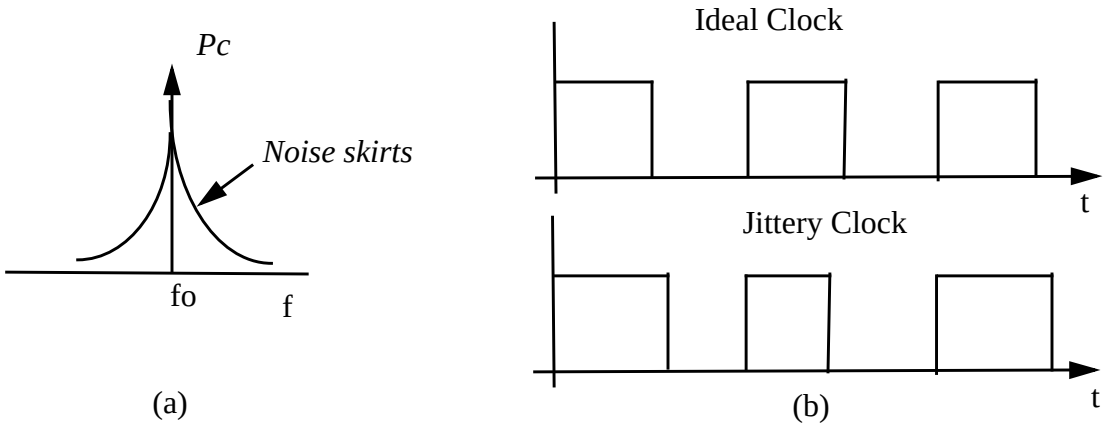

FIGURE 2. Frequency and time domain effects of noise sources in PLLs. (a) Phase noise in output power spectrum. (b) Jitter in time domain.

This report discusses the trade-off in designing PLLs such that they exhibit minimum phase noise and jitter. Section2 particularly focuses on the individual noise properties of different building blocks. Section 3 analyzes a first order PLL and defines the fundamental trade off in PLL design with respect to the loop bandwidth. Section 4 extends the analysis to higher order loops and elaborates on typical design trade-off. Section 5 focuses on a step by step PLL design procedure that meets all trade-off in PLL design.

2.0 Noise Properties of PLL Building Blocks

This section investigates the noise properties of different PLL building blocks.

2.1 Oscillator Noise

There are two oscillators that contribute to the phase noise of the PLL: one is the reference oscillator and the other is the VCO. Although both oscillators can be modeled similarly, it will be evident later that their effects on the output noise are distinct just due to their position in the loop.

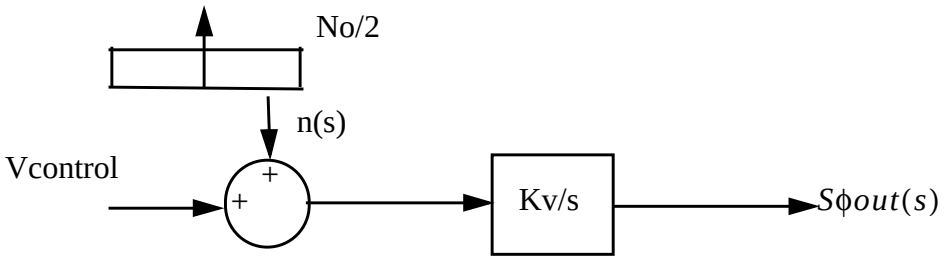

FIGURE 3. Noise model for the VCO

A VCO can be modeled as a noiseless VCO which has an additive white noise at the input as shown in Fig. 3 where n(s) is a white noise source with a double sideband power spectral density of No/2. The output power spectrum can be expressed as [3],

$$S\phi out(\omega) = \left|\frac{Kv}{j\omega}\right|^2 Sin(\omega) = Kv^2 \frac{No}{2\omega^2} \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where Kv is the VCO gain in Hz/V. Although this is a very simplified model and only considers the $1/f^2$ behavior of the VCO it is sufficient to predict the output noise of the PLL in the presence of VCO noise. The reference oscillator is assumed to have a similar behavior but the constant of proportionality will be different [4].

2.2 Frequency Divider Noise

The excess noise of a digital divider can be modeled as an additive noise source at its output. In a PLL this noise usually appears directly at the input of the phase detector and experiences the same transfer function as the noise on the input terminal. This effect will become clear in Section 4.

2.3 Phase Detector Noise

Usually phase detectors are not a major source of noise in PLLs [4]. Their noise properties have been studied to some extent in [5].

3.0 Noise Analysis of First Order PLLs

For a first order loop, no exploit filter H(s) exists and the PD is usually implemented using an analog multiplier or an XOR gate. Assuming no divider, the closed loop phase transfer function of the 1st order loop with a PD gain of Kp volts/rad. can be expressed as,

$$\frac{\phi out(s)}{\phi in(s)} = \frac{K}{K+s} = \frac{1}{1+\frac{s}{\omega loop}} \quad \ldots\ldots\ldots\ldots (2)$$

where the loop bandwidth, $\omega loop$=K=KpKv. The loopbandwidth is defined as the -3 dB frequency of the closed loop transfer function (or the unity gain frequency of the for-

ward transfer function). The block diagram of the 1st order loop with noise sources is shown in Fig. 4.

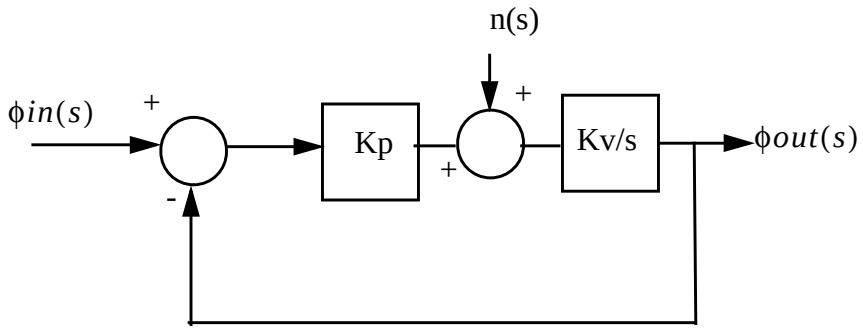

FIGURE 4. Block diagram of first order PLL with noise sources

Assuming an ideal phase detector, the two noise sources in the circuit are the VCO and the reference input. The phase noise at the output can be calculated using superposition. Assuming a noiseless input, the effect of VCO phase noise can be calculated using the transfer function from n(s) to $\phi out(s)$, which is

$$\frac{\phi out(s)}{n(s)} = \frac{Kv}{KpKv + s} \quad \ldots\ldots\ldots (3)$$

Consequently, the output phase noise due to VCO phase noise only can be expressed as,

$$S\phi out(\omega) = \frac{No}{2}\left|\frac{\phi out(s)}{n(s)}\right|^2 = \frac{NoKv^2}{2\left(Kp^2Kv^2 + \omega^2\right)} \quad \ldots\ldots\ldots (4)$$

Comparing equation (1) and (4), it is evident that the phase noise of the PLL output is the same as the phase noise of the VCO for offset frequencies larger than $\omega loop$. This is because the PLL is unable to react fast enough to fast random changes in the VCO output and hence they directly appear on the output. At low offset frequencies, the PLL compen-

sates the slow random variations produced by the VCO noise at the output by adjusting the VCO control voltage and thus suppresses the VCO noise. These effects are shown in Fig. 5.

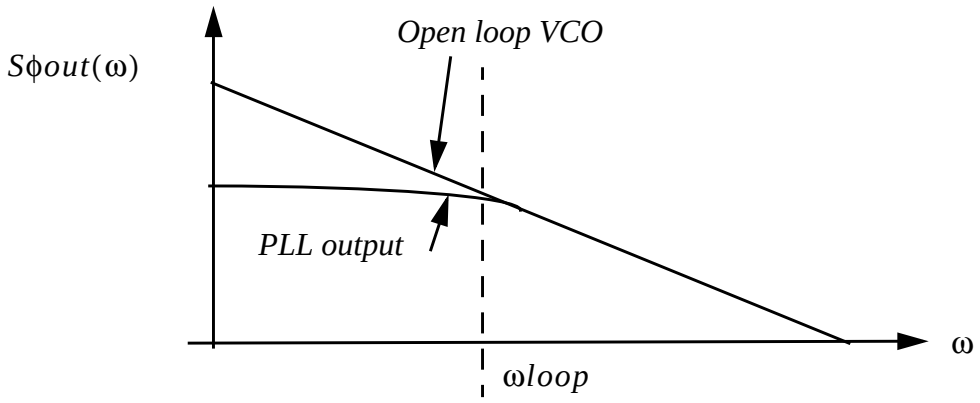

FIGURE 5. Output phase noise spectrum with a noiseless input.

Now assuming a noiseless VCO, the response of the loop to the phase variations in the input is considered. The input is usually another oscillator which will have its own phase noise characteristics. Taking into account only the phase noise in the $1/f^2$ region, its power spectrum can be written as,

$$S\phi_{in}(\omega) = \frac{\alpha}{\omega^2} \quad \ldots\ldots\ldots\ldots\ldots (5)$$

The power spectrum at the output can be easily calculated as,

$$S\phi_{out}(\omega) = \frac{\alpha K_p^2 K_v^2}{\omega^2\left(K_p^2 K_v^2 + \omega^2\right)} \quad \ldots\ldots\ldots (6)$$

which is depicted in Fig. 6.

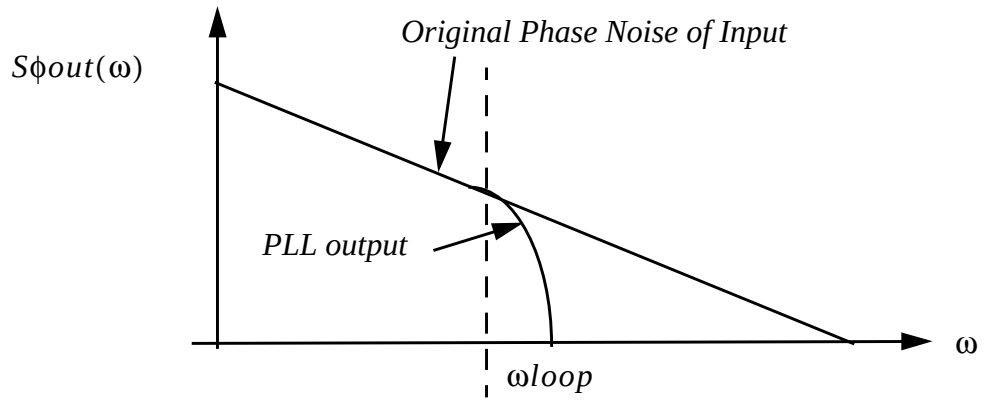

FIGURE 6. Output phase noise spectrum with a noise less VCO

If the two noise sources in the PLL are combined we obtain the phase noise plot of Fig. 7. The plot reveals a fundamental property of the PLL: its phase noise is dominated by the input source noise at frequency offsets below the loop bandwidth and by the VCO noise at frequency offsets above the loop bandwidth. Thus a PLL having a noisy VCO and a clean reference input should be designed to have a large loop bandwidth. But the loop bandwidth is inversely related to the PLL settling time [6]. Consequently, if the loop bandwidth is large, the PLL takes little time for locking and has a large noise reduction of the internal VCO noise, but cannot have a good suppression of the external input noise. If, however, the loopbandwidth is small, the PLL can have large input jitter reduction, but takes longer time for locking and leaves much of the internal VCO noise unreduced. The proper choice of the loop bandwidth depends on the particular application. For frequency synthesizers, the reference input is clean and hence the loop bandwidth should be chosen to be large to suppress the VCO noise. For clock recovery circuits, the input is random data and hence the loop bandwidth should be chosen to be small to suppress the input noise, provided that the VCO is well designed for minimum noise.

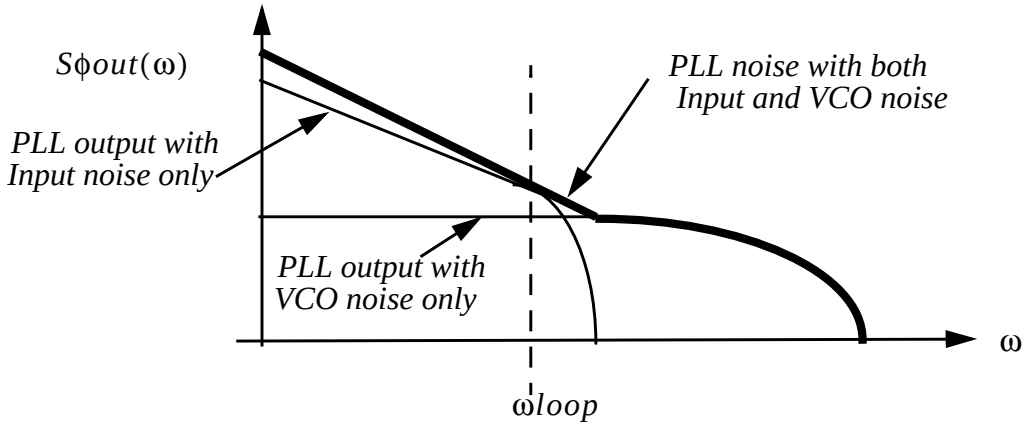

FIGURE 7. Phase noise plot of first order loop including Input and VCO noise.

4.0 Noise Analysis for Higher Order Loops

Higher order PLLs employ phase frequency detectors (PFD), charge pumps and loop filters to ensure zero static phase error which is a problem in first order loops. Fig. 8 shows the main noise contributors in such PLLs [7].

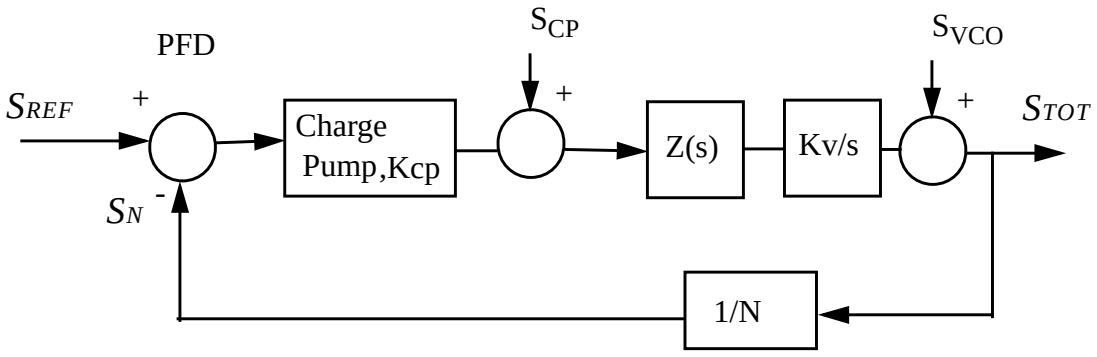

FIGURE 8. PLL phase noise contributors.

Here S_{REF} is defined as the noise power that appears on the reference input to the PD, Sn is the noise power due to the feedback divider appearing at the frequency input to the PD, S_{CP} is the noise power due to the charge pump and PFD and S_{VCO} is the noise power of the VCO. Assuming uncorrelated sources, all the effects at the output are added in an rms fashion to give the total noise of the system:

$$S_{TOT} = X^2 + Y^2 + Z^2 \ldots\ldots\ldots(7)$$

where S_{TOT} is the total noise power at the output, X^2 is the noise power at the output due to S_N and S_{REF}, Y^2 is the noise power at the output due to S_{CP} and Z^2 is the noise power at the output due to S_{VCO}. As derived in the previous section, the contribution of each noise source to the output depends on the transfer function from that noise to the output. Thus,

$$X^2 = (S_{REF} + S_N)\left(\frac{G}{1+GH}\right)^2 \ldots\ldots\ldots(8)$$

where the forward transfer function, $G=K_{CP}K_{VCO}Z(s)/N$ and the transfer function of the feedback loop, $H=1/N$. At frequency offsets lower than the loop bandwidth, $G>>1$, and thus

$$X^2 = (S_{REF} + S_N)(N)^2 \ldots\ldots\ldots(9)$$

At offsets larger than the loop bandwidth, $G<<1$ and hence $X^2=0$. Thus S_{REF} and S_N is low pass filtered by the loop.

The overall noise contribution due to the charge pump and phase detector noise,SCP can be calculated by referencing S_{CP} back to the input of the PFD. The equivalent noise power at the PFD input is S_{CP}/K_{CP}^2. This is then multiplied by the closed loop. Hence

$$Y^2 = S_{CP}\left(\frac{1}{K_{CP}}\right)^2\left(\frac{G}{1+GH}\right)^2 \ldots\ldots\ldots(10)$$

Comparing equation (10) with (8) it is evident that S_{CP} is also low pass filtered by the loop. Finally the phase noise contribution of the VCO noise to the output can be expressed as,

$$Z^2 = S_{VCO}\left(\frac{1}{1+GH}\right)^2 \ldots\ldots\ldots(11)$$

Thus the VCO noise is high pass filtered by the loop since G is low pass. To summarize, the dominant contributors to the output phase noise response at offsets lower than the loop bandwidth are the reference oscillator noise, frequency divider noise and the charge pump noise. Thus by using a clean reference oscillator (such as a crystal oscillator), a large charge pump gain and a low frequency divider ratio, the phase noise and jitter at the PLL output can be reduced at low frequency offsets. However, since N programs the output frequency, it is not generally available as a factor in noise reduction. Increasing the charge pump gain will reduce the phase noise and make the PLL step response faster, but it has its own drawbacks too. In locked condition, the charge pump does not inject any net current to the loop filter ideally. But due to mismatch between the components of the charge pump, a small net current flows to the loop filter thus affecting the control voltage of the VCO resulting in a shift in VCO frequency. This will produce a phase error at the input of the charge pump due to the negative feedback in the loop. Hence the charge pump

will inject a corrective pulse of current to bring the VCO frequency back to its previous value. Once this is accomplished, the above process repeats itself. Thus the VCO frequency toggles between two values under the locked condition. In other words, the control voltage will possess ripples even after the PLL attains lock. In the frequency domain, this effect will produce spurs at the reference frequency or multiples of the reference frequency. The magnitude of these spurs is directly proportional to the ripple in the control voltage and hence the charge pump gain. Reference spurs (Fig. 9) should be at least 50dB below the PLL output frequency to ensure a clean spectrum. This in turn limits the increase in charge pump gain to achieve low phase noise at frequency offsets lower than the loop bandwidth.

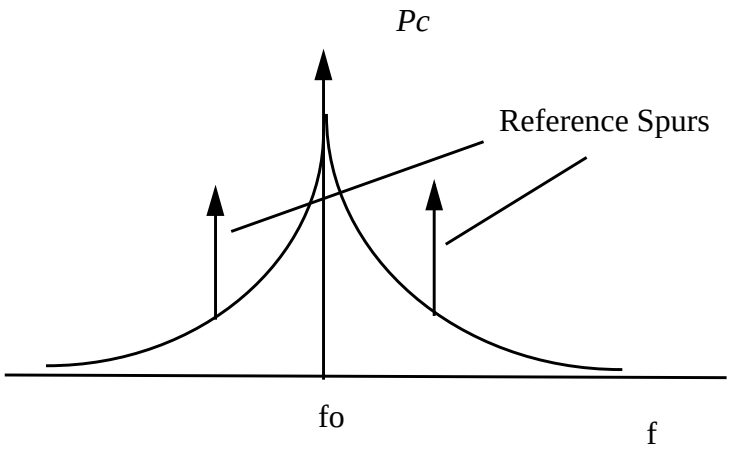

FIGURE 9. Reference spurs in the output power spectrum.

Finally, at frequency offsets larger than the loop bandwidth, the main contributor is the VCO noise. To gather more insight into the VCO noise, a third order Type II PLL, which is the most common PLL topology in monolithic high frequency circuits is considered (Fig. 10).

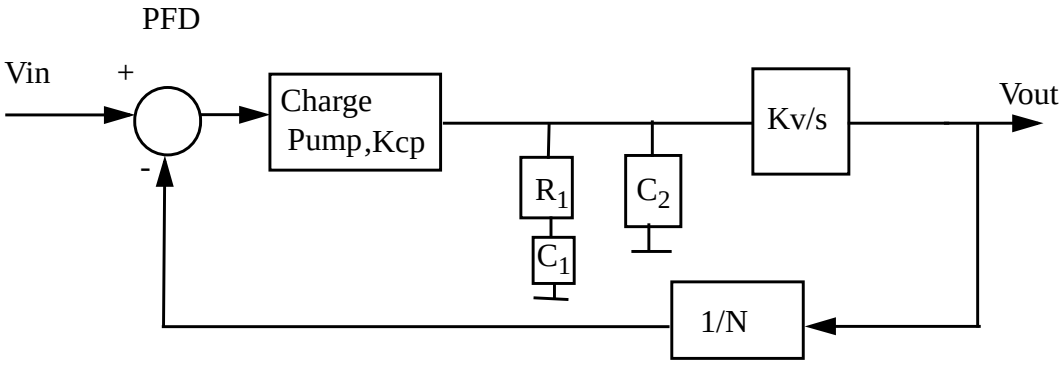

FIGURE 10. Third order Type II PLL

The main part of the VCO noise comes from the thermal noise produced by the resistance R_1 in the loop filter [8]. The thermal noise on the control voltage per unit bandwidth can be approximated as,

$$Vn^2 = \left(\frac{1}{1+\frac{C_2}{C_1}}\right)^2 \left(\frac{1}{1+\frac{R_1 C_2}{1+\frac{C_2}{C_1}}}\right)^2 V_{nR1}^2 \ldots\ldots\ldots (11)$$

where V_{nR1}^2 denotes the double sideband noise density of R1(=2kTR1). Approximating the noise per unit bandwidth in (1) by a sinusoid and using narrow band frequency modulation theory, the output relative phase noise per unit bandwidth at an offset $\Delta\omega$ can be expressed as [8],

$$\frac{Pn}{Pc} = 10\log\left(\left(\frac{C_1}{C_1+C_2}\right)^2\left(\frac{2KTR_1}{1+\left(R_1\frac{C_1C_2}{C_1+C_2}\Delta\omega\right)^2}\right)\left(\frac{Kv}{2\Delta\omega}\right)^2\right)\ldots\ldots\ldots(12)$$

where the output noise power Pn is normalized with respect to the carrier power Pc.

Equation (12) reveals two important aspects. First a low Kv is required for a low phase noise PLL. However, reducing Kv will make the loop dynamics slower and the PLL will take a long time to correct abrupt changes in frequency. The PLL will also require a large time to lock during start up. Usually Kv cannot be varied, because once the VCO is designed Kv becomes fixed.

The second aspect of equation (12) is the effect of the thermal noise of the resistor. Reducing R_1 is always desirable but this would require an increase in C_1 to maintain stability of the loop. Since the stability factor (neglecting C_2) is defined as,

$$\zeta = 0.5R_1\sqrt{C_1KvK_{CP}}\ldots\ldots\ldots(13)$$

Hence a two fold reduction in R_1 would require C_1 to increase by four times to maintain the same amount of loop stability provided other parameters are constant. The required increase in C_1 leads to a severe area penalty. This problem can be somewhat alleviated by using MOS capacitors instead of poly capacitors. However, MOS caps are nonlinear and hence limit the control voltage range. To achieve the maximum tuning range,

the control voltage must approach the supply and ground rails, demanding a reasonable capacitor linearity across this range.

5.0 Design Procedure

Having discussed the different trade-off in reducing the output noise of PLLs, we know attempt to describe a step by step design procedure of PLLs that simultaneously promise good phase noise properties, low reference spurs and enhanced loop stability. The procedure is derived from [9] with some necessary modifications. The design procedure is described for a third order Type II PLL and can be easily extended to higher order PLLs. It is basically a trial and error procedure which terminates once low phase noise has been achieved:

1. Kv (i.e. VCO gain) is determined from simulation.

2. The maximum phase margin of the PLL is expressed as [9],

$$PMmax = arc\tan(\sqrt{b+1}) - arc\tan\left(\frac{\sqrt{b+1}}{b+1}\right) \ldots\ldots\ldots (14)$$

where $b=C_1/C_2$. A desired phase margin is chosen (typically>60^o) and b is determined from (14).

3. The loopbandwidth is given as [9],

$$\omega loop = \frac{\sqrt{b+1}}{\tau} \ldots\ldots\ldots\ldots (15)$$

where $\tau = R_1 C_1$. Typically the loop bandwidth is chosen to be one tenth the PLL output frequency [10]. Consequently $\tau = R_1 C_1$ can be determined using (15).

4. Assuming a sinusoidal ripple on the control voltage line due to charge pump mismatches, the reference spurs will be ΔP dB below the carrier where,

$$\Delta P = -20\log\frac{Kv\left(\frac{Ip}{C_1}\right)Tref}{2fref} \quad \ldots\ldots\ldots(16)$$

With reference spurs typically 50 dB below the carrier and all other parameters known (fref=reference frequency=1/Tref; N=divider ratio), Ip/C_1 can be determined (Ip=charge pump current). Ip and C_1 also satisfy [9]

$$\frac{KvIp}{2\pi N}\left(\frac{b}{b+1}\right) = \frac{C_1}{\tau^2}\sqrt{b+1} \quad \ldots\ldots\ldots(17)$$

Thus (16) and (17) can be used to determine Ip and C_1. Since b is known from step (2), C2 can also be determined. Similarly R1 can be determined since $\tau = R_1 C_1$ is known from step (3).

5. Finally the noise contribution of R1 is determined using (12). If the calculated noise is negligible (i.e. typically -138 dBc/Hz@10MHz offset [8]) the design is complete otherwise C_1 must be increased from step 4 and step 5 must be repeated.

6.0 Conclusion

Designing low noise PLLs is very challenging since a number of performance metrics have to be taken into account simultaneously such as stability and reference spurs. The design is complicated because these metrics are not independent of each other; an improvement in one effect results in degradation in the other. The charge pump gain and

the loop filter resistance are the two basic parameters that can be utilized to improve the noise at low frequency offsets and large frequency offsets respectively. Increasing the charge pump gain promises low phase noise at low offset frequencies but has a detrimental effect on the reference spurs in the frequency spectrum. Reducing the resistance in the loop filter reduces the phase noise at high frequency offsets but effects the stability of the PLL. A step by step design procedure is described that takes into account all these effects.

7.0 References

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