TRANSIMPEDANCE AMPLIFIER WITH DIFFERENTIAL PHOTODIODE CURRENT SENSING

Bahram Zand, Khoman Phang, and David A. Johns

Dept. of Electrical and Computer Engineering
University of Toronto
Toronto, Ontario, M5S 3G4, CANADA

ABSTRACT

This paper presents a balanced receiver structure suitable for wireless infrared data communications. The receiver provides a fixed photodiode bias voltage with the use of a regulated cascode input stage. Together with an active feedback loop used to eliminate dc photocurrents, the receiver implements ac coupling without the need for matching capacitors. Differential sensing of the photodiode current improves sensitivity. Designed for a 0.35μm digital CMOS process, simulation results show that the circuit consumes 12mW at 3V, provides 40kΩ transimpedance gain over a bandwidth of 200 MHz, and has a minimum power supply rejection ratio of 40 dB over the entire operating bandwidth.

I. INTRODUCTION

Practically every new laptop computer, PDA (personal digital assistant), and digital camera comes equipped with an infrared (IR) wireless port. Over short distances, IR free-space links offer an industry-standard wireless solution unmatched in low cost and high speed. Digital CMOS is the preferred technology because of its low cost and high potential for system integration. However, building single-chip optical receivers in CMOS technology is challenging because low supply voltages, small transconductances, and substrate noise make it difficult to achieve high bandwidth and good sensitivity. IR wireless receivers must also be able to reject dc photocurrents generated by ambient light. Sometimes these photocurrents are much larger than the signal current, resulting in reduced swing or even saturation at the optical receiver.

Previously reported implementations [1] [2] sensed the photocurrent single-endedly. In addition, in order to reject noise from the photodiode bias source, an additional dummy capacitor was used [1] to match the photodiode capacitance. In this paper, we present an improved receiver structure that realizes differential sensing of the photodiode and eliminates the need for a matching capacitor. It uses a truly differential feedback structure for improved power supply rejection. The photodiode bias circuit has also been incorporated into the receiver. The resulting circuit is an IR wireless receiver front-end with improved gain, bandwidth, and power supply rejection.

II. PREAMPLIFIER ARCHITECTURE

Fig. 1 shows the simplified schematic of the proposed preamplifier structure. The circuit is comprised of three sections: the photodiode bias input stage, the transimpedance amplifier, and the dc photocurrent rejection feedback loop. Transistors M_{f3} and M_{f6} regulate the reverse bias voltage across the photodiode. Regulated cascode circuit (RGC) [3] is employed to reduce the input impedance seen at the sources of M_{f5} and M_{f6}. These transistors provide a common-gate input buffer stage to the transimpedance amplifier. Transistor M_{f4} is added to improve the symmetry of the signal path. M_{f3} and M_{f4} are just for level shifting and as shown in Fig.3 they will be bypassed by C_1 and C_2 at our frequencies of interest.

Although, the proposed receiver structure does not impose any constraints on the design of the transimpedance amplifier, we present here a differential transimpedance amplifier that uses local shunt feedback in the second stage. The amplifier is similar to the two-stage design presented in [1], but uses a n-channel input differential pair similar to the design in [4] to achieve higher bandwidth and reduced thermal noise.

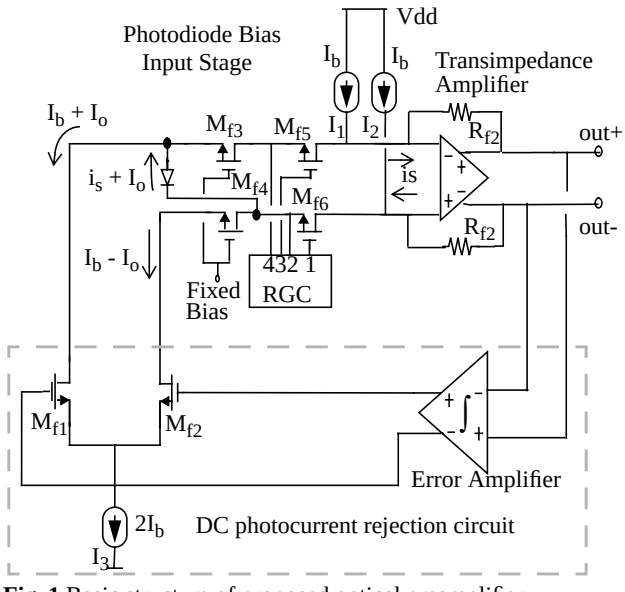

Fig. 1 Basic structure of proposed optical preamplifier.

The dc rejection feedback loop consists of an error amplifier and a differential pair made up of transistors

0-7803-5474-5/99/$10.00(C)1999 IEEE

M_{f1} and M_{f2}. The error amplifier functions as an integrator and determines the average difference in the differential outputs. Current sources I_1 and I_2 bias the cascode transistors $M_{f3\text{-}6}$. In the absence of any dc photocurrent, all currents sourced by I_1 and I_2 will be drawn away from the transimpedance amplifier by the differential pair. The presence of a dc photocurrent, I_o, results in a negative differential offset voltage at the output of the transimpedance amplifier. This offset causes the error amplifier to change the differential voltage applied to the differential pair. In steady state, the bias current increases by I_o for M_{f1} and decreases by I_o for M_{f2} as illustrated in Fig. 1. In essence, the dc photocurrent has been steered into the differential pair, away from the transimpedance amplifier. In contrast, the differential pair appears as a high impedance path to the signal current, i_s. As a result, i_s passes through to the transimpedance amplifier where it is sensed differentially, resulting in a transimpedance gain of $2R_{f2}$.

The proposed structure offers several advantages over the original structure reported in [1] and shown in Fig.2. The most significant advantage is that the proposed structure is fully differential. In the original structure, only the transimpedance amplifier is differential. As well, the sensing of the photodiode current is single-ended, so that only photocurrent sourced from the anode of the photodiode is used. This has two disadvantages: first, the current being sunk by the cathode of the photodiode is not put to use, effectively halving the signal current. Secondly, driving a differential transimpedance amplifier single-endedly creates an asymmetry in the differential structure. As a result, an additional capacitor, C_d', is required at the other input terminal of the transimpedance amplifier in order to match the photodiode capacitance, effectively rebalancing the circuit. Perfect matching ensures that noise injected at the bias voltage, V_{ref}, appears only as a common-mode signal which is effectively rejected by the differential transimpedance amplifier. Unfortunately, achieving good matching is difficult since the photodiode is an external device, and its capacitance varies with the applied reverse bias voltage.

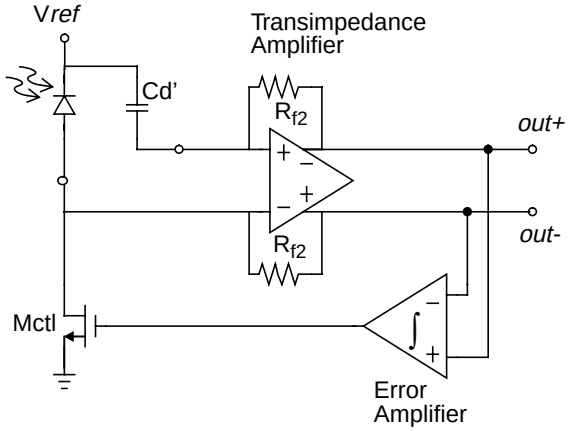

Fig. 2 Active dc photocurrent cancellation circuit presented in [1].

With the proposed differential structure, the photocurrent is sensed differentially. Since the photodiode is placed across the differential inputs of the transimpedance amplifier, the resulting circuit is inherently balanced, eliminating the need for a dummy matching capacitor.

Unlike the dc photocurrent rejection circuit in Fig.2, the bandwidth of the proposed receiver structure is independent of the dc photocurrent level. The lower cut-off frequency is not affected because the differential pair is already biased with a current of I_b which is designed to be much larger than the maximum dc photocurrent. The upper cut-off frequency is not affected because the bias currents of transistors M_{f3} and M_{f6} are regulated by the feedback loop to I_b regardless of the value of I_o.

III. PHOTODIODE BIAS INPUT STAGE

The photodiode biasing circuit including the common-gate and RGC transistors is shown in Fig. 3. The reverse bias voltage on the photodiode is determined by the voltage differences at the sources of M_{f3} and M_{f6}. For a 3V supply, the applied bias voltage ranges from a minimum of the threshold voltage of an NMOS device to a maximum of about 1V which is required to keep all MOSFETs in the active region. To explain the operation of the RGC blocks, we refer to the equivalent half-circuit schematic shown in Fig.4.

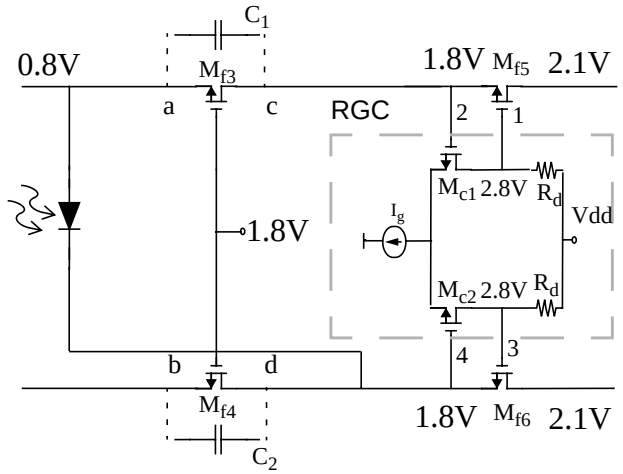

Fig. 3 Regulated cascode (RGC) circuits.

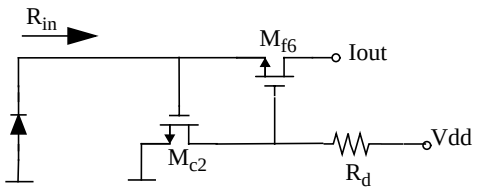

Fig. 4 Equivalent half-circuit of RGC block.

The input impedance of this circuit is

0-7803-5474-5/99/$10.00(C)1999 IEEE

$$R_{in} \approx \frac{1}{g_{m_{M_{f6}}}\left(1 + g_{m_{M_{c2}}} R_d\right)} \qquad (1)$$

Basically, it is the input impedance of a simple common-gate stage reduced by the factor $(1 + g_{m_{Mc2}} R_d)$ which is one plus the loop gain of feedback circuit made up of M_{c2} and R_d. Some design considerations which limit the minimum achievable input impedance include the allowable voltage drop across R_d, power consumption, and frequency response of the feedback circuit. For the differential configuration, the impedance looking into the bias circuit will be twice that given in equation (1). The frequency pole resulting from the depletion capacitance of the photodiode, C_{PD}, and the differential input impedance $2R_{in}$ is

$$P_1 = \frac{1}{2R_{in}C_{PD}} \qquad (2)$$

To illustrate the design process, if we assume a photodiode capacitance of 5 pF and wish to have a pole at 250 MHz, the differential impedance of the input stage must be kept about 125Ω. This means that, for a transconductance of 4.5 mA/V at the cascode device, Mf_5, we need a minimum RGC loop gain of 2.55. This can be achieved by choosing R_d = 600Ω and g_{mMc1} = $4.25mA/V$. Other poles such as the pole created by the feedback network, R_{f2} and C_{f2}, as well as complex poles introduced by the second stage of differential transimpedance amplifier (Fig.7) will limit the total bandwidth to about 200 MHz. The simulated differential input impedance of the input bias stage is shown in Fig.5. Note how the impedance is maintained at around 125Ω only up to the required bandwidth. While the photodiode capacitance as well as pad and packaging parasitic effects at nodes a and d of Fig.3 create an asymmetry in the circuit, capacitors C_1 and C_2 will alleviate this problem by bypassing transistors M_{f3} and M_{f4} at high frequencies. These capacitors are off-chip capacitors in the range of a few nF.

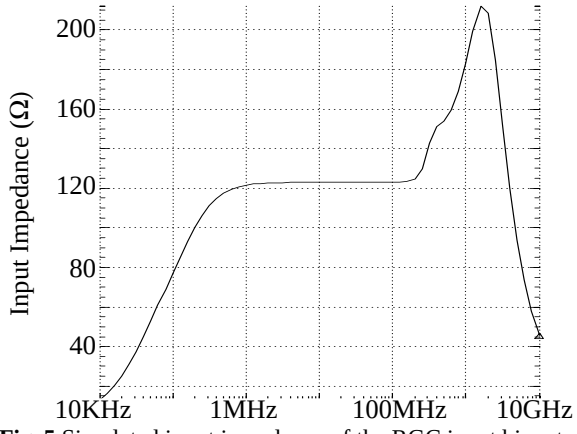

Fig. 5 Simulated input impedance of the RGC input bias stage.

IV. DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER

Fig. 6 shows the schematic diagram of the transimpedance amplifier. Diode-connected transistor M_{13} is used to level-shift the output common-mode voltage to about 2.1V. The transimpedance gain of the circuit is given by

$$\frac{2A_{vd}}{1 + A_{vd}} R_{f2} = 2R_{f2} \qquad for A_{vd} \gg 1 \qquad (3)$$

where $A_{vd} = g_{mi}R_{f1}$ is the open-loop voltage gain of differential amplifier and g_{mi} is the transconductance of the input differential pair[1].

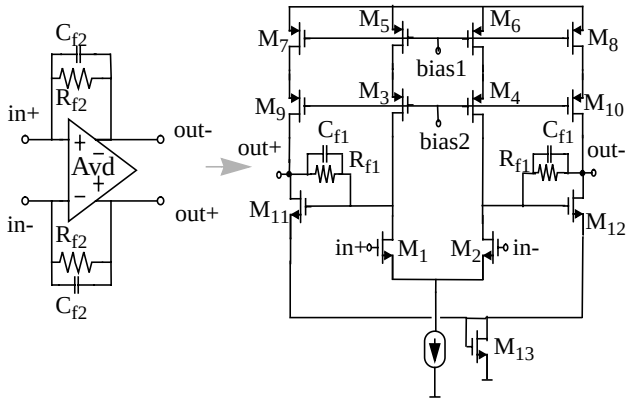

Fig. 6 Differential transimpedance amplifier circuit.

The bandwidth of this transimpedance amplifier is dependent on the capacitance seen at the input terminals as well as the frequency response of second stage. Because the photodiode bias input stage has isolated the transimpedance amplifier from the large photodiode capacitance, non-dominant poles of the total circuit are determined by the second stage of the above circuit. A small-signal model for the second stage of transimpedance amplifier is shown in Fig. 7 where C_{f1} is the total shunt feedback capacitance bridging the drain and gate of M_{11} or M_{12} and C_i and C_o are the input and output capacitance respectively.

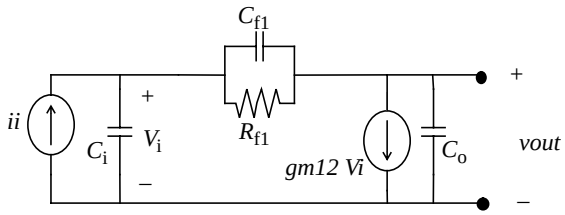

Fig. 7 Simplified model for second stage.

Because of the presence of two capacitors, C_i and C_o, the second stage exhibits a second-order response. Shunt feedback capacitor, C_{f1}, can be used to tune the pole locations and to maximize the bandwidth [1].

0-7803-5474-5/99/$10.00(C)1999 IEEE

V. SIMULATION RESULTS

The simulated frequency response of the complete receiver circuit is shown in Fig. 8. The preamplifier has a bandwidth from 180 KHz up to 200 MHz with gain of 40kΩ (92dBΩ), and a minimum input noise current density of $5pA/\sqrt{Hz}$. It consumes 12mW using a single 3V supply. In comparison with [1], the proposed circuit exhibits four-fold improvement in the gain-bandwidth product with the same technology and power dissipation.

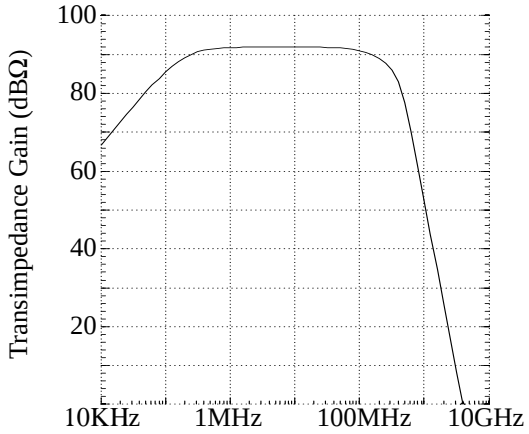

Fig. 8 Frequency response of entire receiver circuit.

Fig.9 shows the differential output steady state transient response to a 10μA input pulse stream after the cancellation of dc components.

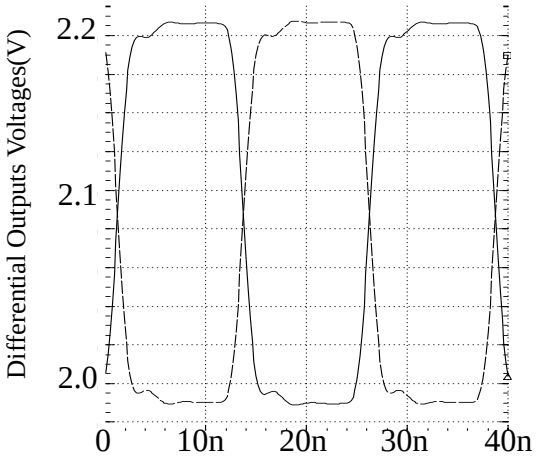

Fig. 9 Pulse response of optical receiver.

Because of the symmetric configuration, this circuit is highly immune to substrate noise and power supply modulation. Fig. 10 shows the Power Supply Rejection Ratio (PSRR) of the receiver. The PSRR is at least 40 dB over the entire bandwidth of the receiver for C_1=C_2=10nF.

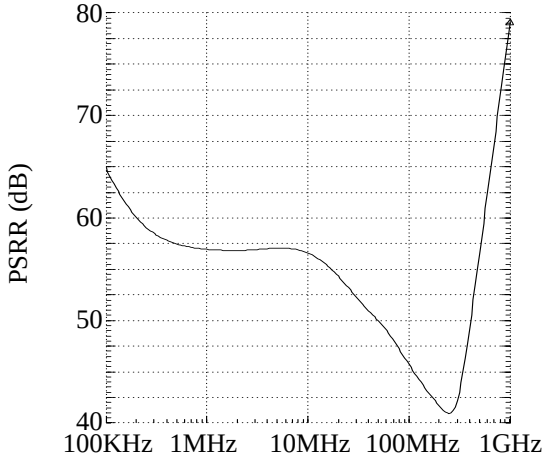

Fig. 10 Power supply rejection vs. frequency.

VI. SUMMARY

This paper proposes a balanced fully differential receiver structure for use in infrared wireless data communications. The structure rejects dc photocurrents using negative feedback around the transimpedance amplifier. Input common-gate transistors operating as regulated cascodes reduce the input impedance of the receiver, moving the dominant pole away from the transimpedance stage. Differential sensing of the signal current doubles the overall transimpedance gain and the bandwidth has also been improved. The proposed symmetric configuration is robust to common-mode interference. This circuit is designed for a 3V, 0.35 μm CMOS process. Simulation results show the preamplifier provides a gain of 40 kΩ over a bandwidth of 180 kHz to 200 MHz with a minimum PSSR of 40dB.

VII. REFERENCES

[1] K. Phang and D.A. Johns, "A 3-V CMOS Optical Preamplifier with dc Photocurrent Rejection," *IEEE Proc. ISCAS*, TAA8-8, June 1998.

[2] R.G.Swartz, Y.Ota, M.J.Tarsia, and V.D.Archer, "A Burst Mode, Packet Receiver with Precision Reset and Automatic Dark Level Compensation for Optical Bus Communications, "*Symp. on VLSI technology*, Kyoto, Japan, pp.67-68, May 1993.

[3] S.M. Park and C. Toumazou, "Low Noise Current-Mode CMOS Transimpedance Amplifier for Giga-bit Optical Communication, " *IEEE Proc. ISCAS*, TAA8-4, June 1998.

[4] R. Coppoolse, J. Verbeke, P. Lambrecht, J. Codenie, and J. Vandewege, "Comparison of a Bipolar and a CMOS Front End in Broadband Optical Transimpedance Amplifiers," *Proc. 38th Midwest Symp. on Cir. and Sys.*, Brazil, pp. 1026-1029, Aug. 1996.

0-7803-5474-5/99/$10.00(C)1999 IEEE