

Analysis of Timing Jitter in Ring Oscillators Due to Power Supply Noise

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ABSTRACT

This paper presents a time-domain method for estimating the jitter in ring oscillators that is due to power supply noise. The method is used to analyze and compare the RMS cycle-to-cycle jitter of ring oscillators constructed from three possible delay elements: a CMOS digital inverter, a differential pair, and a current steering logic (CSL) inverter. Spice simulations verify the analysis method, and the results indicate that both the differential pair and CSL inverter provide superior supply noise immunity to the CMOS digital inverter.

1. INTRODUCTION

Ring-based voltage-controlled oscillators (VCO) are well-suited for integration since they require no external components. While their intrinsic phase noise is relatively high compared to that of harmonic or LC oscillators, the dominant noise source is often actually due to the power supply. Such noise typically appears as steps or impulses on the power supply of the oscillator, and it affects both the frequency and phase of the VCO, causing cycle-to-cycle jitter.

Since jitter is a time-domain characteristic, we will use the linear, time-invariant, time-domain oscillator model [1], shown in Figure 1 for a 3-stage ring oscillator, in our analysis of jitter due to supply noise.

In Figure 1, each element in the ring oscillator is modeled as a cascade of an integrator and a Schmitt trigger block. The output waveforms of the proposed, three-stage ring oscillator are shown in Figure 2. Each inverting stage in the ring contributes a time delay to the total period of oscillation. The delays contributed by the i -th stage, τ_{ri} and τ_{fi} are measured from the time the output begins switching to the time, t_{sp} , when it reaches the switching threshold voltage (V_{sp}) of the input to the next stage, respectively.

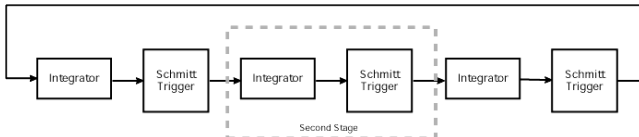


Figure 1: Time Domain Model for a 3-Stage Ring Oscillator

Hence the period of oscillation, T_0 , for an N -stage ring oscillator is given as:

$$T_0 = \sum_{i=1}^N (\tau_{ri} + \tau_{fi}) \quad (1)$$

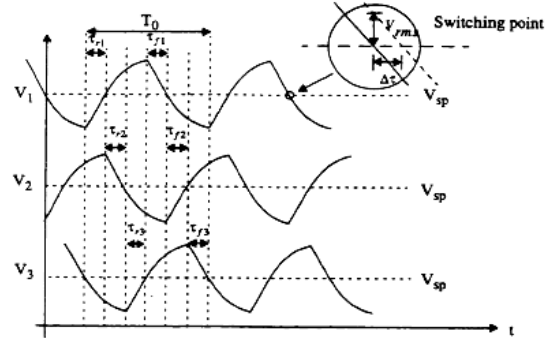


Figure 2: Output Waveforms for the 3-Stage Ring Oscillator

As can be seen in Figure 2, any perturbation voltage on the output of the integrator waveforms alters the time taken to reach the switching threshold. This timing error passes to the other stages in the oscillator ring and contributes to the total output jitter. As shown in [2], an RMS noise voltage $v_{RMS}(t_s)$, at the time of the threshold crossing, causes timing jitter which is proportional to the voltage error divided by the rising slope (S_{ri}) or falling slope (S_{fi}) of the output waveform. Thus the RMS cycle-to-cycle jitter for an N -stage ring oscillator can be expressed as [1]:

$$\sigma = \sqrt{\sum_{i=1}^N \left[\left(\frac{\Delta V_O(t_{sp-R})}{S_{ri}} \right)^2 + \left(\frac{\Delta V_O(t_{sp-F})}{S_{fi}} \right)^2 \right]} \quad (2)$$

To determine the effect of supply noise on the oscillator, the following relation can be used to estimate the change of period due to a small variation in the supply voltage:

$$\frac{\Delta T_{OSC}}{\Delta V_{DD}} = 2N \cdot \frac{\frac{\Delta V_O}{\Delta V_{DD}} \Big|_{V_O=V_{SP}}}{\frac{\Delta V_O}{\Delta t} \Big|_{V_O=V_{SP}}} \quad (3)$$

From Equation 3, we see that jitter is essentially dictated by two characteristics of the delay element: the power supply rejection ratio (PSRR), represented by the numerator, and the maximum slope at the switching-point of each delay element, represented by the denominator. In the next two sections, we will derive

analytic expressions for these two characteristics for the three delay element types shown in Figure 3: a standard CMOS digital inverter, the differential-pair, and the current steering logic (CSL) inverter [3]. M for the CSL inverter refers to the relative aspect ratio between the input common-source stage device and the diode-connected load device.

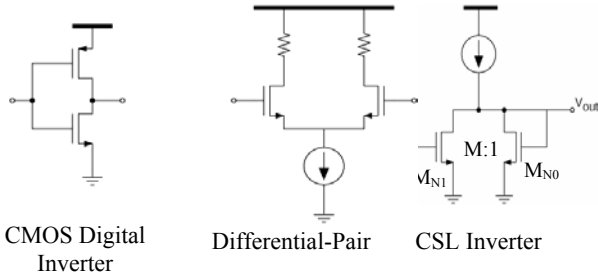


Figure 3: Three types of VCO Delay Elements

2. Mathematical Jitter Analysis

2.1 Power Supply Rejection Ratio (PSRR)

Figures 4(a-c) show the small-signal models for the three delay element types. These models are extracted at the switching point of the circuits, the point at which oscillators are most sensitive to power supply-induced timing jitter [4]. For the small-signal models, R_{CS} represents the equivalent output impedance of the cascode current source, and C_p represents the parasitic capacitance, referenced to V_{DD} , at the output node. This capacitance is the sum of stray drain-bulk and drain-gate capacitances from the cascode transistor of the PMOS current source.

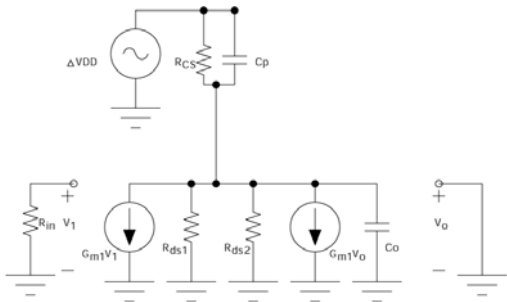


Figure 4a): Equivalent Small-Signal Circuit for the CSL Inverter

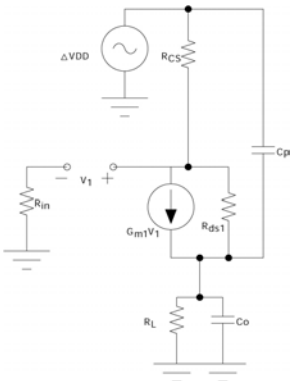


Figure 4b): Equivalent Small-Signal Circuit for the Diff. Pair

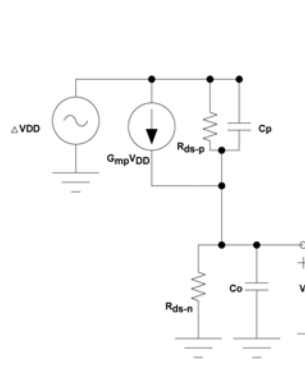


Figure 4c): Equivalent Small-Signal Circuit for the CMOS Digital Inverter

Table 1 summarizes the transfer functions derived from Figures 4(a-c). These equations were compared with the Spice simulation results obtained using a 0.18μ digital CMOS technology and which are shown in Figure 5.

Element Type	PSRR ($\Delta V_o/\Delta V_{DD}$) (V/V)
Digital Inverter	$\frac{\Delta V_{O-INV}(s)}{\Delta V_{DD}(s)} \approx \frac{g_m + C_p \cdot s}{2g_{ds} + s \cdot (C_p + C_o)} \quad (4)$
Differential Pair	$\frac{\Delta V_{O-DIFF}(s)}{\Delta V_{DD}(s)} \approx \frac{1 + g_m r_{ds}^2 C_p \cdot s}{g_{m2}^2 r_{ds}^2 + s \cdot g_m r_{ds}^2 (C_p + C_o)} \quad (5)$
CSL Inverter	$\frac{\Delta V_{O-CSL}(s)}{\Delta V_{DD}(s)} \approx \frac{1 + g_m r_{ds}^2 C_p \cdot s}{g_{m2}^2 r_{ds}^2 + s \cdot g_m r_{ds}^2 (C_p + C_o)} \quad (6)$

Table 1: Analytic Expressions for the PSRR of Three Delay Element Types

We draw the following observations:

- 1) The PSRR for the CMOS digital inverter is low-pass in nature, flattening out at high-frequencies. The digital inverter exhibits extremely poor low-frequency PSRR compared to either of the other two delay elements since any power-supply noise is amplified by the small-signal gain of the inverter. This is one of the reasons why digital inverters are not used in VCOs that are intended for jitter-sensitive applications.
- 2) The PSRR of both the differential-pair and CSL inverter are nearly identical over all frequency bands. The PSRR is approximately $1/(g_m r_{ds})^2$ at low frequencies, gradually degrading at higher frequencies until it reaches $C_p/(C_p + C_o)$, at which point the circuit operates as a capacitive voltage divider between the stray capacitances to V_{DD} , C_p , and the dominant load capacitance to V_{SS} , C_o .

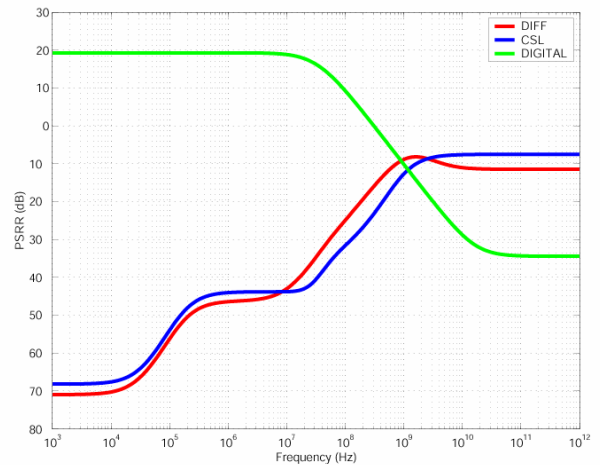


Figure 5: Spice Simulation Results Showing the PSRR for all 3 Types of Delay Cells

2.2 Rising and Falling Slopes

Expressions for the rising and falling slopes for both the CMOS digital inverter and the differential-pair can be found in references [1] and [5] respectively, while the derivation for the CSL inverter can be found in the Appendix. Table 2 summarizes the results for the three delay elements for an N-stage oscillator.

Element		
Digital Inverter [1]	$\frac{\beta_p \cdot V_{DD}^2}{2C_L} \cdot \left(\frac{\pi}{2} - 0.35\right)$	$-\frac{\beta_n \cdot V_{DD}^2}{2C_L} \cdot \left(\frac{\pi}{2} - 0.35\right)$
Differential Pair [5]	$\frac{\beta_0 \cdot V_{EFF-0}^2}{2C_L}$	$-\frac{\beta_0 \cdot V_{EFF-0}^2}{2C_L}$
CSL Inverter (Appendix)	$\frac{\beta_0 \cdot V_{EFF-0}^2}{2C_L} \cdot \frac{M}{(M+1)}$	$-\frac{\beta_0 \cdot V_{EFF-0}^2}{2C_L} \cdot \frac{M^2}{(M+1)}$

Table 2: Rise and Fall Slopes

Here, V_{eff-0} is the gate overdrive voltage present when the delay elements are at their switching threshold, C_L represents the total lumped output load capacitance of each delay stage, and β_0 , β_p and β_n represent the $\mu \cdot C_{ox} \cdot W/L$ of the analog NMOS input transistors along with the digital inverter p- and n-channel devices, respectively.

3. Analytical and Simulation Results

Having derived analytic expressions for both the PSRR and the rising and falling slopes for each delay element type, we can now estimate the frequency sensitivity to power supply noise using Equation 3. Assuming the supply voltage is modulated by a sinusoid, $\Delta V_{DD} = V_m \cdot \cos(\omega_m t)$, the oscillator period deviations, ΔT , can be derived for all three delay elements. Subsequently, the autocorrelation functions for the oscillator period deviations, ΔT , with respect to t can be obtained using the following relation:

$$C_{TT}(\tau) = E[\Delta T(t + \tau) \cdot \Delta T(t)] \quad (7)$$

Subsequently, it has been proven in [6] that the mean square cycle-to-cycle jitter σ^2 is equal to:

$$\sigma^2 = 2C_{TT}(\tau) \Big|_{\tau=0} - 2C_{TT}(\tau) \Big|_{\tau=1/f_0} \quad (8)$$

Thus, from Equations 7 and 8, the RMS cycle-to-cycle jitter due to power supply noise can be estimated for all three types of oscillator rings. Table 3 lists the final results:

Element	Estimated, RMS Cycle-to-Cycle Jitter: ΔT_{CC}
Digital Inverter	$\frac{2NC_L}{\beta_0 \cdot V_{DD}^2 \cdot k_{INV-2}} \cdot \sqrt{\frac{g_m^2 + (C_p \omega_m)^2}{4g_{ds}^2 + (C_p + C_O)^2 \omega_m^2}} \cdot V_m \cdot \sqrt{1 - \cos(2\pi \frac{f_m}{f_0})}$ (9)
Differential Pair	$\frac{2NC_L}{\beta_0 \cdot V_{eff0}^2} \cdot \sqrt{\frac{1 + [g_m r_{ds}^2 C_p \omega_m]^2}{[g_m^2 r_{ds}^2]^2 + [g_m r_{ds}^2 (C_p + C_O) \omega_m]^2}} \cdot V_m \cdot \sqrt{1 - \cos(2\pi \frac{f_m}{f_0})}$ (10)
CSL Inverter	$\frac{2NC_L}{M \beta_0 \cdot V_{eff0}^2} \cdot \sqrt{\frac{1 + [g_m r_{ds}^2 C_p \omega_m]^2}{[g_m^2 r_{ds}^2]^2 + [g_m r_{ds}^2 (C_p + C_O) \omega_m]^2}} \cdot V_m \cdot \sqrt{1 - \cos(2\pi \frac{f_m}{f_0})}$ (11)

Table 3: Table of σ_{RMS} , Estimated RMS Cycle-to-Cycle Jitter Due to Supply Noise

Spice simulations were performed to verify the RMS cycle-to-cycle jitter values estimated by Equations 9 to 11. Figure 6 shows the output spectrum and measured RMS cycle-to-cycle jitter for a 5-stage ring oscillator implemented utilizing each of the three delay element types. All of the oscillator rings were tuned to have a center frequency of 129MHz. The 1.8V supply was modulated with a 10% sinusoid at frequencies of 10MHz, 88MHz, 129MHz and 188MHz. Figure 6 shows the output spectrum for the 10MHz case, in which the tone introduced by the power supply noise is modulated by the spectrum of the oscillator ring itself, introducing distortion and timing jitter in the output spectrum.

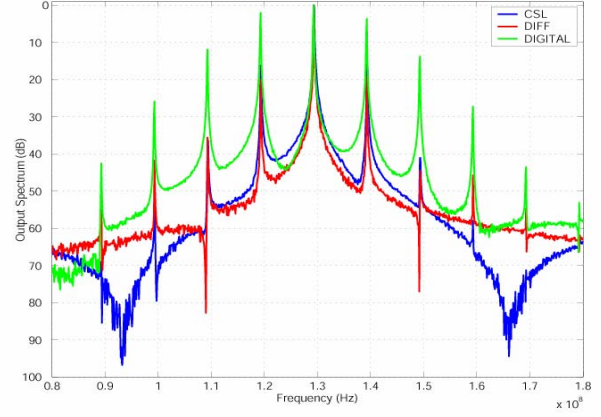


Figure 6: Output Spectrums, $F_M=10\text{MHz}$

Table 4 places the simulated results alongside the estimated values from our analysis. Table 4 compares estimated and simulated data for both the CSL and differential-pair delay elements. Both the differential pair and the CSL inverter analysis and simulations exhibited the best matching since the linear, time-invariant model of an oscillator ring used in this analysis is most accurate for oscillators with small-signal voltage swings [7]. In addition, simulation results also verified the relation between timing jitter and the spectral makeup of injected supply and substrate noise relative to the oscillator frequency, as predicted by Equations 9-11.

RMS Jitter	Result	Digital Inverter	Diff. Pair	CSL Inverter
σ_{RMS} : $F_M=10\text{MHz}$	Calculated	873ps	42ps	24ps
	Simulated	373ps	94ps	84ps
σ_{RMS} : $F_M=88\text{MHz}$	Calculated	1.59ns	153ps	36ps
	Simulated	517ps	157ps	92ps
σ_{RMS} : $F_M=129\text{MHz}$	Calculated	0 ps	0 ps	0 ps
	Simulated	2.4ps	2.8ps	2.1ps
σ_{RMS} : $F_M=188\text{MHz}$	Calculated	391ps	141ps	30ps
	Simulated	105ps	135ps	49ps

Table 4: Table of σ_{RMS} , Estimated and Simulated RMS Cycle-to-Cycle Jitter for Various Power-Supply Modulation Frequencies, $F_M=10\text{MHz}$, 88MHz, 129MHz and 188MHz

Figure 7 illustrates how the final analytic expressions in Table 3 can be used to predict the sensitivity of the ring oscillator to the frequency spectrum of the supply noise. This is critical in understanding what bands of power-supply and substrate noise should be isolated from oscillator rings to achieve low jitter performance. Figure 7 predicts that both the CSL inverter and differential-pair based ring oscillators exhibit excellent low-frequency power rejection far superior to the digital inverter based oscillator due to the high PSRR of both cascaded delay elements at low-frequencies. However, at higher frequencies, the reduced PSRR of both the differential and the CSL oscillator rings cause both of their predicted RMS, cycle-cycle jitter transfer-functions to increase significantly. Furthermore, Equations 9 to 11 predict that all three oscillator rings should exhibit nulls in their jitter transfer-functions at the harmonics of the oscillator ring center-frequency, (i.e., for $f_m = f_O, 2 \cdot f_O, 3 \cdot f_O$, etc.); indeed, the simulation results in Table 4 for $f_m = f_O$ validate this prediction.

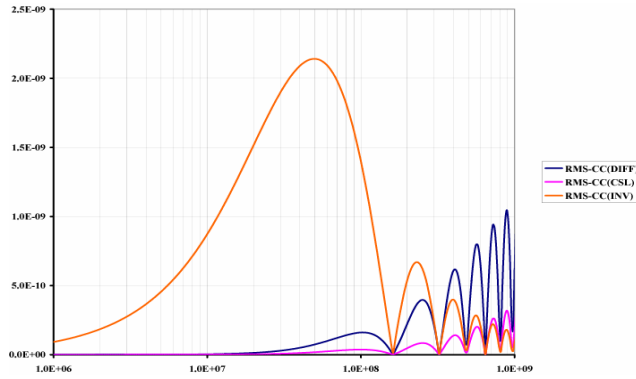


Figure 7: Plot of Calculated σ_{RMS} Versus Supply Noise Frequency, F_M .

4. Conclusions

The equations developed in this work can significantly aid in the design of ring oscillators. Complex relationships such as timing jitter are very difficult and time-consuming to simulate and model, so these expressions provide an apriori means of estimating the RMS cycle-to-cycle jitter due to power supply noise. The proposed analysis method allows critical design parameters to be estimated early in the design stage, allowing approximate sizings of transistors and phase-locked loop parameters to be optimized, thereby reducing the time required to iterate and optimize both the design of the oscillator and of the complete phase-locked loop.

5. REFERENCES

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Appendix: Rising and Falling Slopes of a CSL Inverter

Referring to Figure 3, when a positive input step voltage is applied to the CSL inverter, at the switching threshold, both M_{N0} and M_{N1} operate in the active region. As a result, performing KCL at the output node results in:

$$I_{CS} = \frac{\beta_0}{2} \cdot (V_O - V_{TN})^2 + M \cdot I_{CS} + C_L \frac{dV_O}{dt} \quad (A-1)$$

It can also be shown that the switching point (V_{SP}) for a CSL inverter biased with a tail current of I_{CS} is:

$$V_{sp} = V_{TN} + \sqrt{\frac{2I_{CS}}{(M+1)\beta_0}} \quad (A-2)$$

As a result, the falling slope of a CSL inverter at the switching point can be found by substituting Equation A-2 into Equation A-1, yielding:

$$\frac{dV_O}{dt}_{-fall} = -\frac{\beta_0 \cdot V_{EFF-0}^2}{C_L} \cdot \frac{M^2}{2(M+1)} \quad (A-3)$$

Similarly, to calculate the rising slope of the CSL inverter, it is now assumed a negative input step voltage is applied to the CSL inverter. At the switching threshold, $V_O = V_{SP}$ and only M_{N0} is on and operating in the active region. As a result, this time performing KCL at the output node results in:

$$I_{CS} = \frac{\beta_0}{2} \cdot (V_O - V_{TN})^2 + C_L \frac{dV_O}{dt} \quad (A-4)$$

Once again, Equation A-2 is substituted, yielding a rising slope of:

$$\frac{dV_O}{dt}_{-rise} = \frac{\beta_0 \cdot V_{EFF-0}^2}{C_L} \cdot \frac{M}{2(M+1)} \quad (A-5)$$

As can be seen in Equations A-3 and A-5, the slope during a falling transition is typically M time larger than for a rising transition because of the large, transient, charging current provided by the switching transistor M_{N1} , which is on for falling transitions only.