ANALYSIS OF OUTPUT RIPPLE IN MULTI-PHASE CLOCKED CHARGE PUMPS

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ABSTRACT

This paper presents a mathematical analysis of the ripple voltage caused by a mismatch in parasitic capacitances in multi-phase, clocked charge pumps. Through detailed circuit modeling, we show that a relatively *large* pedestal ripple is caused by a *small* mismatch in parasitic capacitance. We present a simple circuit solution and verify its performance with simulation and experimental results.

I. INTRODUCTION

In the context of deep sub-micron CMOS technologies and reduced supply voltages approaching 1V, the charge pump or voltage multiplier emerges as an important building block. On-chip charge pumps can not only provide higher internal supply voltages, they can generate higher *bias* voltages that can be used to extend the performance of certain low-voltage circuits[1-4]. In crucial biasing applications, circuit performance may suffer if a multi-phase, clocked charge pump is used; such charge pumps display a characteristic we will refer to as 'pedestal feedthrough' resulting in a significant output ripple voltage. In this paper, we discuss the origins of pedestal feedthrough and present a detailed analysis that accurately quantifies the resulting ripple.

II. CHARGE PUMP

The charge pump in Fig. 1 is based on a simple cross-connected NMOS transistor cell [5] and the utilization of two serial switches at the output alternately driven by a two-phase clock. The circuit consists of three closely coupled charge pump cells [4]. The middle cell uses devices Q_1 and Q_2 to generate level-shifted clock signals with the full supply swing. Clock signals Φ_1 and Φ_2 have a signal swing of V_{DD}. These level-shifted clock signals are used to turn on the outermost charge pump consisting of devices Q_3 and Q_4, and to pass the input voltage, V_{in}, to the top plates of capacitors C_3 and C_4. The clock signals Φ_{1Vin} and Φ_{2Vin} that drive capacitors C_3 and C_4 may have a reduced voltage swing that is equal to the input voltage, V_{in}, in order to realize a voltage doubler (i.e. $Vout = 2V_{in}$). In general, the charge pump acts as a voltage summer, adding the voltage swing of clock signals Φ_{1Vin} and Φ_{2Vin} to the input voltage. As such, if the voltage swing of the clocks is V_{DD}, then at steady state, the voltages at the top plates of C_3 and C_4 fluctuate between V_{in} and (V_{in} + V_{DD}). The third and final charge pump cell uses devices Q_5 and Q_6 to drive the dual phase PMOS output switches Q_7 and Q_8. Bias voltage V_{SWL} is adjustable and can be set to equal V_{in} or made slightly less in order to reduce the output resistance of the PMOS switches. The steady state output voltage of the charge pump is

$$V_{out} = V_{in} + V_{DD} . \quad (1)$$

Higher output voltages may be generated by adding more pumping stages. The clock signals are generated from an integrated, non-overlapping, two-phase clock generator. The technique of bulk-switching [5] can be applied to improve the overall power efficiency of the charge pump, but it has not been included in this design because the intended application only requires the charge pump to drive the gates of MOSFETs. Since no current is drawn, power efficiency is not crucial.

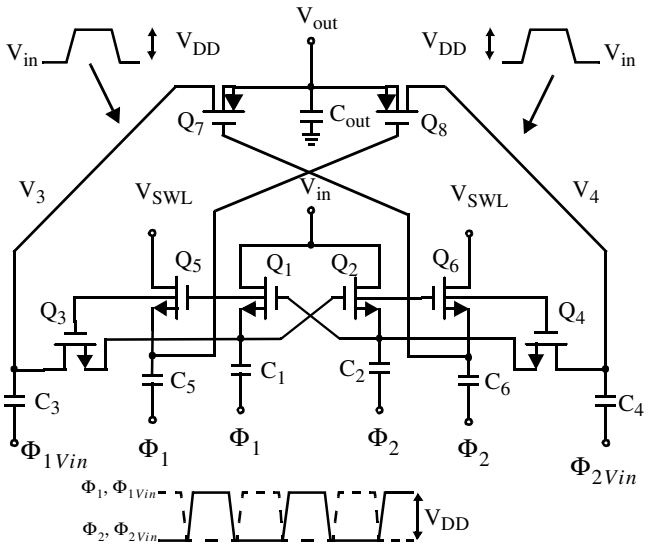

Fig. 1 Dual phase charge pump with associated steady-state waveforms.

The charge pump suffers from a ripple voltage at the output, even in the absence of a load resistance. The voltage ripple is generated through parasitic current leakage, charge injection, clock feedthrough, and pedestal feedthrough. An output ripple from 8 to 10 mV (peak-to-peak) was measured experimentally from an initial implementation of the charge pump[4]. This measured ripple was much larger than the predicted simulated ripple of about 0.5mV. Upon further analysis, we determined that our simulation results, while predicting the effects of charge injection and clock feedthrough, did not account for the effects of mismatch. And while we initially postulated that the increased ripple was the result of a mismatch between capacitors C_3 and C_4, further analysis revealed that, while this mismatch is a contributing factor, the dominant cause of ripple is actually the mismatch between the *parasitic* capacitances at nodes V_3 and V_4 in Fig. 1.

III. RIPPLE ANALYSIS

In this section, we analyze the effects of the various mismatches on pedestal feedthrough and develop a model for predicting the ripple voltage. Fig. 2 shows the output stage of the charge pump, including device overlap capacitances and parasitic node capacitances.

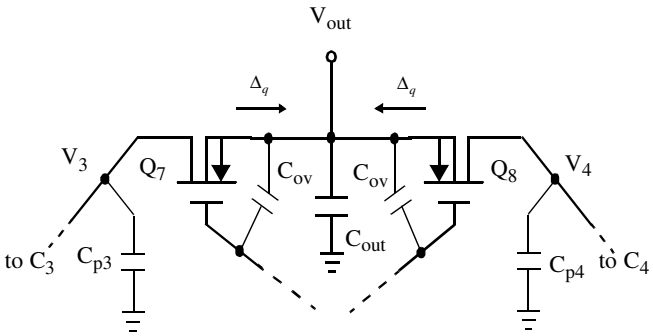

Fig. 2 Sources of charge injection, clock feedthrough and pedestal feedthrough.

Pedestal feedthrough can be understood by considering the symmetry of the charge pump. The final output voltage during one clock phase is determined by the voltage that exists on the top plate of capacitor C_3 through Q_7 in Fig. 1. During the next clock phase, the voltage on the top plate of C_4 is passed to the output through Q_8. Ideally, both of these voltages are identical and the output is a constant. However, if there is a mismatch between capacitors C_3 and C_4, or more importantly, between parasitic capacitances C_{p3} and C_{p4}, then the two voltages will not be the same and the output waveform will resemble a 'pedestal' or a periodic square wave whose amplitude will be the difference between the two voltages. Assuming the left side of the charge pump charges the output capacitor to V_{out3} through Q_7 and that the right side charges the output capacitor to V_{out4} through Q_8, the amplitude of the output pedestal would then be $|V_{out4} - V_{out3}|$. Expressions for V_{out3} and V_{out4} can be derived by referring to Fig. 3. Fig. 3a shows that when Φ_1 is high, C_{out} is charged to some steady-state voltage, V_{out3}, and the top plate of C_4 (and C_{p4}) is charged to the input voltage, V_{in}. During the next clock phase when Φ_2 goes high, C_{out} is connected in parallel to C_4 and C_{p4}, and the output assumes a steady-state voltage of V_{out4} as shown in Fig. 3b.

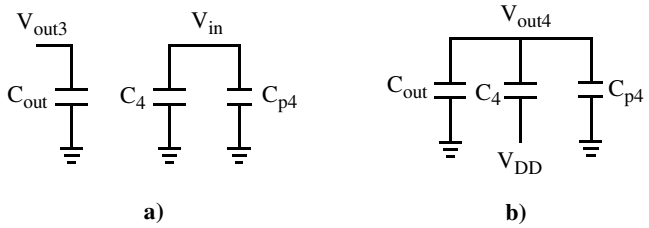

Fig. 3 Equivalent right half-circuit of the charge pump on clock phases a) Φ_1 and b) Φ_2.

In the absence of any output load, charge is conserved between these two clock phases so that

$$V_{out3} \cdot C_{out} + V_{in} \cdot (C_4 + C_{p4}) = V_{out4} \cdot (C_{out} + C_{p4}) + (V_{out4} - V_{DD}) \cdot C_4 . \quad (2)$$

Isolating V_{out4} we have

$$V_{out4} = \frac{V_{in} \cdot (C_4 + C_{p4}) + V_{DD} \cdot C_4 + V_{out3} \cdot C_{out}}{C_{out} + C_4 + C_{p4}} . \quad (3)$$

In a similar manner, it can be shown that due to the symmetry of the charge pump, V_{out3} is given by

$$V_{out3} = \frac{V_{in} \cdot (C_3 + C_{p3}) + V_{DD} \cdot C_3 + V_{out4} \cdot C_{out}}{C_{out} + C_3 + C_{p3}} . \quad (4)$$

By combining equations (4) and (5) and isolating the output voltages, we obtain the relations

$$V_{out3} = \frac{V_{in} \cdot \left\{ C_3 + C_{p3} + \frac{C_{out} \cdot (C_4 + C_{p4})}{C_{out} + C_4 + C_{p4}} \right\} + V_{DD} \cdot \left\{ C_3 + \frac{C_{out} \cdot C_4}{C_{out} + C_4 + C_{p4}} \right\}}{C_{out} + C_3 + C_{p3} - \frac{C_{out}^2}{C_{out} + C_4 + C_{p4}}} \quad (5)$$

and

$$V_{out4} = \frac{V_{in} \cdot \left\{ C_4 + C_{p4} + \frac{C_{out} \cdot (C_3 + C_{p3})}{C_{out} + C_3 + C_{p3}} \right\} + V_{DD} \cdot \left\{ C_4 + \frac{C_{out} \cdot C_3}{C_{out} + C_3 + C_{p3}} \right\}}{C_{out} + C_4 + C_{p4} - \frac{C_{out}^2}{C_{out} + C_3 + C_{p3}}} . \quad (6)$$

In the absence of any parasitic capacitances (i.e. $C_{p3} = C_{p4} = 0$), equations (5) and (6) reduce to

$$V_{out3} = V_{out4} = V_{in} + V_{DD} \tag{7}$$

as expected. Note that equation (7) holds even if $C_3 \neq C_4$, thereby proving that a mismatch between C_3 and C_4 alone, in the absence of any stray capacitance, will not contribute to the output ripple. In the presence of parasitic capacitances, $V_{out3} \neq V_{out4}$, and a pedestal voltage ripple will exist at the output and will have an amplitude of

$$\Delta V_{ped} = \frac{V_{DD} \cdot (C_3 \cdot C_{p4} - C_4 \cdot C_{p3})}{C_{out} \cdot (C_3 + C_4 + C_{p3} + C_{p4}) + C_3 \cdot C_4 + C_3 \cdot C_{p4} + C_4 \cdot C_{p3} + C_{p3} \cdot C_{p4}} \tag{8}$$

where $\Delta V_{ped} = V_{out3} - V_{out4}$. If we assume that $C_3 = C_4 = C$ and $C_{out} \gg C$ then the above equation may be simplified as follows:

$$\Delta V_{ped} \cong \frac{\Delta C_p}{2 \cdot C_{out}} \cdot V_{DD} \tag{9}$$

where $\Delta C_p = C_{p4} - C_{p3}$. This equation shows that for a relatively *small* parasitic capacitance mismatch, a sufficiently *large* output ripple will result. Physically, capacitances C_{p3} and C_{p4} represent the combined effects of the nonlinear capacitances associated with switches Q_3 and Q_4, Q_7 and Q_8, the top plate parasitic capacitances of C_3 and C_4, and the parasitic capacitances to the substrate from all interconnect lines. For a 0.35µm CMOS process and using a switch aspect ratio of 1µm/0.4µm, these parasitic capacitances were extracted to be about 0.1 to 0.2 pF. For example, if we assume C_{p3} = 0.12 pF and C_{p4} = 0.08 pF (i.e. a 50% mismatch) and for C_{out} = 7 pF and V_{DD} = 1.2 V, the output voltage pedestal ripple will be approximately 3.4 mV according to equation (9). For a mismatch of 0.08 pF, the voltage pedestal will also double to 6.8 mV. Fig. 4a) is a simulation of the output of the charge pump with a 0.04 pF mismatch in parasitic capacitances that confirms the validity of equation (8) and the approximation of equation (9).

As suggested by equation (8), with the presence of parasitic capacitances, a mismatch between capacitors C_3 and C_4 does contribute to pedestal feedthrough. And while our simulations have shown this mismatch to be less significant than the mismatch between the parasitic capacitances, these two sources of mismatch are not independent, and any mismatch in capacitors C_3 and C_4 will indirectly cause a mismatch in the top plate parasitic capacitances. However, if C_3 and C_4 are small capacitors, their contribution to the overall stray capacitance will be small in comparison to the junction parasitics of the active devices.

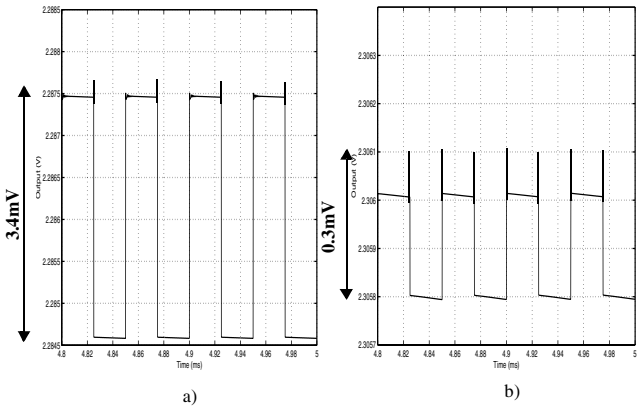

Fig. 4 Output showing pedestal clock feedthrough for a 0.04 pF mismatch in parasitics: a) original charge pump, b) modified half-phase charge pump.

IV. ELIMINATING PEDESTAL FEEDTHROUGH

From equation (9) it would appear that the only way to reduce the effect of pedestal feedthrough is to use small-area devices resulting in a smaller ΔC_p, or to increase the output capacitance, C_{out}. The first option is not practical since the technology limits the smallest devices possible. In the charge pump presented in [4], pedestal feedthrough was still significant in spite of the use of minimum sized switches. The second option can be used to some advantage but a larger output capacitance would result in longer charge-up times and occupy more integrated area, especially if multiple charge pumps are incorporated on chip.

One simple circuit solution would be to simply disconnect Q_7 and Q_8 at the output and to use only one output as shown in Fig. 5. The pedestal feedthrough due to mismatches between the two halves of the charge pump would then be eliminated and only the residual ripple due to parasitic current leakage, charge injection, and clock feedthrough would remain. It is worth noting that the balanced structure in Fig. 5 can be simplified by eliminating Q_3 and Q_7.

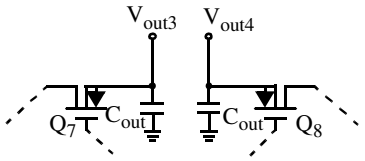

Fig. 5 Circuit modification to eliminate pedestal feedthrough.

Fig. 4b) is a simulation of the output of the modified charge pump with 0.04 pF mismatch in parasitics. The pedestal feedthrough is now eliminated, and only a residual

voltage ripple of 0.3mV — an order of magnitude lower than the ripple in Fig. 4a) — is present. Although this method succeeds in eliminating the ripple due to pedestal feedthrough, the resulting half-phase clocked charge pump is less efficient. For applications requiring the charge pump to deliver power to the output, alternative measures for reducing ΔC_p in equation (9) are needed in order to simultaneously achieve both high efficiency and low output ripple.

A simulation comparison of the step-up responses is shown for the original multi-phase clocked charge pump and the modified half-phase circuit for a 0.1 pF mismatch in parasitics in Fig. 6. A load capacitance of 7 pF and V_{in}=1.2V was used in both cases. As expected, the modified charge pump with its half-phase clocking scheme, takes about twice as long to charge up to steady state.

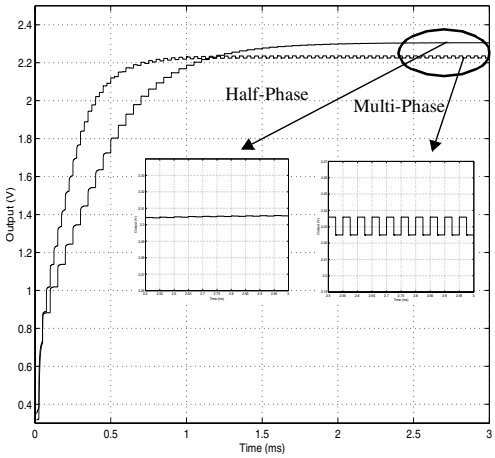

Fig. 6 Step-up responses of the original multi-phase charge pump and the modified half-phase version.

V. EXPERIMENTAL RESULTS

The half-phase clocked charge pump was fabricated in a double-poly, triple metal, 0.35µm CMOS process for use in a low-voltage, programmable hearing aid filter application [2]. A microphotograph of the charge pump is shown in Fig. 9. The measured amplitude of the output ripple was 0.8-1.0mV, or about ten times smaller than the ripple found on the initial charge pump design described in [4].

VI. CONCLUSIONS

The contributing factors to pedestal feedthrough in multi-phase clocked charge pumps were examined, and we have shown that the mismatch in parasitic capacitance of internal nodes in the charge pump proved to be the most significant. Analytic expressions of the output ripple were derived and showed that a relatively small parasitic capacitance mismatch will result in a sufficiently large output ripple. A simple circuit modification was proposed that significantly reduces pedestal feedthrough at the cost of power efficiency. However, such a solution can be readily applied with no apparent disadvantages in applications where the charge pump is only driving the gates of MOSFETs.

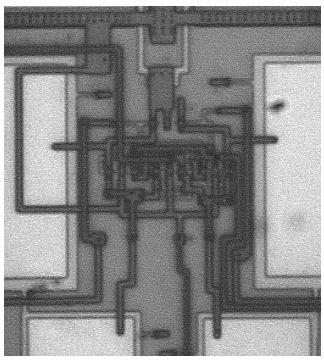

Fig. 9. Microphotograph of the modified charge pump.

VII. REFERENCES

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