14.4 A 1V 1mW CMOS Front-End with On-chip Dynamic Gate Biasing for a 75Mb/s Optical Receiver

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Optical communications is rapidly expanding beyond long-haul fiber-optic networks into shorter distance, lower-cost applications such as infrared wireless links and fiber-to-the-home (FTTH). CMOS implementations of optical receivers are attractive given their reduced cost and size, but the trend towards lower system voltages in CMOS challenges the long-term viability of integrated designs. Traditionally, low-voltage operation has not been a requirement, and few receiver designs have pushed below 2V where low voltage seriously impacts performance. To date, the lowest reported design uses low-threshold devices to achieve 1.2V operation [1]. In contrast, the optical front-end presented here achieves 1V operation without special devices.

The biggest design challenge lies at the preamplifier stage. Beside maximizing the gain and sensitivity for a given bandwidth, the preamplifier must also have a wide dynamic range and provide the photodiode with a sufficient reverse bias voltage. The bias voltage can be maximized using the wide-swing, low-voltage transimpedance amplifier shown in Figure 14.4.1. The design consists of a sub-1V current amplifier [2] in transimpedance configuration, and achieves a closed-loop gain approaching $-R_f$ for large current gains. The common-gate input stage sets input voltage to $(V_{bias} - V_{GS1})$ which is adjustable and can be reduced to the saturation voltage of transistor M_2, V_{DSsat2}, to keep M_2 active. The resulting photodiode bias voltage is $(V_{DD} - V_{DSsat2})$ which is about 80% of the 1V supply. Since the output is biased at V_{GS3} $(= V_{tn} + V_{DSsat3})$ and can swing down to V_{DSsat3}, the amplifier has a wide output swing equal to the threshold voltage, V_{tn}, which represents about 60% of the 1V supply.

In addition to a wide output swing, the dynamic range of the preamplifier can be further enhanced by adapting the transimpedance gain in accordance to the signal strength. However, variable-gain transimpedance amplifiers have traditionally been a challenge to stabilize [3]. The problem is overcome in this design by replacing the usual voltage amplifier with a current amplifier [4]. Doing so also realizes a constant bandwidth that is ideally independent of the transimpedance gain. This characteristic helps to reject out-of-band noise in any gain setting.

Although the variable feedback resistor, R_f, can be implemented using either an nMOS or pMOS device, an nMOS device is preferred because its decreased resistance under large negative-going signals realizes soft limiting that further enhances receiver dynamic range. Biasing the transistor is a challenge since its source and drain voltages already lie near the supply. For a 1V supply and without low-threshold devices, a charge pump is required to bias the gate above the supply. Given the sensitivity of the preamplifier, the bias voltage must be stable and free of ripple. By driving the gate directly from the output of the charge pump, a process referred to here as dynamic gate biasing (DGB), no current is drawn and the output ripple is minimized.

The charge pump is shown in Figure 14.4.2. The circuit is a voltage doubler with two unique characteristics. First, the doubler has a separate input, V_{IN}, because the bias voltage to be doubled is different from the supply. Second, the doubler can accept input levels that lie near the threshold voltage. This ability is important in low-voltage applications where the bias voltages are often only slightly higher than the device threshold voltage. The lowest voltage charge pump reported to date requires a supply voltage at least 0.5V above the threshold [5].

To overcome this limitation, the standard charge pump must be redesigned to take advantage of the full supply voltage when driving switches. This voltage doubler consists of three tightly-coupled charge pumps. The inner-most charge pump uses devices M_1 and M_2 to generate level-shifted clock signals with the full supply swing. These clock signals are used to drive the outer-most charge pump that performs the actual doubling of the bias voltage using devices M_3 and M_4. The clock signals Φ_{1Vin} and Φ_{2Vin} have a reduced voltage swing that is equal to the input voltage. The final charge pump uses devices M_5 and M_6 to generate full-swing clock signals, but here the low level is shifted to V_{SWL} that is optimized for driving the pMOS output switches M_7 and M_8. The full-swing clock signals Φ_1 and Φ_2 are generated from an integrated, non-overlapping, two-phase clock generator.

The test chip uses a commercial 0.35µm digital CMOS process with typical threshold voltages of 0.6V (nMOS) and -0.65V (pMOS). The chip architecture is shown in Figure 14.4.3. The signal path consists of the transimpedance preamplifier followed by two post gain stages that reuse the optimized transimpedance design in a transconductance-transimpedance topology. Additional circuitry using a 3V supply is incorporated on-chip only to aid testing, and is represented by the shaded blocks. The measured frequency response along the signal path is shown in Figure 14.4.4. The preamplifier alone provides a nominal transimpedance gain of 2.4kΩ over 45MHz, while the complete front-end provides 210kΩ over 50MHz. The overall gain of the front-end is adjustable from 210kΩ down to 19kΩ by varying the gate bias voltage from 1.68V to 2V. On-chip RC filtering of the bias voltage, V_{DGB}, reduces ripple due to charge injection and isolates the gain stages. At the maximum gain setting, the input-referred noise current density is flat across the passband and equal to $11pA/Hz^{1/2}$. The measured eye-diagram of a free-space optical link at maximum gain and 75Mb/s is shown in Figure 14.4.5. A summary of chip performance is given in Figure 14.4.6, and a micrograph of the test chip is shown in Figure 14.4.7.

Acknowledgements:
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References:
[1] M. Nakamura and N. Ishihara, "1.2V, 35mW CMOS optical transceiver ICs for 50Mbit/s burst-mode communication," Electronic Letters, vol. 35, no. 5, pp. 394-395, 1999.
[2] V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, "900mV differential class AB OTA for switched opamp applications," Electronics Letters, vol. 33, no. 17, pp. 1455-1456, 1997.
[3] K. Phang and D.A. Johns, "A CMOS Optical Preamplifier for Wireless Infrared Communications," IEEE Trans. Circuits and Systems II, vol. 46, no. 7, pp. 852-859, July 1999.
[4] B. Wilson and J. D. Drew, "Novel Transimpedance Amplifier Formulation Exhibiting Gain-Bandwidth Independence," IEEE Proc. Int. Symp. Circuits and Systems, vol. 1, pp. 169-172, June 1997.
[5] J.-T. Wu and K.-L. Chang, "MOS Charge Pumps for Low-Voltage Operation," IEEE J. Solid-State Circuits, vol. 33, no. 4, pp. 592-597, April 1998.

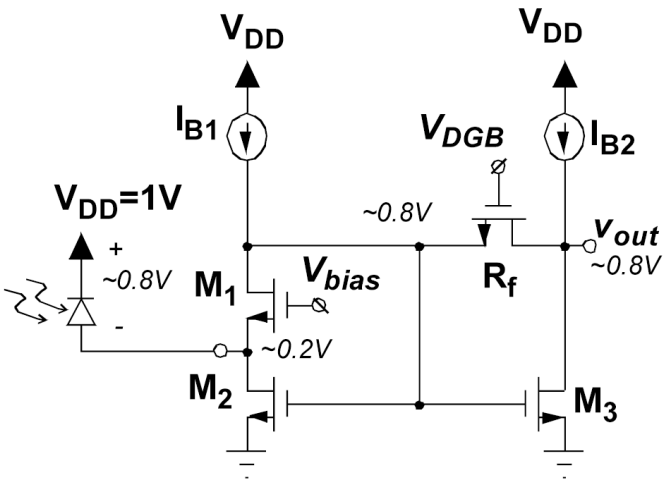


Figure 14.4.1: 1V transimpedance amplifier.

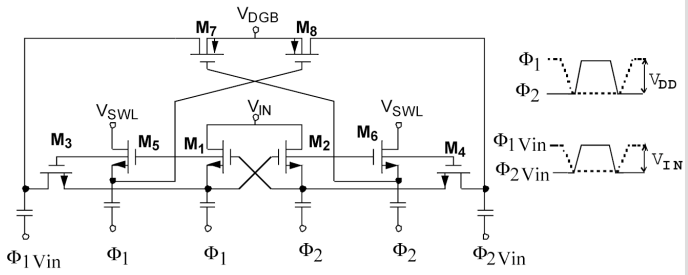


Figure 14.4.2: Sub-1V bias voltage doubler.

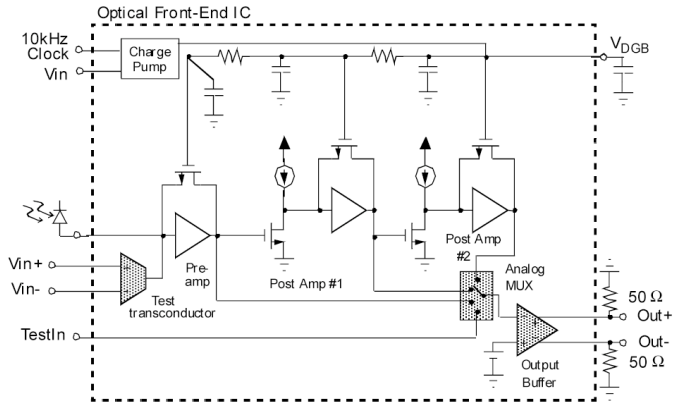


Figure 14.4.3: Chip block diagram.

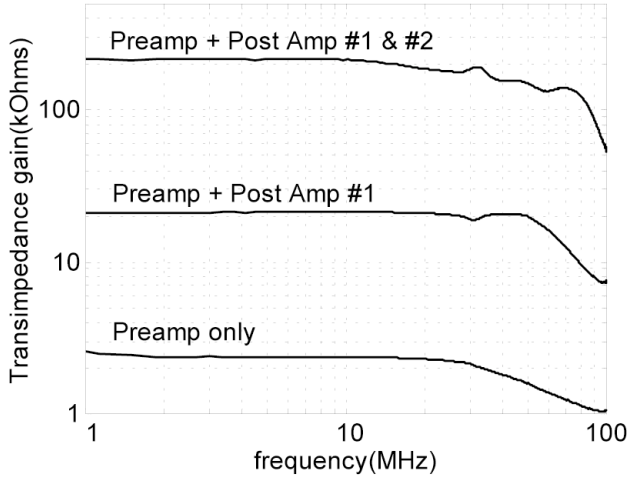


Figure 14.4.4: Measured frequency response.

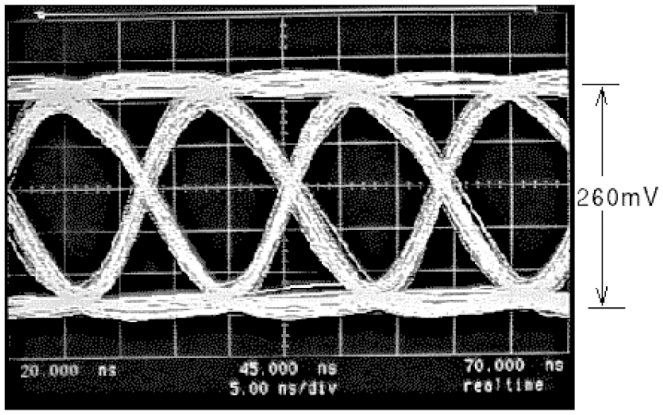


Figure 14.4.5: Eye diagram for 75Mb/s optical link.

Technology	0.35μm CMOS (V_t:0.6 and -0.65V
Supply voltage	1V
Power dissipation	1mW
Photodiode capacitance	1pF
Max. gain	210 kΩ
Bandwidth	50MHz
Input noise	11pA/√Hz
Max. input current	40μA
Active area	0.13mm^2

Figure 14.4.6: Performance summary.

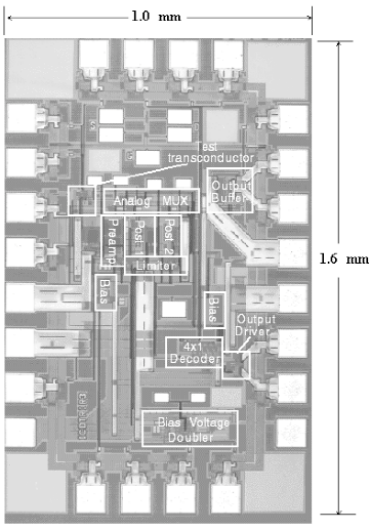
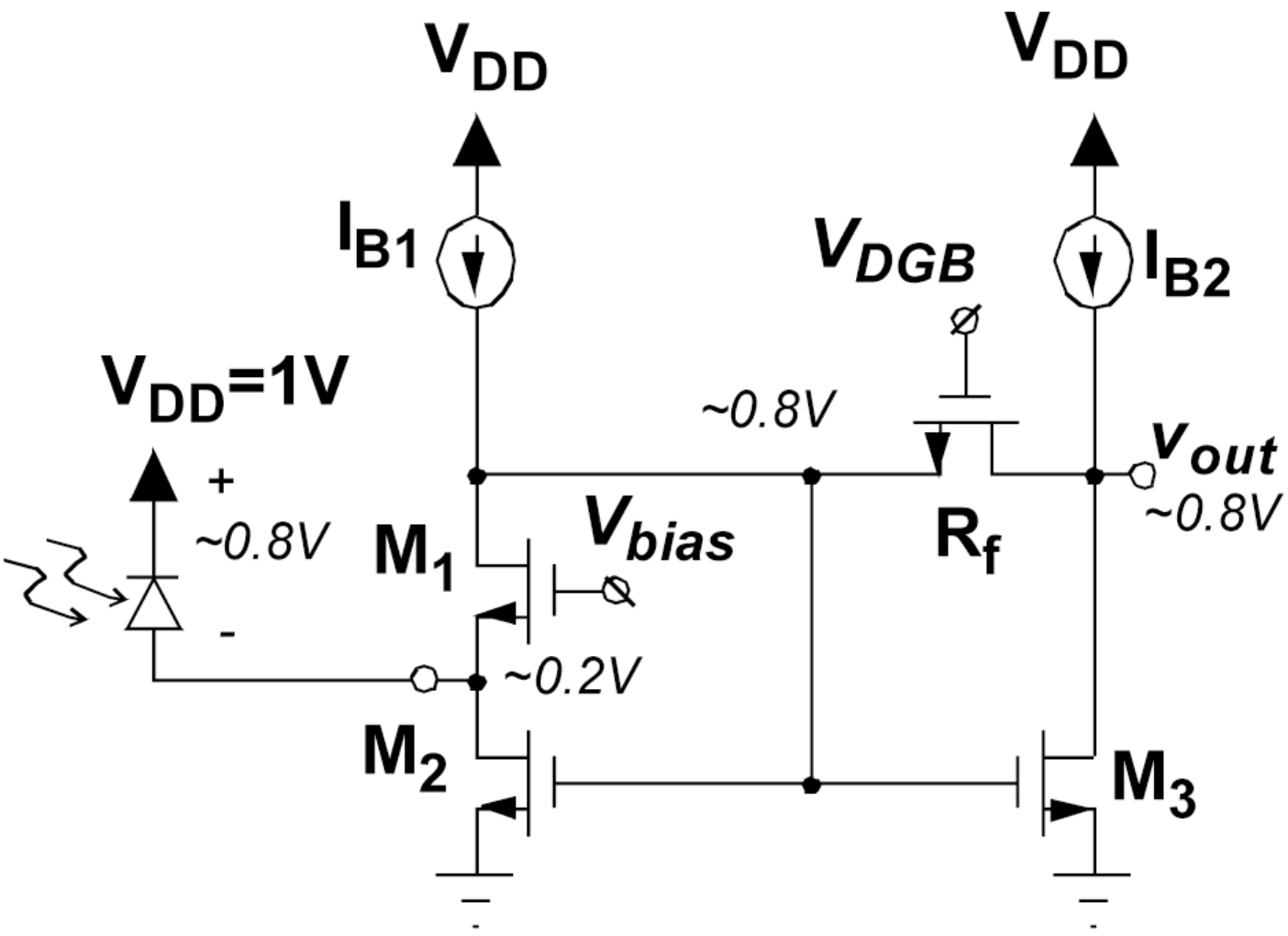


Figure 14.4.7: Die micrograph for 1V 1mW CMOS optical receiver front-end.



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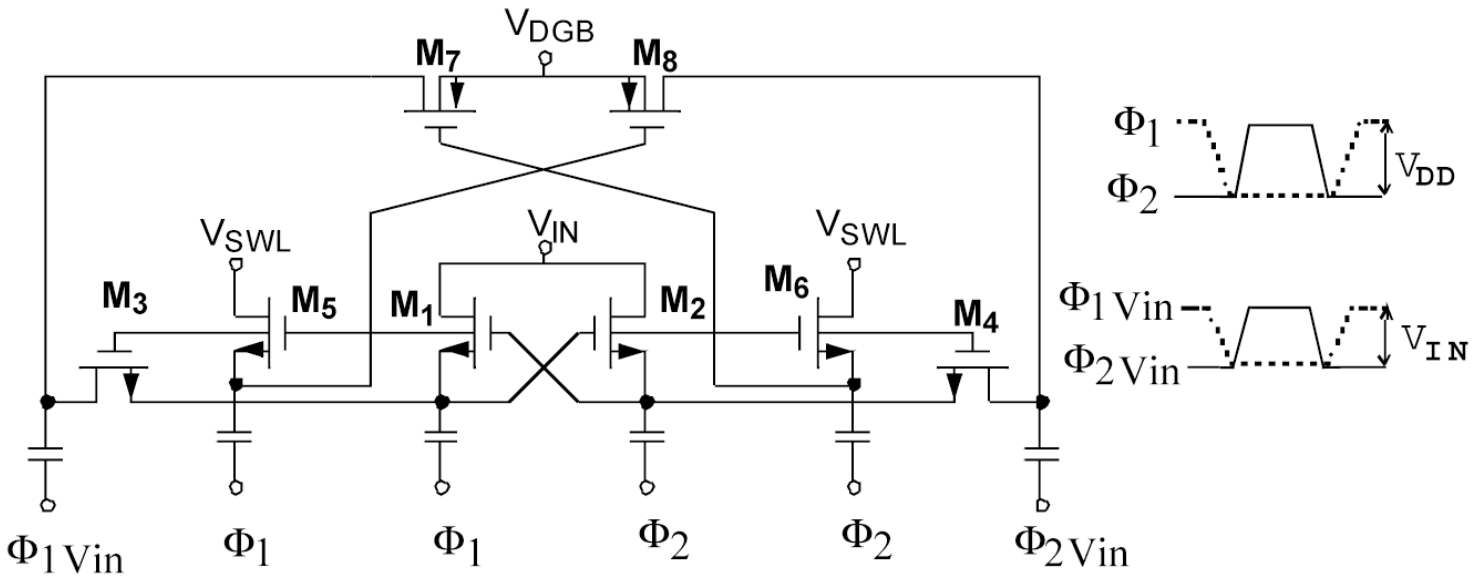

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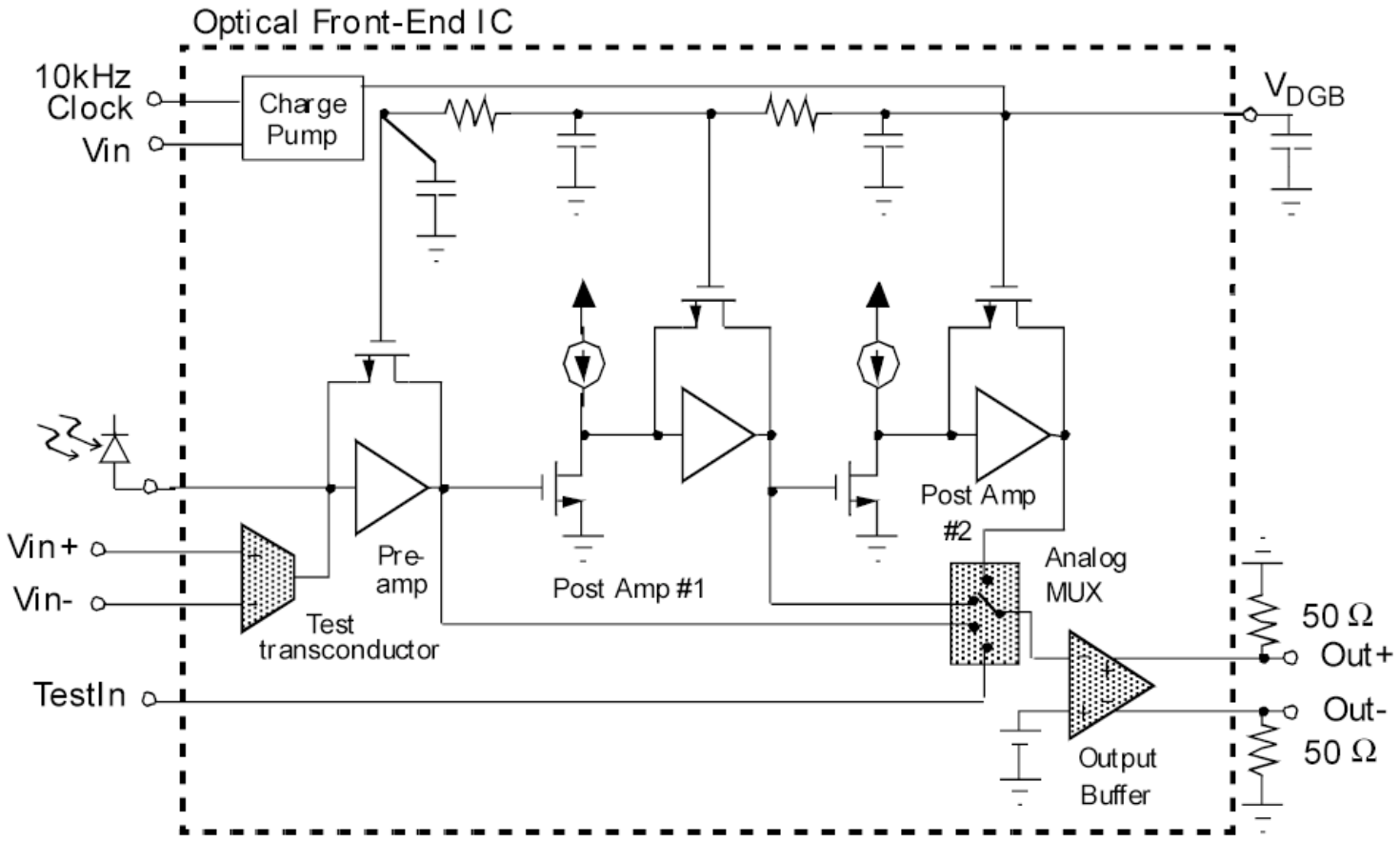

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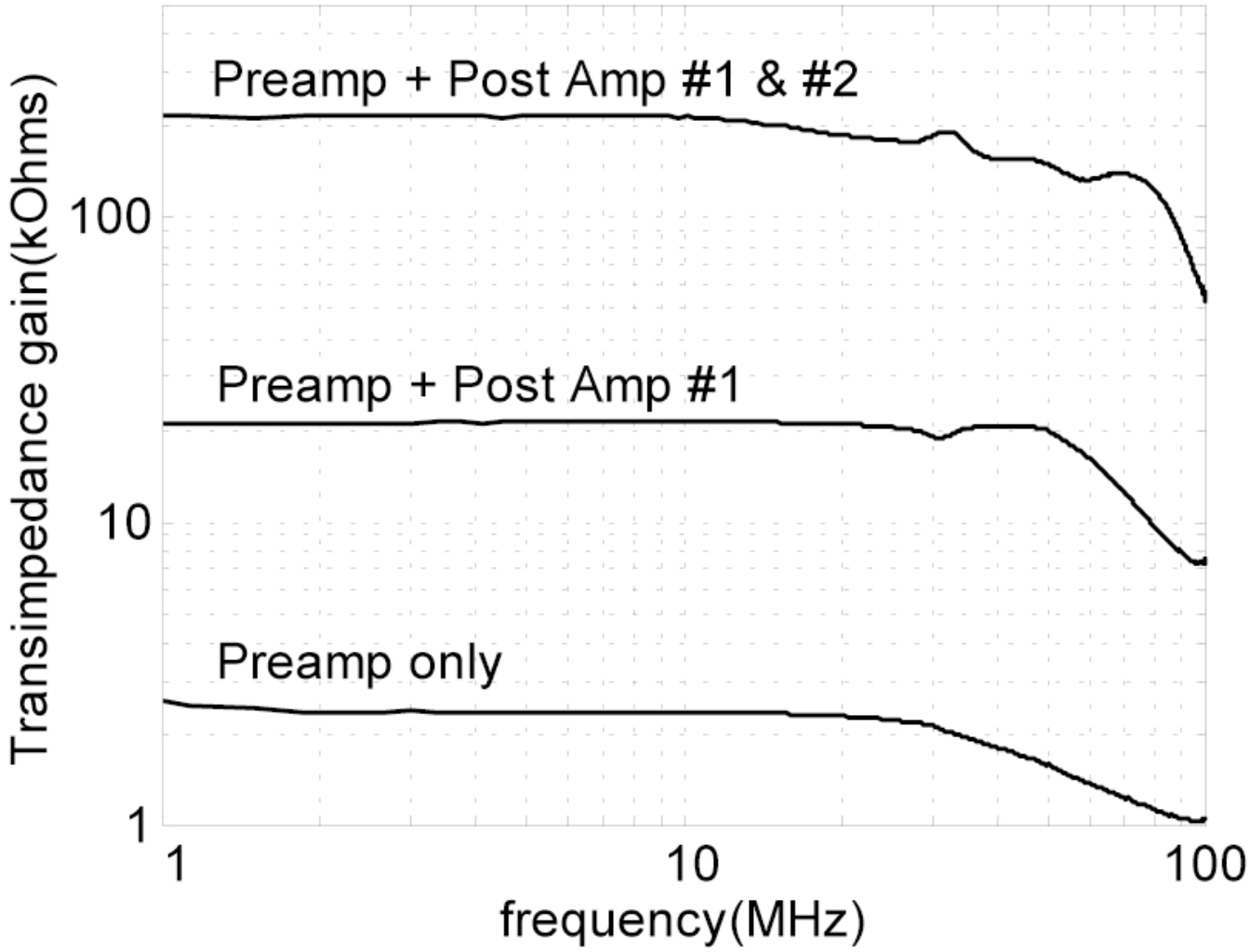
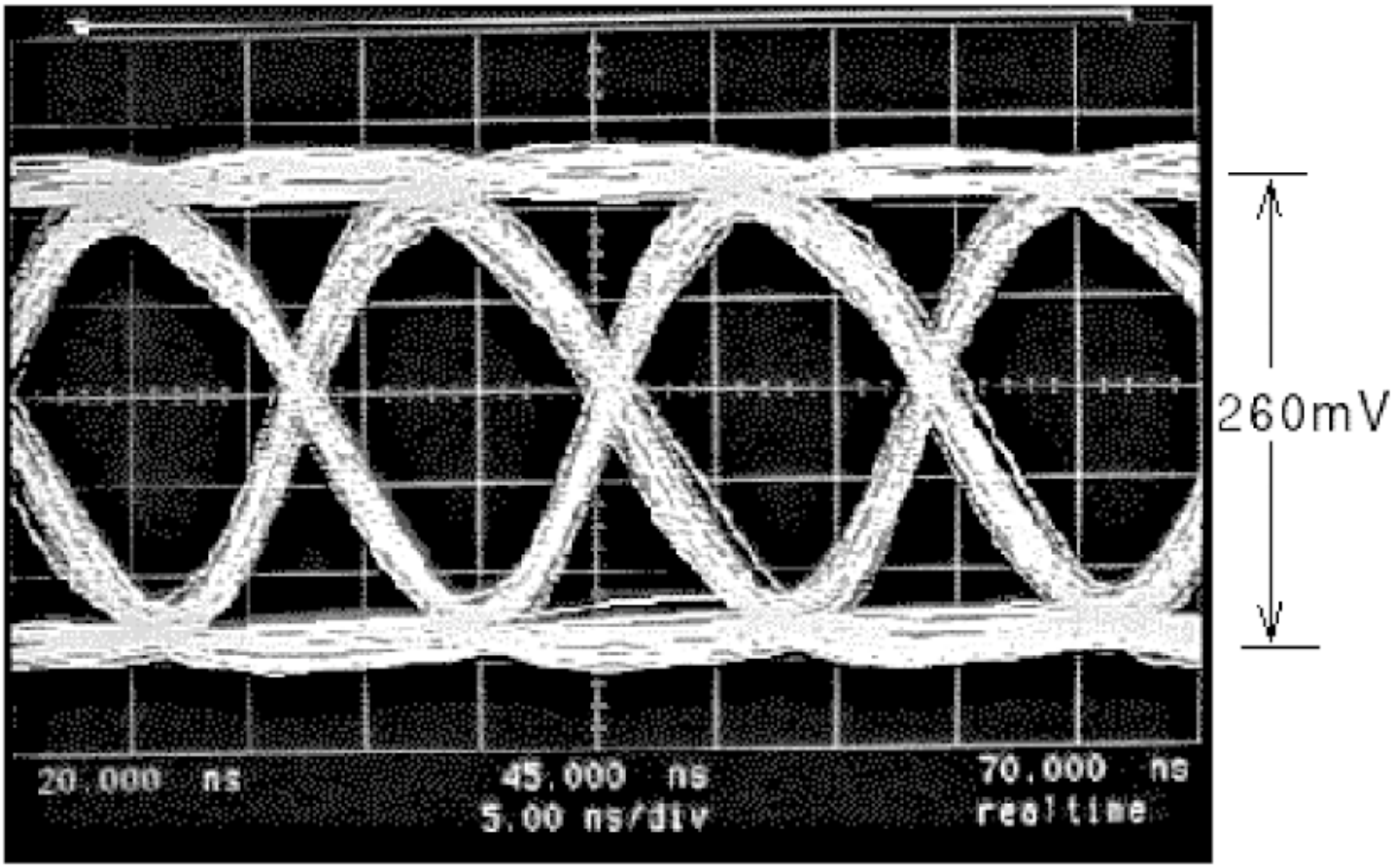


Figure 14.4.4: Measured frequency response.



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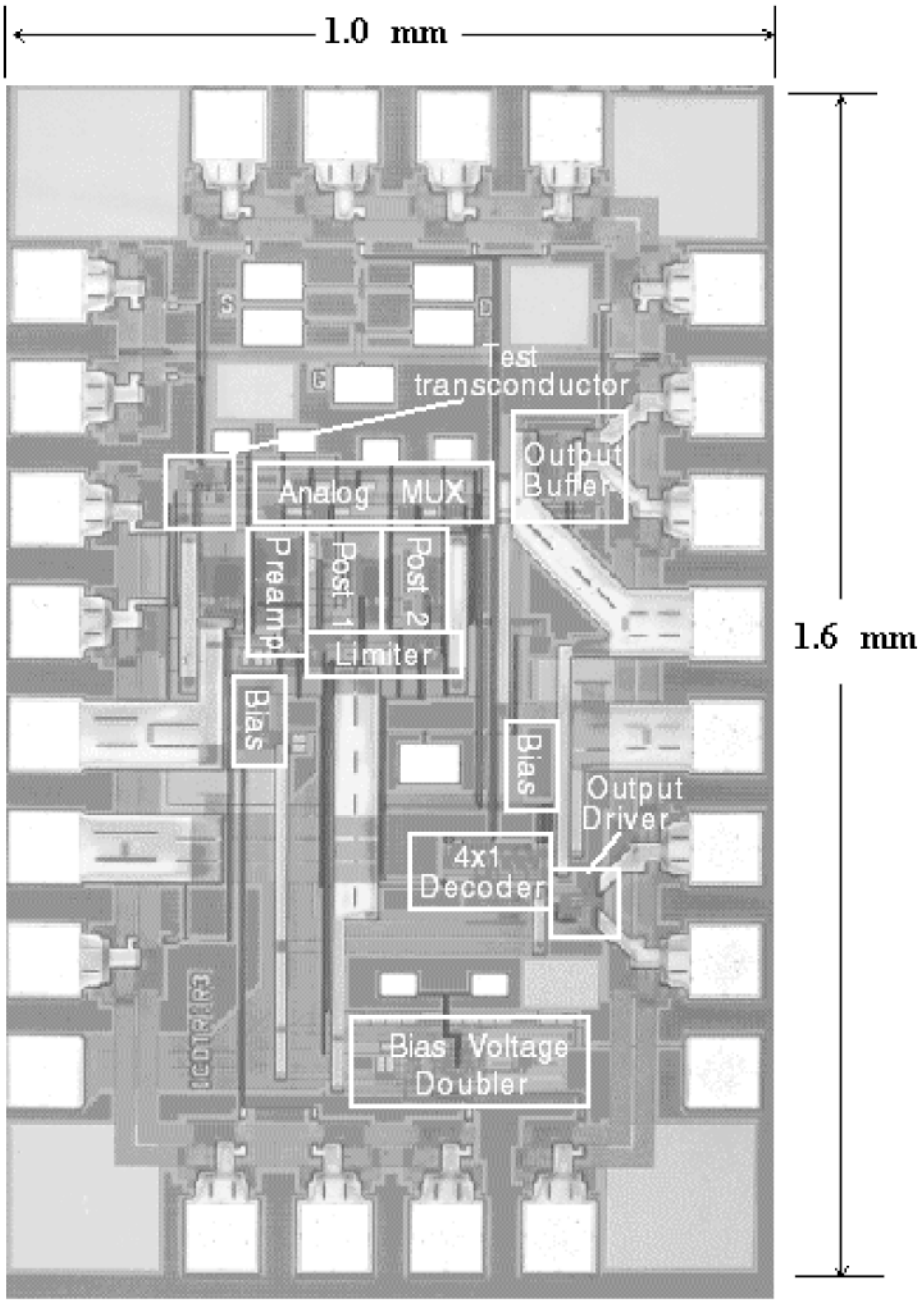

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