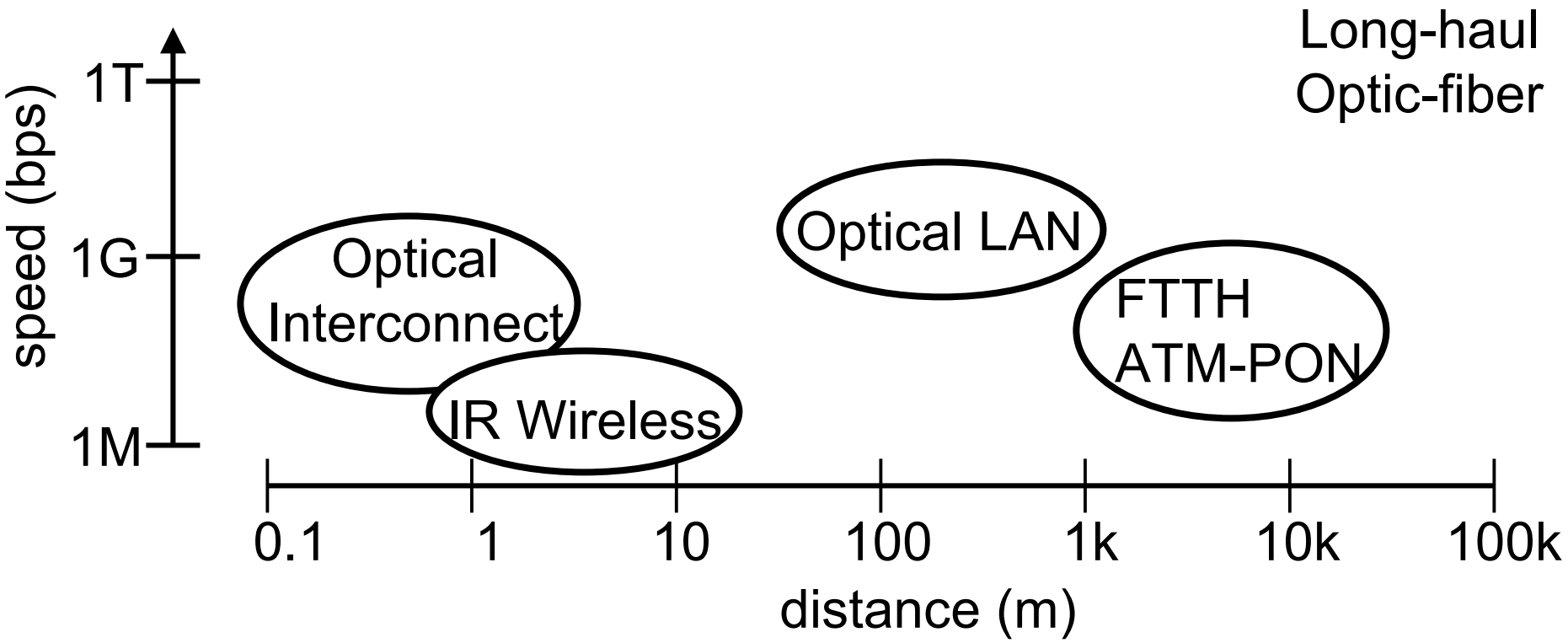
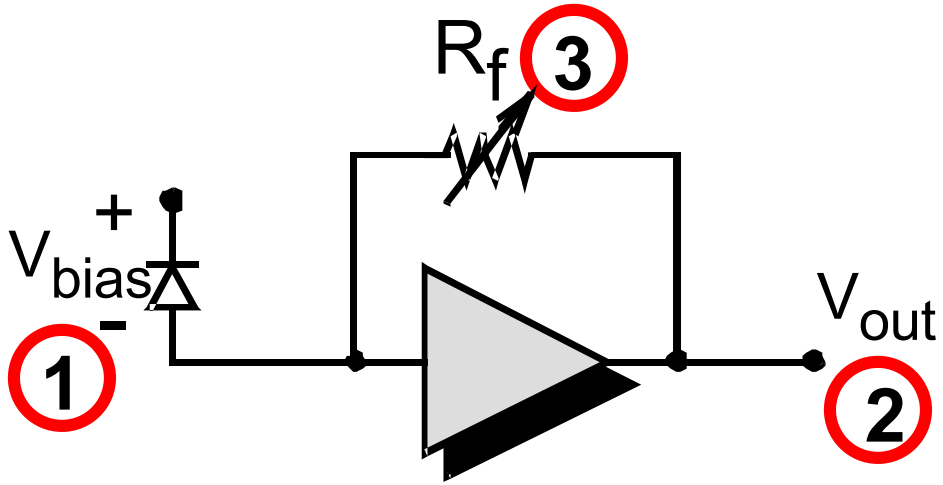
Motivation

Emerging applications of optical communications requiring higher integration and lower power:



Objective

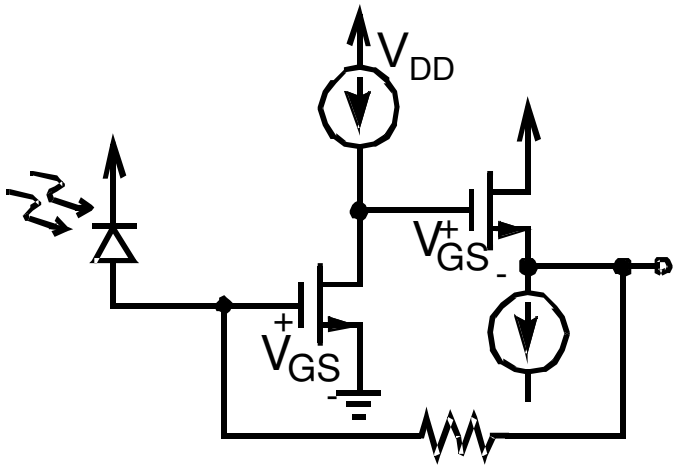
To develop a 1V optical preamp in conventional CMOS



- Design Challenges
  1. Maximizing photodiode bias voltage
  2. Wide output signal swing
  3. Achieving variable-gain for wider dynamic-range

Conventional TIA Topologies

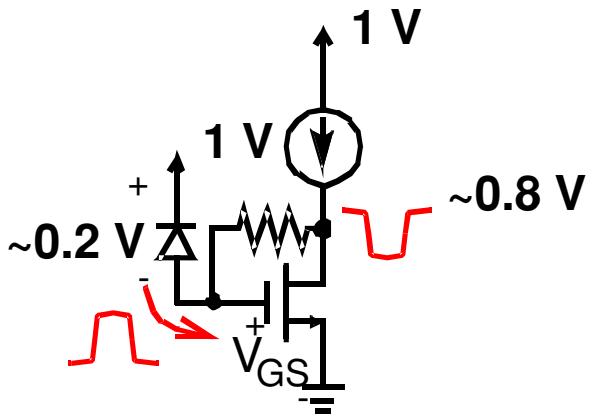
Two-stage



$$V_{DD,min} > 2V_{GS} \approx 1.6V$$

✘ Unsuitable for 1V operation

Single-stage



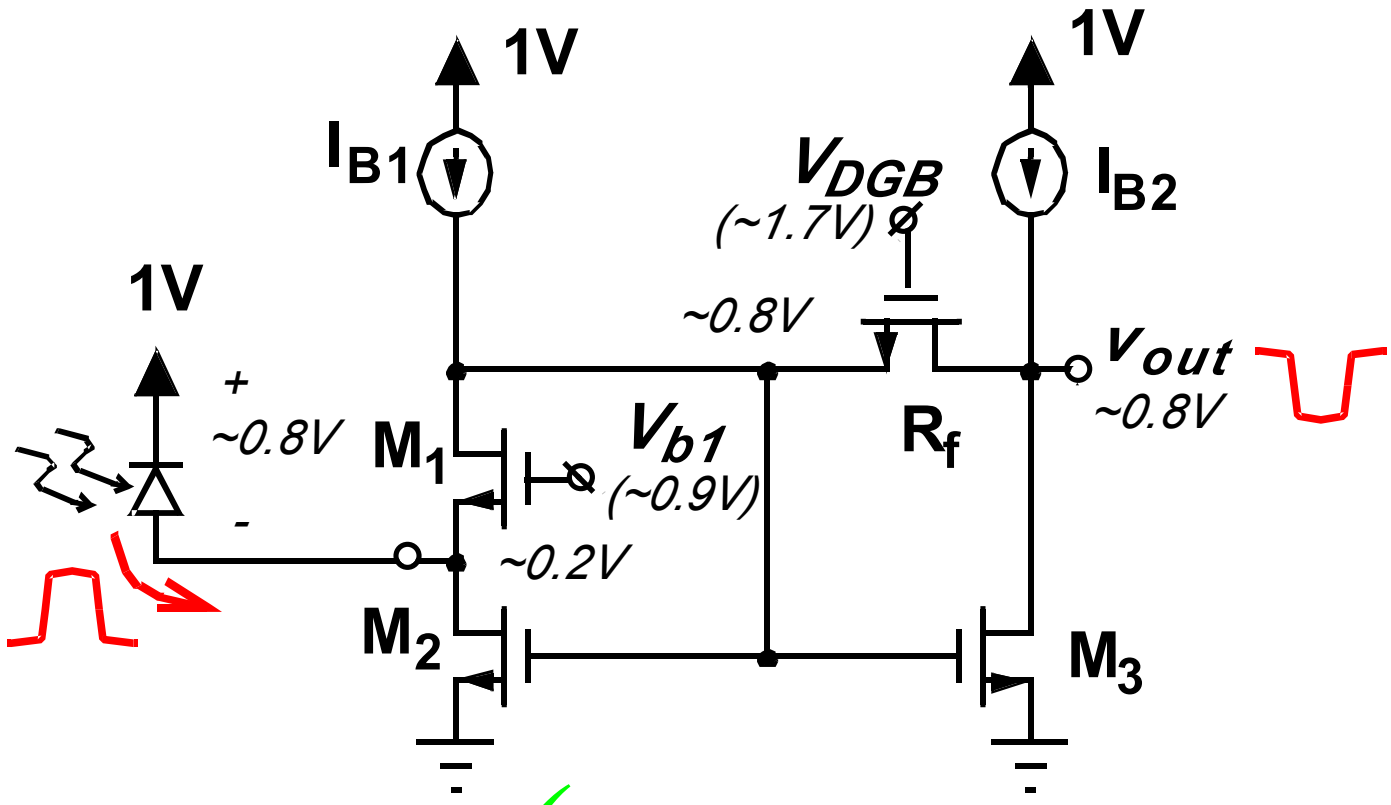
✓ Capable of 1V operation

✓ Large output swing, V_t=0.6V

✘ Small PD bias voltage ~ 0.2V

Proposed Low-Voltage TIA

LV current amplifier in transimpedance configuration



- ✓ 1V operation
- ✓ Large output swing, V_t=0.6V
- ✓ Large PD bias, $V_{DD} - V_{DSsat2}$ ~0.8V

Design Optimization

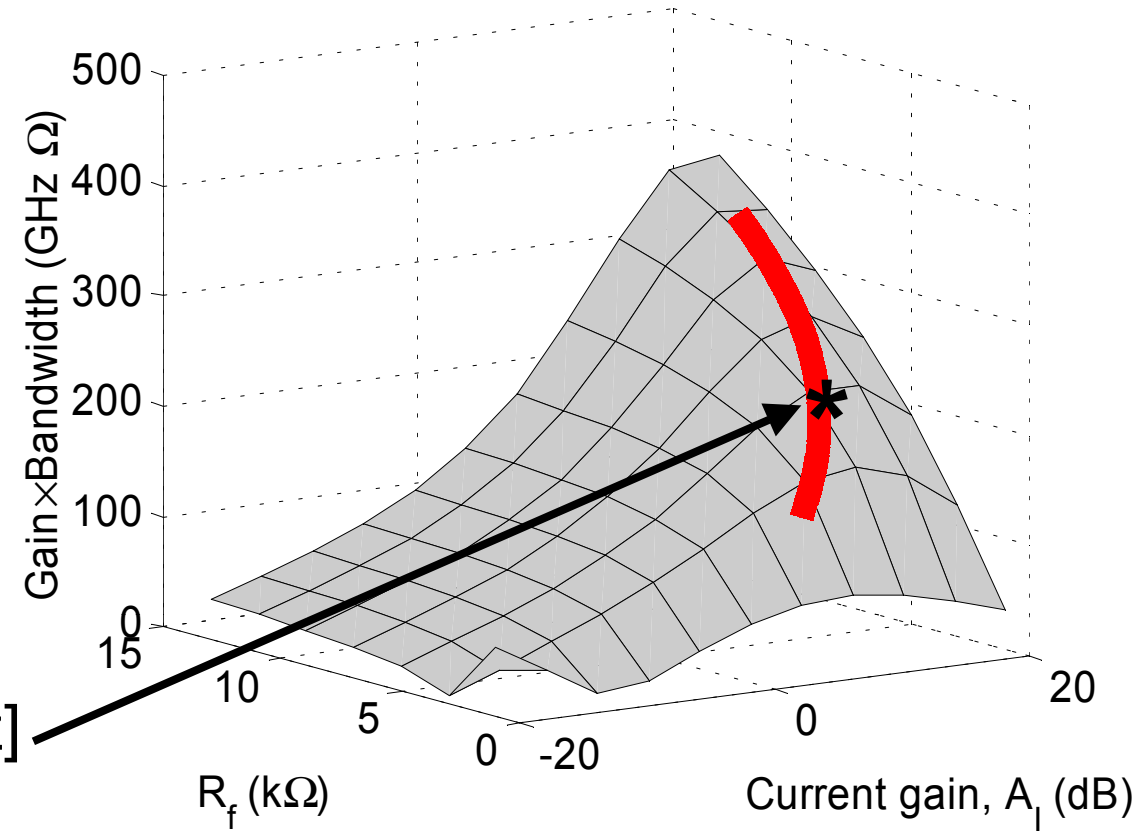
Bandwidth

$$\omega_{-3dB} = \frac{g_{m1}(1 + A_I^{-1})}{C_{gs1} + C_{db2} + g_{m1} R_f C_{out} / A_I}$$

Gain

$$\frac{v_{out}}{i_{PD}} = \frac{A_I}{1 + A_I}(1/g_{m1} - R_f)$$

$$A_I = \frac{g_{m3}}{g_{m2}}$$

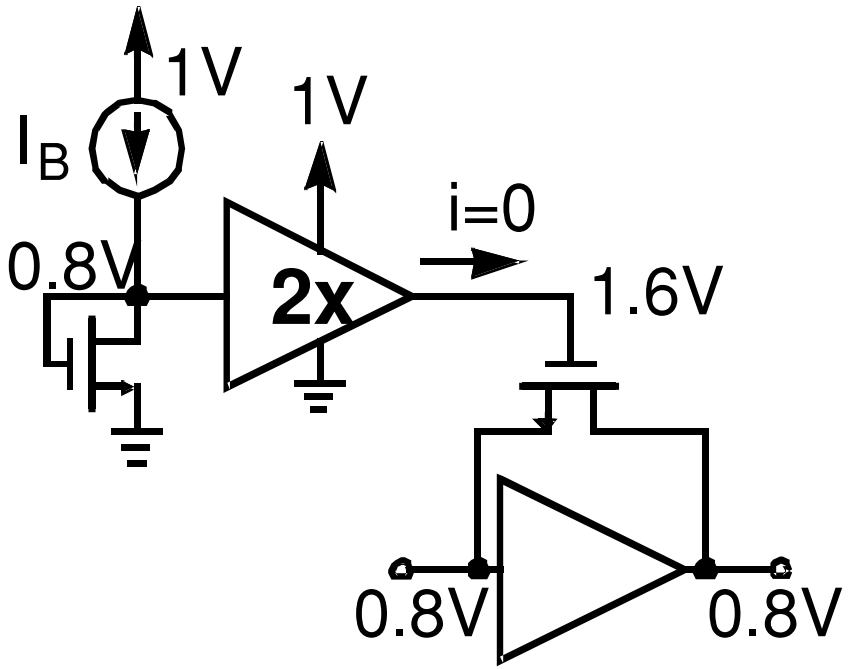


Optimum point [50MHz]
(5kΩ,12dB)

Achieving Variable Gain

- Gate voltage of NMOS resistor must be biased higher than the 1V supply
- **Solution:** Use voltage doubler to directly bias the gate

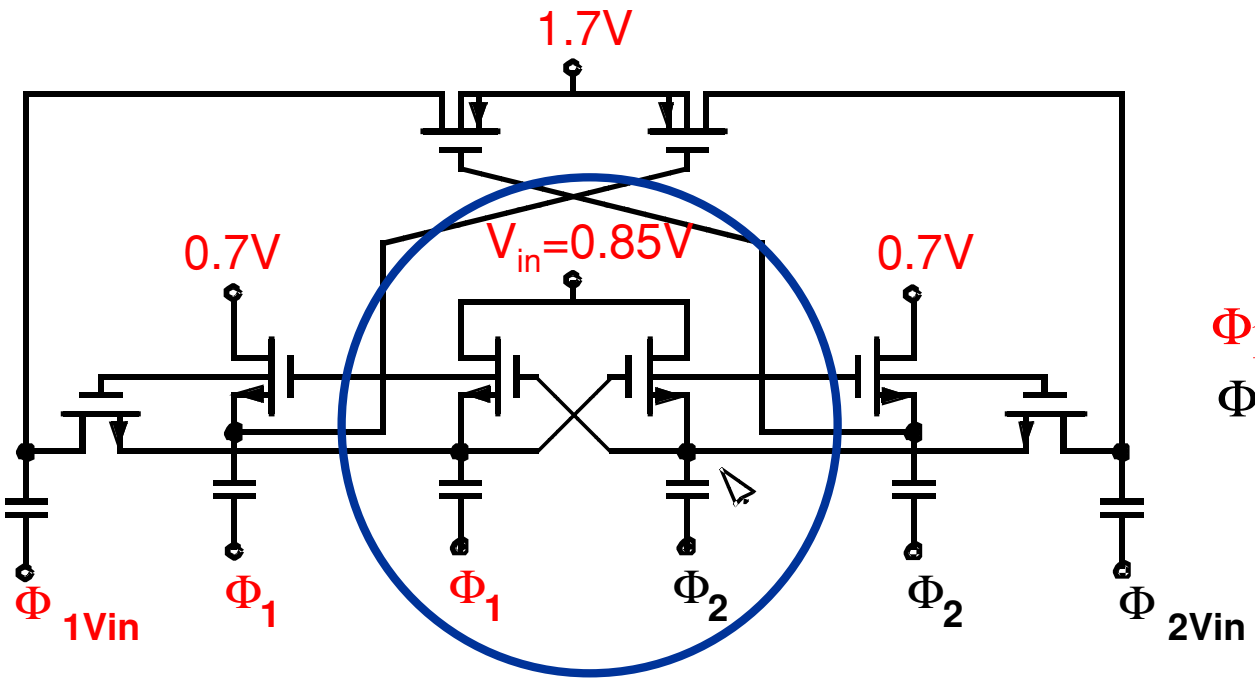
→ **Dynamic Gate Biasing**



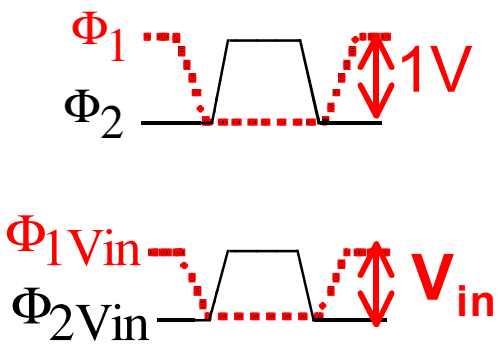
✓Charge pump supplies no current, minimizing ripple

Sub-1V Bias VoltageDoubler

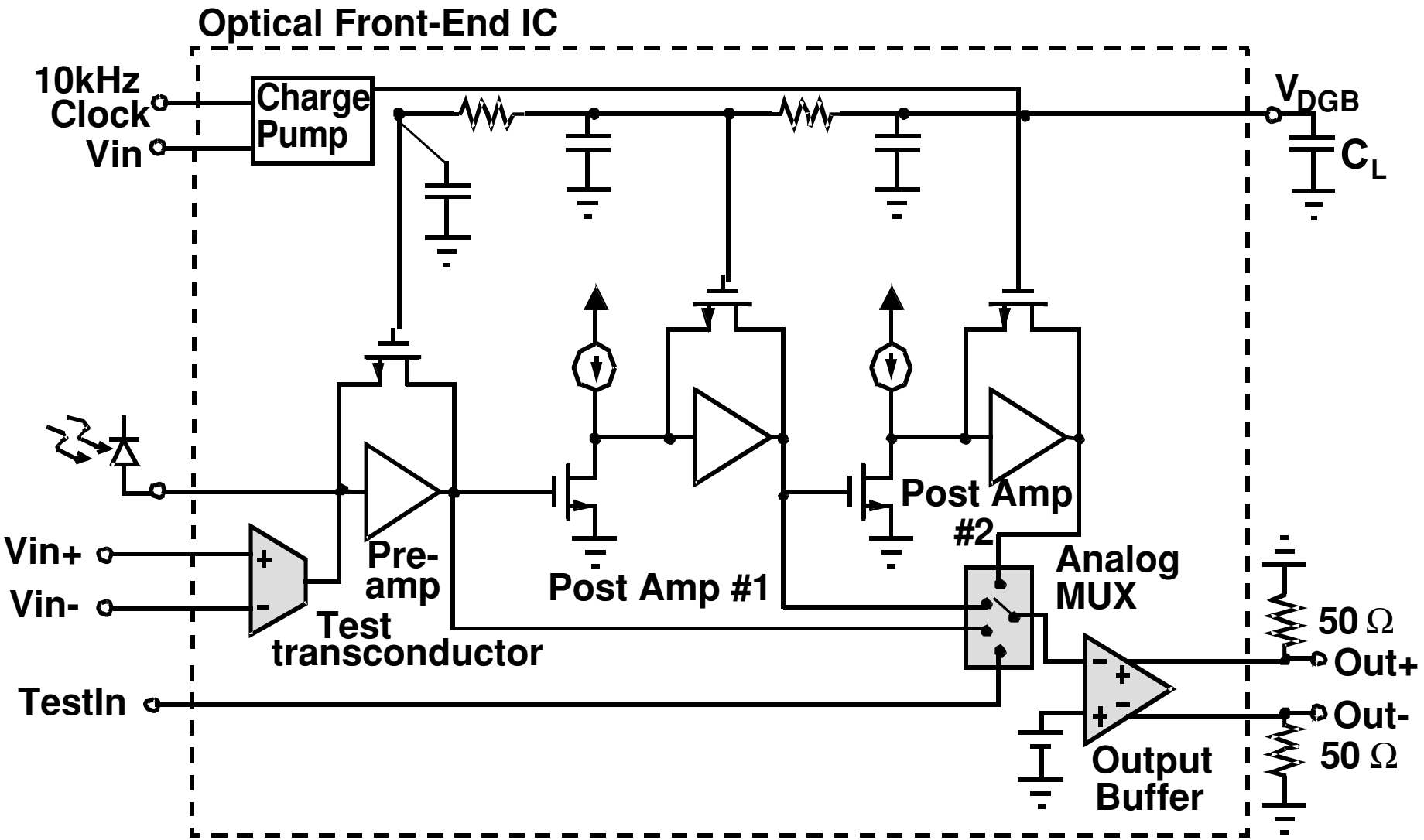
- Uses full supply swing for driving switches
- A separate input for the bias voltage
- Capable of doubling voltages near the device threshold

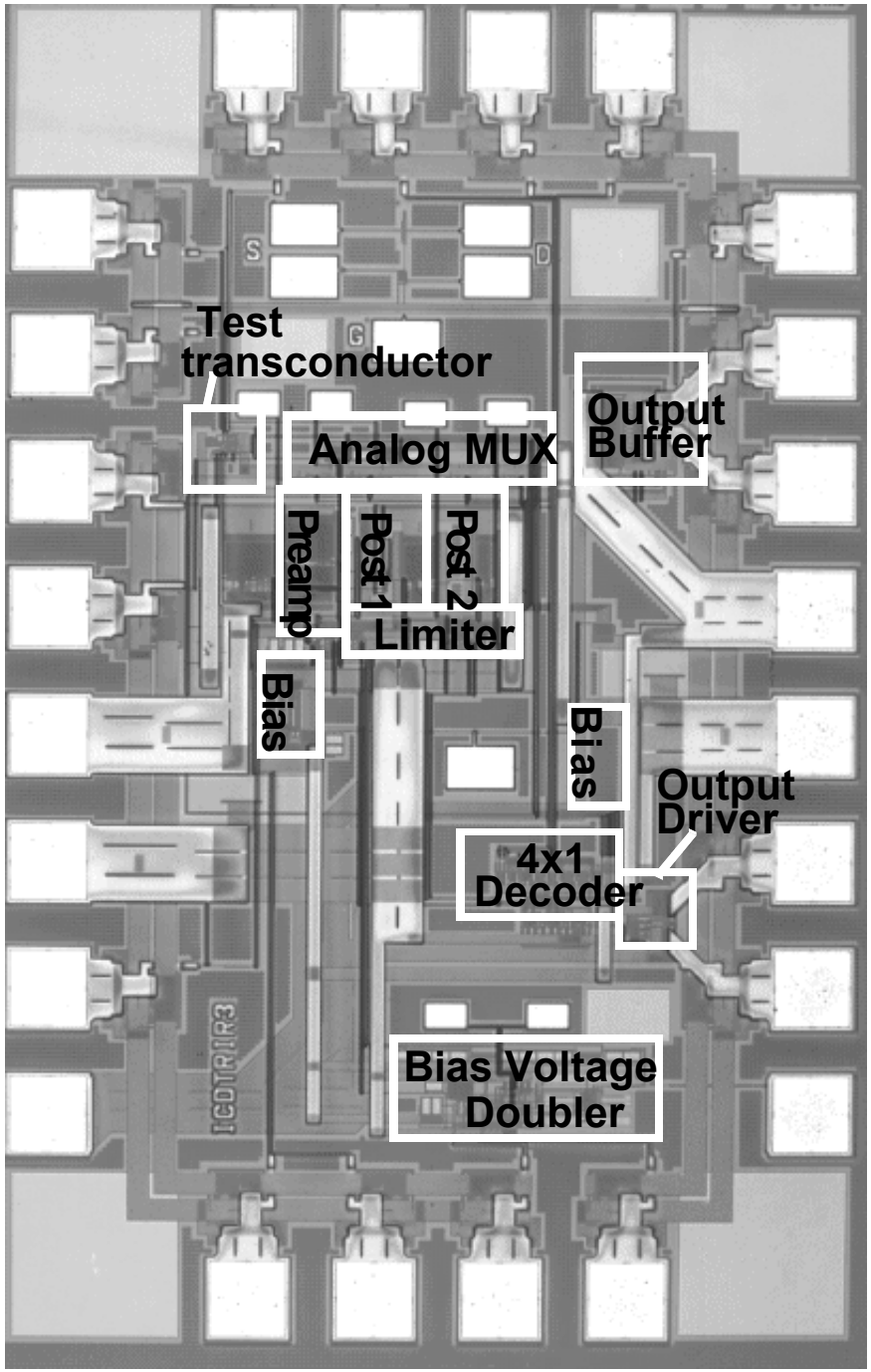


Basic charge pump

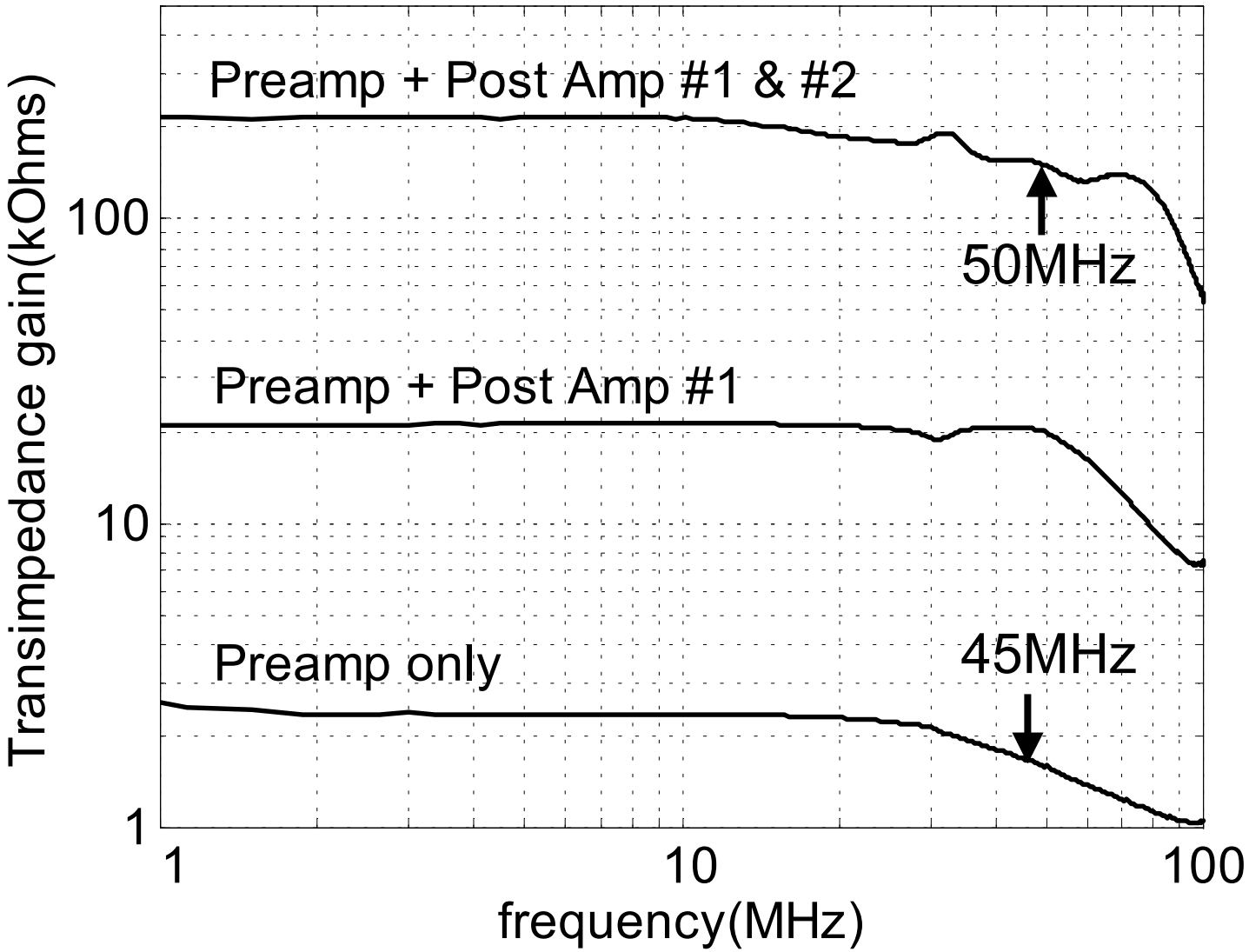


Chip Block Diagram

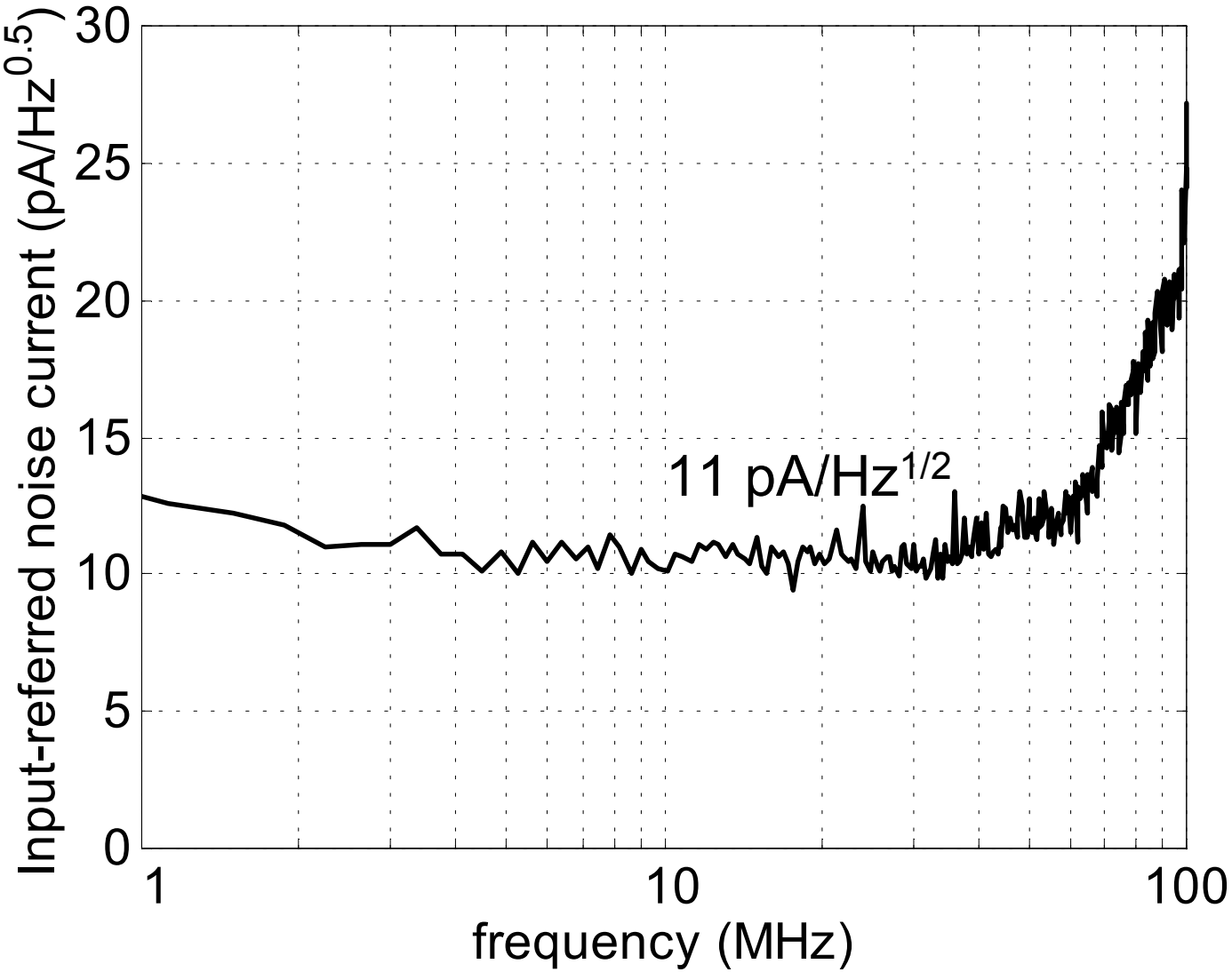




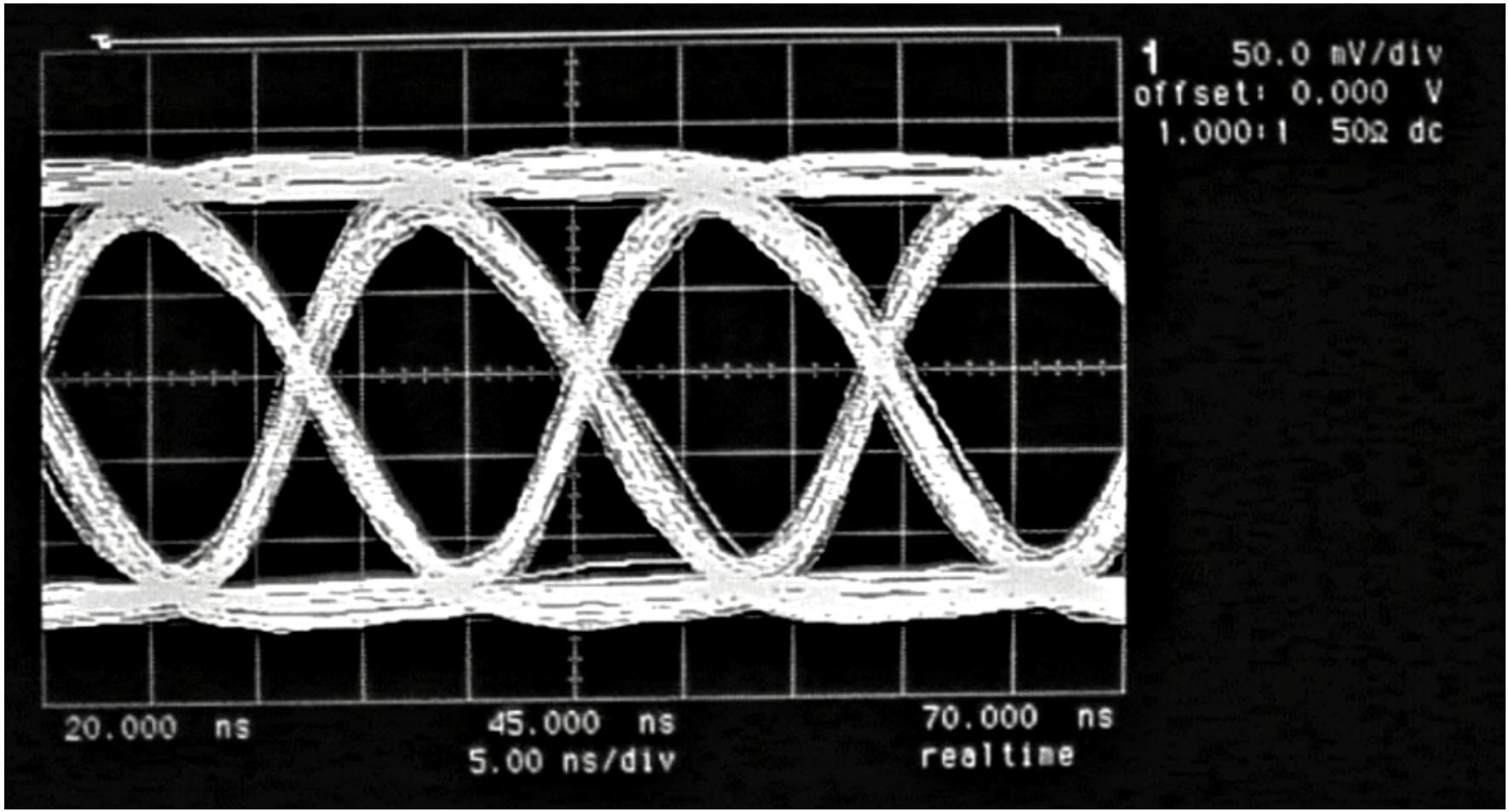
Experimental Frequency Response



Input Noise Spectrum



Eye Diagram

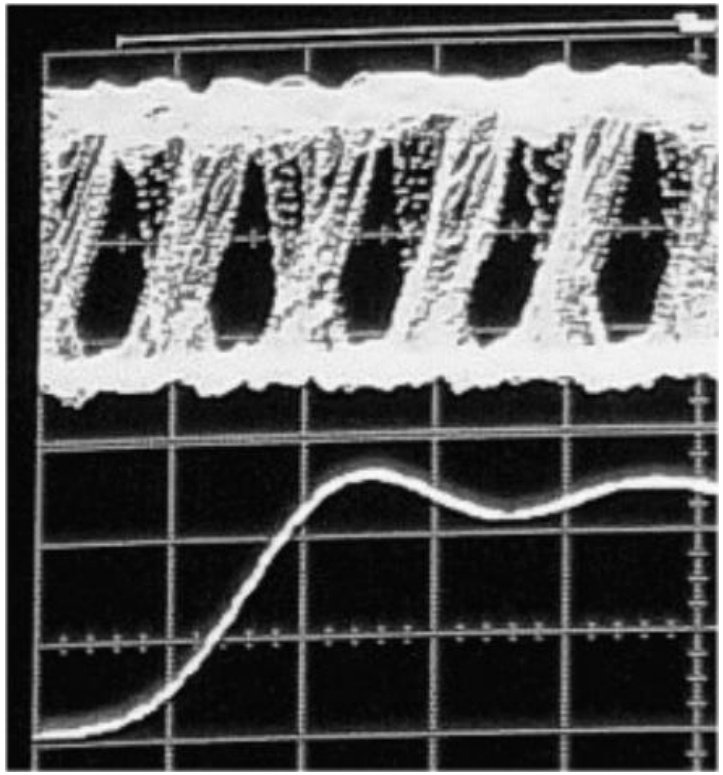


75 Mb/sec free-space optical link

Controlling Charge Injection

Eye Diagram

Doubler Clock



No external capacitor
(10 pF on chip)

With 200pF
external capacitor

Performance Summary

Technology	0.35 μm CMOS (V_t:0.6 and -0.65V)
Supply voltage	1 V
Power dissipation	1 mW
Photodiode capacitance	1 pF
Max. gain	210 kΩ
Bandwidth	50 MHz
Input noise	11pA/√Hz
Max. input current	40 μA
Active area	0.13 mm^2

Summary

- Low-voltage TIA topology maximizes PD bias voltage and output swing
- CMOS TIA achieves 1V operation without low-threshold devices
- Sub-1V bias voltage doubler used for the dynamic biasing of MOSFET gates