DISTORTION ANALYSIS USING SIGNAL FLOW GRAPHS AND VOLTERRA SERIES

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ABSTRACT

This paper describes a graphical method of nonlinear circuit analysis. The method combines circuit analysis using driving-point impedances and signal flow graphs with distortion analysis using the Volterra series. The result is a method of distortion analysis which is more intuitive and flexible than traditional methods. The method is demonstrated in the analysis of a common-emitter amplifier in which the second- and third-order harmonic distortion ratios are determined. The method is also applied to comparing the distortion of different voltage buffer circuits based on an emitter follower and on a differential pair with unity gain feedback.

INTRODUCTION

Distortion is a key issue in the design of many types of circuits. The Volterra series has long been used to analyze distortion in analog circuits[1]. Unlike numerical simulations which give no information about the source of the distortion, closed form expressions for distortion components in terms of circuit parameters can be found using the Volterra series. Unfortunately, the method of presenting the Volterra series analysis can be complex, and its results give little instinct into how the distortion is affected by the circuit parameters. Consequently, the Volterra series is often under-utilized by circuit designers.

In this paper we demonstrate how signal flow graphs (SFG), traditionally applied to linear systems, can be combined with the Volterra series to present a more intuitive analysis of distortion when the circuit behaves in a weakly nonlinear way. The SFG is derived using driving-point impedance analysis, or the DPI/SFG method proposed by Ochoa[2][3]. The method is demonstrated in the distortion analysis of a common-emitter amplifier. Simulation results are provided to demonstrate the accuracy of the expressions derived using the SFG. The SFG method is used to obtain apriori distortion figures and trends prior to lengthy and involved simulations involving transient analysis and FFT. Finally, we demonstrate how this method can be used by designers to gain insight through the distortion analysis of two different buffer circuits realizations that are based on an emitter follower and a differential pair.

THE VOLTERRA SERIES

Many practical circuits can be assumed to behave in a weakly nonlinear way, and under this condition, closed form expressions for the nonlinearity can be obtained using the Volterra series. The Volterra series for a circuit is generally represented as a summation of n^{th} order operators as shown in Figure 1, where

$$H_n[x(t)] = \int_{-\infty}^{\infty} \cdots \int_{-\infty}^{\infty} h_n(\tau_1, \ldots, \tau_n) x_1(t-\tau_1) \cdots x_n(t-\tau_n) d\tau_1 \cdots d\tau_n \qquad (1)$$

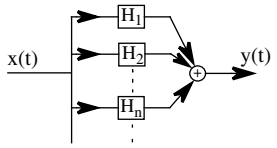

Figure 1. Block Diagram representation of the Volterra Series

The function $h_n(\tau_1,...,\tau_n)$ in (1) is what is known as a Volterra kernel. $H_n(s_1,...,s_n)$, the multi-dimensional Laplace transform of $h_n(\tau_1,...,\tau_n)$, can be used to calculate the magnitude of distortion components. The complex frequency variable is given by $s_i = \sigma_i + j\omega_i$ for $i = 1, 2, \ldots, n$. The representation of the nonlinearity as a summation of operators of different order operating on a signal allows us to examine the contribution of each order of nonlinearity individually. Dominant contributions can then be identified and analyzed. For weakly nonlinear circuits that are excited by small signals, usually only the first three terms are retained. In addition, second-order components are largely cancelled in fully differential designs.

AMPLIFIER DISTORTION ANALYSIS

As an example, we will analyze the distortion in the common-emitter (CE) amplifier shown in Figure 2. Our analysis is based on the distortion analysis presented in [4][5] using the Volterra Series. The nonlinearities considered in this circuit are due to the resistor r_π and the transconductance g_m. These nonlinearities are associated with the exponential I-V characteristic of the

transistor: $i_B = (I_S/\beta)e^{v_{BE}/V_T}$. This characteristic can be approximated using the first three terms of a power series.

$$i_B \approx I_B + g_\pi v_{be} + K_{2g\pi} v_{be}^2 + K_{3g\pi} v_{be}^3 \quad (2)$$

$$i_C = \beta i_B \approx \beta I_B + g_m v_{be} + K_{2gm} v_{be}^2 + K_{3gm} v_{be}^3 \quad (3)$$

where I_B is the base dc bias current, and the power series coefficients are given by

$$K_{2g\pi} = K_{2gm}/\beta = g_m/(2\beta V_t), K_{3g\pi} = K_{3gm}/\beta = g_m/\left(6\beta V_t^2\right) \quad (4)$$

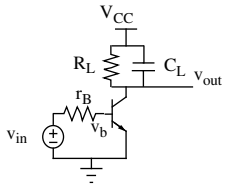

Figure 2. Schematic of the common emitter amplifier circuit

The nonlinear terms in (2) and (3) can be represented in the schematic by the two current sources $i_{NLg\pi}$ and i_{NLgm} as shown in Figure 3. The nonlinear currents are given by:

$$i_{NLg\pi} = K_{2\pi} v_{be}^2 + K_{3\pi} v_{be}^3 \quad (5)$$

$$i_{NLgm} = K_{2gm} v_{be}^2 + K_{3gm} v_{be}^3 \quad (6)$$

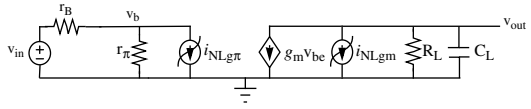

Figure 3. Small signal equivalent circuit with nonlinearities

The linear, second-, and third-order responses of the amplifier can be represented together in a single SFG as shown in Figure 4. The Volterra Series has allowed us to separate the response of each order and to create a SFG where the node voltages directly correspond to the Volterra kernels[5][6]. We can obtain the Volterra kernels directly by applying a normalized input, v_{in}=1, and by solving the output signal for each order system.

Boxes are drawn around the SFG of the linear small-signal circuit to emphasize that the same basic linear network is solved for each order subsystem but with different nonlinear inputs. The linear properties of SFGs such as superposition still hold within these boxes. Three additional symbols in the graph are introduced which are not usually used in SFGs since they represent nonlinear operations: the x^2 block, the x^3 block, and the multiplication block. The nonlinear operations appear between the boxed SFG layers and determine the nonlinear signals which excite each system. The number of frequency variables, s_i, required for each level of response is equal to the order of the kernel. The following sections discuss the development of the SFG in Figure 4.

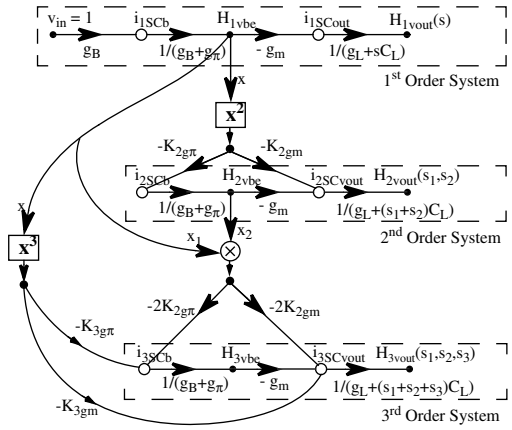

Figure 4.Combined SFG for solving the kernels of the circuit

LINEAR SYSTEM

Our first step is to analyze the linearized circuit shown in Figure 5 by removing all the sources of nonlinearities in the circuit, and to determine the first-order SFG block, H_1. The SFG shown in Figure 6 can be easily derived from the circuit using the DPI/SFG method [2][3], where the black circles represent node voltages, and the white circles represent the short-circuit currents at the same nodes. To obtain the Volterra kernel $H_{1vout}(s)$, we normalize the input and rename nodes as shown in the first-order system in Figure 4. The resulting transfer function is

$$H_{1vout}(s) = -g_m g_B/((g_B + g_\pi)(g_L + sC_L)) \quad (7)$$

The notation we use for the transfer function $H_{1vout}(s)$ is such that the subscript '1' refers to a 1st order kernel transform and the subscript 'vout' refers to the output node.

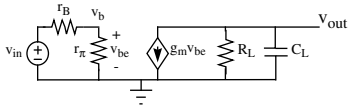

Figure 5. Linearized small signal equivalent circuit

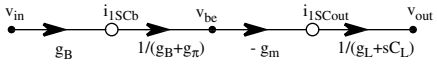

Figure 6. SFG of the linearized circuit in frequency domain

HIGHER ORDER SYSTEMS

Kernel transforms of higher order are found by solving the same basic linear network with a few changes. The series expansion expression in (2) suggests that the linear network is no longer directly excited by the input signal, but by new excitations in the form of nth order nonlinear current sources that represent the nonlinear components. The sources are placed in parallel with each nonlinear element and the orientation of each source is the same as the corresponding controlled current in the

original circuit. The nonlinear signals then propagate through the rest of the linear circuit. The circuit to be solved is shown in Figure 7[5]. The voltages and currents are represented by the same notation of the kernels. The same network is solved for each order but at different frequencies and with different expressions for the nonlinear sources. In [4] it was shown that the nonlinear response of order n can be determined in terms of the lower order nonlinear responses.

To solve for the second-order kernel, the SFG is obtained from the circuit in Figure 7 after setting n=2, note that the input voltage is short-circuited. In the SFG of Figure 4, the contribution of the second-order nonlinear current sources is represented by the additional branches going into the short-circuit current nodes, i_{2SCb} and i_{2SCout}. Noting that H_{vbe} is not a function of frequency, then the nonlinear current sources $i_{2NLg\pi}$ and i_{2NLgm} can be expressed as[5]:

$$i_{2NLgm} = \beta i_{2NLg\pi} = K_{2gm} H_{1vbe}^2 = g_m g_B^2 / (2V_t (g_\pi + g_B)^2) \quad (8)$$

The SFG shows that the nonlinearity of both r_π and g_m is due to a squaring of the controlling 1st order signal $H_{1vbe}(s)$ and a nonlinearity coefficient.

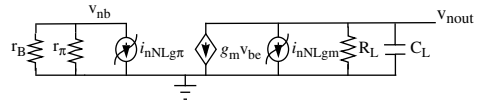

Figure 7. Circuit to be solved for the n^{th} order kernels

To calculate the third-order harmonic distortion component the Volterra kernels are found by solving for node voltages in the linearized network of the third-order system labelled in Figure 4. The total nonlinear current going into the short-circuit node i_{3SCb} is due to the nonlinear current i_B through g_π and can be referred to as $i_{3NLg\pi}$. Similarly, the total nonlinear current going into i_{3SCout} is due to the current i_C of transconductance g_m and referred to as i_{3NLgm}. Since H_{vbe} is independent of frequency, the third-order nonlinear current sources are[5]

$$i_{3NLgm} = \beta i_{3NLg\pi} = K_{3gm} H_{1vbe}^3 + 2K_{2gm} H_{1vbe} H_{2vbe} \quad (9)$$

As (9) illustrates, the third-order nonlinearity results from a component due to the multiplication of three 1st order signals, and a component due to the multiplication of a 1st order signal and a second-order signal. Making use of (4) and (6) we can prove that

$$i_{3NLgm} = \beta i_{3NLg\pi} = \frac{g_m}{6V_t^2}\left(\frac{g_B}{g_B+g_\pi}\right)^3 - \frac{2g_m^2 g_B^3}{4\beta V_t^2 (g_B+g_\pi)^4} \quad (10)$$

HARMONIC DISTORTION ANALYSIS

Having derived the SFG to the third-order, we can now proceed to analyze the second- and third-order harmonic distortion of the amplifier. The harmonic distortion HD_2 is the ratio between the second-order output and the first-order output when $j\omega_2 = j\omega_1$.

$$HD_2 = \frac{A^2}{2}\left|H_{2vout}(jw_1, jw_1)\right| / (A\left|H_{1vout}(jw_1)\right|) \quad (11)$$

where A is the input amplitude. The second-order harmonic output is scaled by 1/2 due to the squaring operation, which can be understood from the trigonometric identity $(A\cos\omega_1 t)^2 = (A^2/2)(1+\cos 2\omega_1 t)$. It also results from applying (1). The kernels H_{2vout} and H_{1vout} are found by directly solving for the node voltages in the SFG of Figure 4. Solving for the kernels directly and assuming that $r_B << r_\pi$ we have

$$HD_2 = A/(4V_t) \times \left|(g_L + jw_1 C_L)/(g_L + 2jw_1 C_L)\right| \quad (12)$$

At low frequencies, HD_2 is independent of the bias point, $HD_2 = A/4V_t$, and at high frequencies, the distortion reduces to $HD_2 = A/8V_t$.

The distortion of common emitter amplifier output was analyzed by performing transient simulations for the circuit and taking the fast Fourier transform (FFT) of the output waveform. Figure 8 compares the second-order harmonic distortion obtained from (12) with that obtained from the transient analysis, which was repeated at different frequencies for an input amplitude of 10mV. We notice that the SFG obtained HD_2 is very close to the actual HD_2. The transistor models used for simulation neglects the internal base, emitter, and collector resistors. To account for their effects they must be added in the SFG analysis, this was avoided in this work to simplify the SFG.

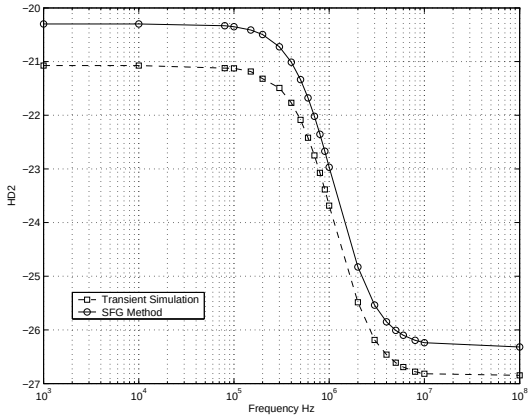

Figure 8. HD_2 for the CE amplifier vs. frequency

HD_3 is the ratio between the third-order output and the first-order output when $j\omega_3 = j\omega_2 = j\omega_1$.

$$HD_3 = (1/4)A^3\left|H_{3vout}(j\omega_1, j\omega_1, j\omega_1)\right| / (A\left|H_{1vout}(j\omega_1)\right|) \quad (13)$$

From the SFG in Figure 4, it can be shown that:

$$H_{3vout}(s_1, s_2, s_3) = \frac{-g_m g_B^4 (g_B - 2g_\pi)}{[6V_t^2 (g_B+g_\pi)^5 (g_L + (s_1+s_2+s_3)C_L)]} \quad (14)$$

If we assume $r_B << r_\pi$, the HD_3 expression becomes

$$HD_3 = \left|-(A^2/(24V_t^2))(g_L + jw_1C_L)/(g_L + 3jw_1C_L)\right| \quad (15)$$

Again, we see that at low frequencies, HD_3 is independent of bias point, $HD_3 = A/24V_t$, and at high frequencies, the distortion reduces to $HD_3 = A/72V_t$. In general, the third-order harmonic distortion is a function of frequency given by (15). Figure 9 compares the third-order harmonic distortion obtained from (15) with that obtained from the transient analysis, which was repeated at different frequencies for an input amplitude of 10mV. We notice that the SFG obtained HD_3 is close to the actual HD_3. Thus the SFG of Figure 4 illustrates how nonlinear signal components are introduced into the system and how they propagate.

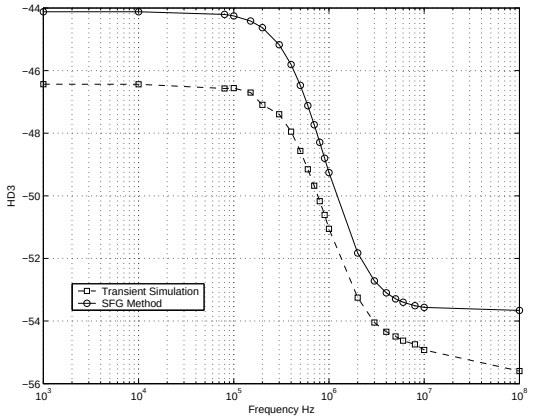

Figure 9. HD_3 for the CE amplifier vs. frequency

COMPARING DISTORTION OF DIFFERENT CIRCUITS

We now present a method for comparing the distortion of different circuit topologies using SFG. When a circuit is represented as a SFG, the SFG can be readily manipulated and simplified so that distinctly different circuit topologies share the same SFG topology. This provides a direct method for comparing circuits. For example, a buffer can be realized using a simple emitter follower (EF) or by feeding back the output of a differential pair to the negative terminal (DP), Figure 10.

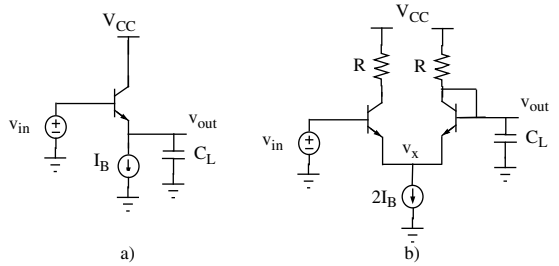

Figure 10. Two buffer circuits: a) Emitter follower b) Differential pair with the unity feedback

Both circuits have the same function but differ in many characteristics such as the level shift that takes place in the emitter follower, the accuracy of the gain offered by the circuit (ideally unity), the distortion offered by each circuit, and the bandwidth. The differential pair is biased using twice the current as the emitter follower to ensure the same DC point for all transistors. Consequently, all transistors have the same power series coefficients. The low frequency combined SFGs of both circuits can be obtained as explained previously, and are shown here in Figure 11 and Figure 12, which show only to the second-order to illustrate the method, but it can be extended to any order.

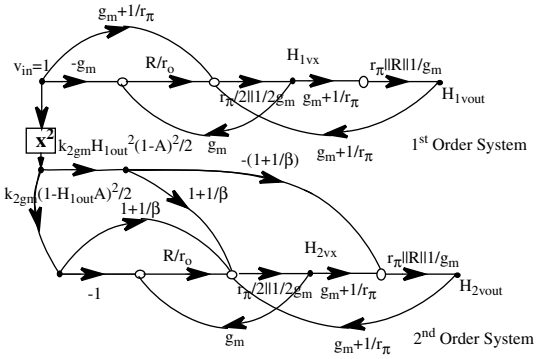

Figure 11. Combined SFG for solving the kernels of the DP

Here the SFGs are simplified by using the fact that $v_{1o} = H_{1vout}v_{in}$, where H_{1vout} is the low frequency gain of the linearized buffer circuit. For the EF it can be expressed as:

$$H'_{1vout} = \left(g_m + \frac{1}{r_\pi}\right)/\left(g_m + \frac{1}{r_\pi} + \frac{1}{r_o}\right) \quad (16)$$

While the gain of the DP with unity feedback can be expressed as:

$$H_{1vout} = \frac{\left(g_m + \frac{1}{r_\pi}\right)\left(g_m + \frac{1}{r_\pi} - \frac{g_m R}{r_o}\right)}{2\left(g_m + \frac{1}{r_\pi}\right)\left(g_m + \frac{1}{r_{\pi'}} + \frac{1}{R}\right) - \left(g_m + \frac{1}{r_\pi}\right)^2 - \frac{g_m R}{r_o}\left(g_m + \frac{1}{r_{\pi'}} + \frac{1}{R}\right)} \quad (17)$$

The relation between the kernel H_{1vx} of the differential pair and the output kernel can be expressed as:

$$A = \frac{H_{1vx}}{H_{1vout}} = \left(g_m + \frac{1}{r_\pi} + \frac{1}{R}\right)/\left(g_m + \frac{1}{r_\pi}\right) \quad (18)$$

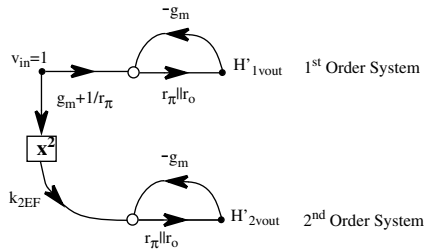

Figure 12. Combined SFG for solving the kernels of the EF

The SFG of the DP with feedback can now be reduced using SFG rules to make the comparison between both circuits possible; all inputs are referred back to a single input node, and the overlapping loops are separated (Appendix). The reduced SFG for the DP is shown in Figure 13. The purpose of the SFG manipulation is to represent both SFGs in a way to allow a direct comparison. We see that both circuits have essentially the same SFG but with different transmittances to the second-order system, where

$$k_{2DP} = \left(k_{2gm}\left(H_{1vout}^2(1-A)^2 - (1-H_{1vout}A)^2\right)\right)/2 \quad (19)$$

and,

$$k_{2EF} = k_{2gm}(1-H'_{1vout})^2/2 \quad (20)$$

This implies that the ratio of the second-order distortion generated by both circuits is directly related to the ratio of the coefficients on the input branches in the SFGs of Figure 12 and Figure 13.

$$\frac{HD_2^{DP}}{HD_2^{EF}} \approx \left|\frac{k_{2DP}/H_{1vout}}{k_{2EF}/H'_{1vout}}\right| = \left|\frac{k_{2gm}\left[H_{1vout}^2(1-A)^2 - (1-H_{1vout}A)^2\right]/H_{1vout}}{k_{2gm}(1-H'_{1vout})^2/H'_{1vout}}\right| \quad (21)$$

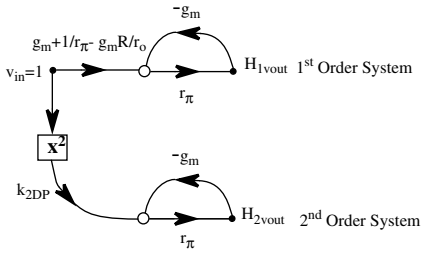

Figure 13. Combined SFG of the DP after reduction

For a bias current of 100μA, β=84, and R=15KΩ, the gain of the DP was H_{1vout}=0.93, and the ratio A=1.034, while the gain of the EF was H'_{1vout}=0.9989. Using these values this ratio is 52.4 dB. This is confirmed by the simulation results in Figure 14. Since the EF was biased with a high impedance current source and wasn't connected to a resistive load, the emitter current and hence the base-emitter voltage is fixed, this explains why the EF offered low distortion. On the other hand in the DP, the sum of the emitter currents of both transistors is fixed but as the input voltage varies the current distribution slightly changes. The input stage can be viewed as an EF loaded with two resistors in series ($1/g_m$+R), then the output voltage is taken across R. This explain why the gain of the DP in this case is less than the EF. Consequently, the base-emitter voltage of the DP transistors varies more than in the EF case giving rise to more distortion. The same analysis can be carried out to compare the third-order distortion. In which the SFG will remain the same, and the only change will be the injected third-order nonlinear currents.

CONCLUSION

In this paper, we demonstrated how signal flow graphs can be applied to weakly nonlinear circuits and used to analyze distortion. Representing the distortion components of different orders on the same graph illustrates how nonlinearities are generated in the system and how various parameters affect the response. The SFG method provides a powerful tool in comparing the performance of different circuits from the distortion point of view. It also helps in the interpretation of distortion results obtained from simulations.

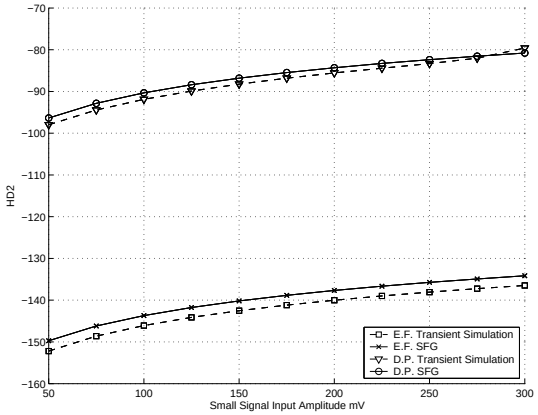

Figure 14. HD_2 for both circuits at low frequencies vs. input signal amplitude

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APPENDIX

This appendix Shows the steps for reducing the SFG of the differential pair with unity feedback.