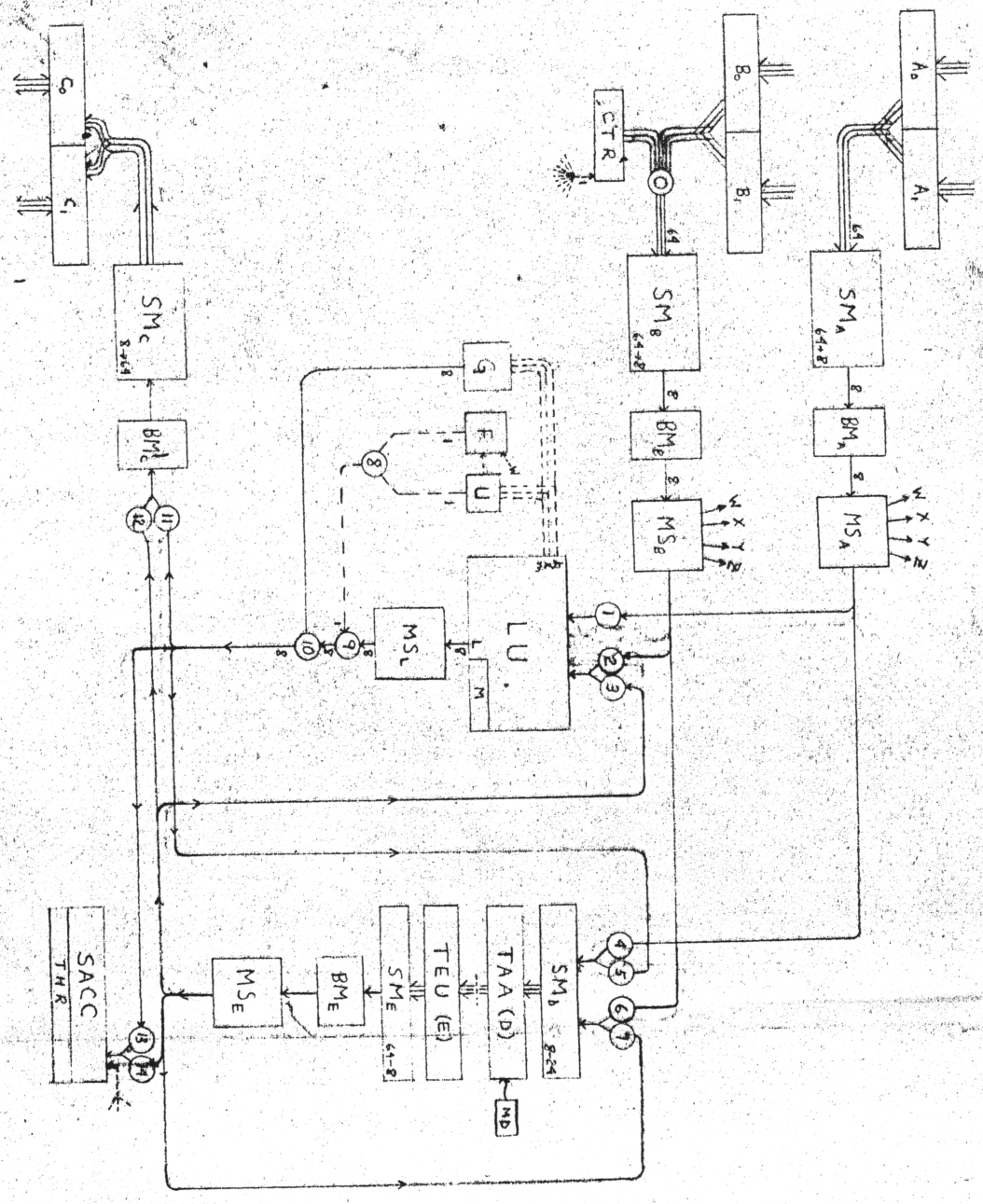


STREAM DATA PATHS



Data Gating:

A gate set at 1 allows data to pass
 A gate set at 0 prevents data from passing

The following modifications apply:

Gate 0: 0 - B → SM_B
 1 - CTR → SM_B

Gates 2, 3: If both are set at 1, only data from B enters LU.

Gates 4, 5: The cutoff of LD is of A. If both 4 and 5 are set at 1, data from A alone enters.

Gates 6, 7: If 6 is set, the cutoff of LD is of B. If 7 is set (whatever 6 may be) one byte comes from 6 and all the rest from 7, the cutoff of LD is then of E.

Gate 8: 0 - H
 1 - F

Gate 9: 0 - L
 1 - U or F from gate 8 in leftmost position with 7 zeroes on right.

Gate 10: 0 - Output from gate 9 (every byte)
 1 - G (end of group only)

Gates 11, 12: If both are set, the data from L enters.

Gates 13, 14: If both are set, the data from E enters.

Roberts - 6 Sept 57

STREAM SETUP WORDS (1)

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63

BASIC INDICATOR REG. ②

BASIC INDICATOR MASK ③

STREAM INDICATOR REGISTER ①

STREAM INDICATOR REGISTER	31	STREAM INDICATOR MASK	31	FF
---------------------------	----	-----------------------	----	----

The 31 Stream Indicator Bits are as follows:

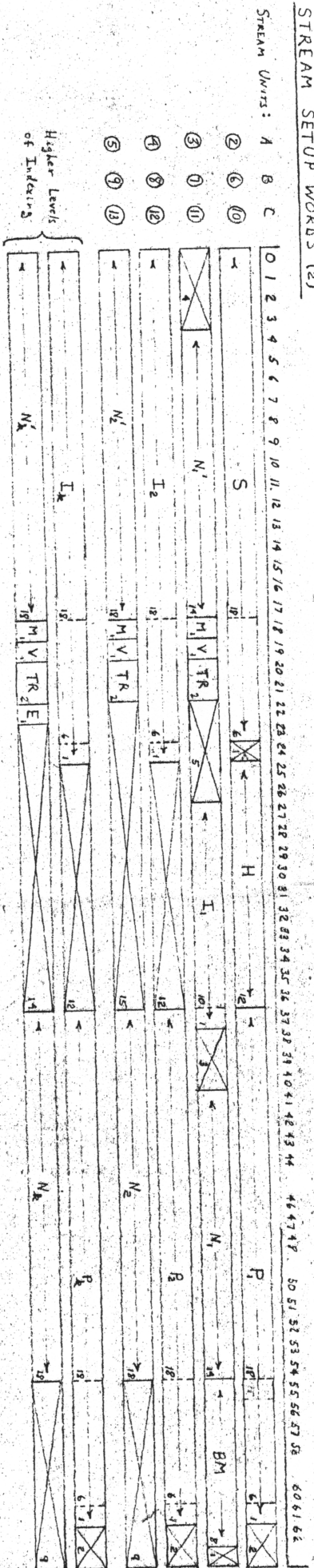
- 0 (Not yet assigned)
- 1 Internal Malfunction
- 2 Invalid Instruction or Address
- 3 Expected Time Clock
- 4 CTR overflow
- 5 SACC overflow or overflow
- 6 SACC sign change to minus
- 7 SACC sign or exceeds threshold
- 8 W
- 9 X
- 10 Y
- 11 Z
- 12 U=0
- 13 U=1
- 14 F=0
- 15 F=1
- 16 G=1
- 17 G=2
- 18 G=3
- 19 G₁A
- 20 G₂B
- 21 G₁C
- 22 G₂A
- 23 G₂B
- 24 G₂C
- 25 G₁A
- 26 G₁B
- 27 G₁C
- 28 Other Computer
- 29 Exchange
- 30 Instruction Tag

Bits 12 - 27 and Bit 30 go on and off. All other bits stay on until they produce arithmetic error (they can then turn off) or until they are sampled (they may then be set on or off).
 FF 62 is 0 in Arithmetic Mode. 1 in Streaming Mode.
 FF 68 can be set by Stream Branch instructions as well as ordinary read into this word.

During the Arithmetic Mode interruptions occur only thru the Basic Indicator Register. During Streaming arithmetic interruptions occur only thru the Streaming Indicator Register. The instructions automatically arising in the latter case are themselves in Streaming Mode. They may fix the difficulty by themselves or branch out into Arithmetic Mode. Then, if the branch was caused by a condition which was joined with several others each one Stream Indicator Bit the Basic Interrupt system would take over. If the condition was represented by a single bit in both registers the bit in the Basic Register would be turned off simultaneously and no Basic Interruption would occur. If the Arithmetic Mode is entered, one must reenter Streaming by specific instruction. This imposes a demand on hardware interrupt response to determine if the machine was in the Streaming Mode when broken occurred and to return to that mode as appropriate. FF 63 can be conveniently used for reentering the mode.

The Arithmetic Mode will contain a "BRANCH TO Y AND ENTER STREAMING" instruction. Each Stream Instruction has a particular bit which when set to 1 will send operations into the Arithmetic Mode at the conclusion of the Streaming process.

STREAM SETUP WORDS (2)



S = Effective Address (24 bits)

H = Address of Higher Levels. The initial value of H indicates where the first word of the 3rd level may be found. All higher level indexing words are stored sequentially. The initial H₁ is stored in a buffer register. If H is interrupted at any time during stream - H₀ will be found thru if notification is currently at the 1st or 2nd levels. If a higher level is being used H will contain the address of the stream index word for that level. (The indexing cycle will be arranged so it cannot be broken between the acquisition of the 1st words of a higher level.)

I = Increment (±10 bits on L₁; ±24 bits on others)

P = Partial Accumulated Increment (±24 bits)

N₁ = Current Count (14 bits on L₁; 18 bits on others)

N = Limit Count (14 bits on L₁; 18 bits on others)

M = Mode Bit

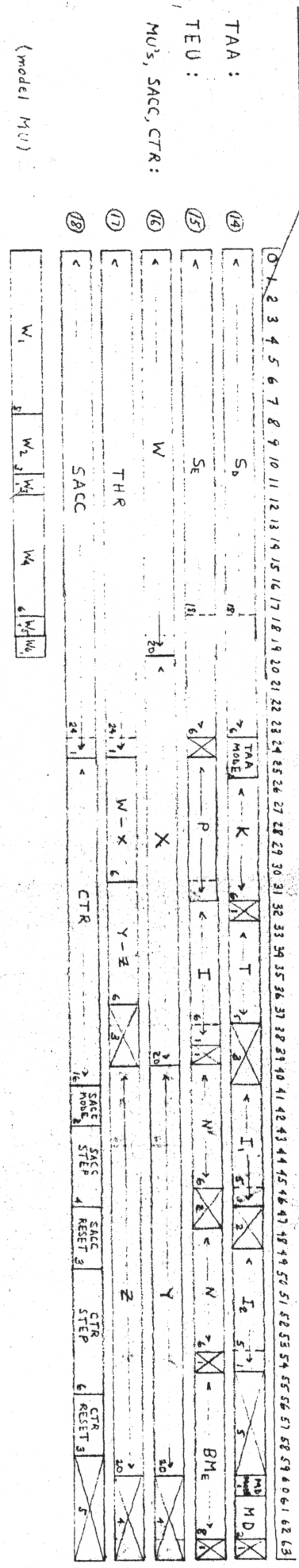
V = Highest Level Bit

TR = Triangular Indexing Bit

E = End-of-Higher Level Indication Bit (Only present in Levels 3 and higher)

Consult Stream Unit Indexing Flow Chart

SIREAM SEIUR WUKD3 (3)



S_0 = Base Address for TAA

TAA MODE: 00 - No Memory Reference
01 - Count (or 0r)
10 - Extract
11 - Extract and Count (or 0r)

K = Count Displacement (Ordered to final assigned address)
(No meaning in model 80A1D) after no effect is replace

[Sequence of operations on TAA: \square Bits from source 1 added to S_0 ; \square Bits from source 2 added to result of \square ; \square MD shift, if any]
 \square Count displacement Ordered to result.

T = Start point within TAA for address assembly
 I_1 = First source increment } The length of word is controlled by I_1, I_2, I_3, I_4
 I_2 = Second source increment } and I_3, I_4 . See GAE Specifications.

MD Mode: 0 - Ineffective
1 - Effective

MD = Current phase of Memory Distributor

S_E = Current Address in TEU (Setup value has no effect)

I = Increment P = Partial Accumulated Increment

N' = Current Count

N = Final Count (N=0 defined as N=64; attempted carry in W then defines equality)

Extraction continues until WEN or the word portion of the current address is about to change. No extraction across word boundaries. Any overflowing bits are made 0.

BME = Bits Mask on E

W, X, Y, Z are H4 four Match Units

W₁ - Match Character

W₂ - Connection: 000 - No connection

- 001 - M5A
- 010 - M5B
- 011 - M5L
- 100 - M5F
- 101 - No connection
- 110 - No connection
- 111 - No connection

W₃ - Scan: 0 - All 8 bits
1 - Rightmost bit only

W₄ - Adjustment function (See Table)

W₅ - Swallow: 0 - Normal Operation
1 - Swallow matched bits

W₆ - Indicator Sense: 0 - Indication on Match
1 - Indication on No-Match

W-X: Adjustment that occurs when

Word X both match simultaneously. This function replacing the sum of the individual functions.

Y-Z: As above, but for Y and Z.

CONTINUED

BA Adminite-9 Sept 57

STREAM SETUP WORDS (4)

THR - Threshold for SACC. Indication if SACC equals or exceeds THR.

SACC - Current Value of SACC. An initial value may be entered. However the automatic reset makes SACC 0.

CTR - Current value of CTR. An initial value may be entered. However the automatic reset makes CTR 0.

SACC Mode: Bit 41: 0 - Entries all positive (Byte entry positions 16-23)
 1 - Entries positive and negative (Byte entry positions 16-23, 24-31)

Bit 42: 0 - Normal Accumulation
 1 - Negative Total set to 0 (The indicator bit recording a change in SACC sign from + to - will still go on when bit 42 is 1 when the bit would have been negative before the reset.)

SACC Step: A one is entered into Bit 21 at the following conditions. This is in addition to any bits that may also be entered.

- 0 - No entry
- 1 - \bar{A}
- 2 - \bar{A}
- 3 - \bar{A}, B
- 4 - \bar{A}, B
- 5 - Byte into C
- 6 - \bar{A}, C
- 7 - \bar{A}, B
- 8 - $F=1$
- 9 - $G=1$
- 10 - $G=2$
- 11 - $G=3$
- 12 - Match in W
- 13 - Match in X
- 14 - Match in Y
- 15 - Match in Z

SACC Reset: SACC is set to 0 at the following conditions:

- 0 - No reset
- 1 - \bar{A}
- 2 - \bar{A}, B
- 3 - \bar{A}, B
- 4 - \bar{A}, B
- 5 - \bar{A}, C
- 6 - Match in W
- 7 - SACC matches THR

CTR Reset: A one is entered into Bit 40 at the following conditions. (Not some specify two conditions)

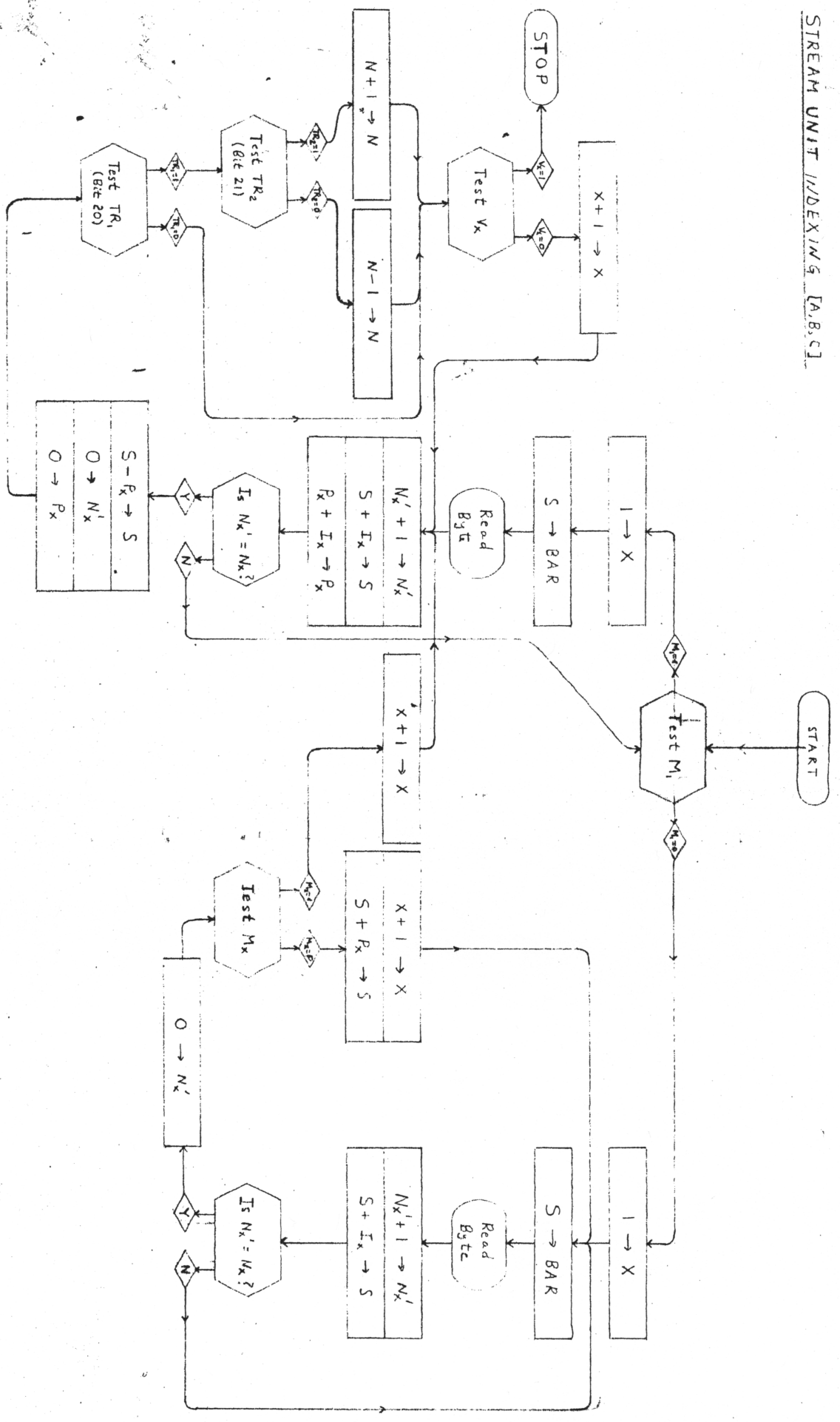
- 0 - No count
- 1 - Byte from A
- 2 - \bar{A}
- 3 - \bar{A}, A
- 4 - \bar{A}, A
- 5 - Byte from B
- 6 - \bar{A}, B
- 7 - \bar{A}, B
- 8 - \bar{A}, B
- 9 - Byte into C
- 10 - \bar{A}, C
- 11 - \bar{A}, C
- 12 - \bar{A}, C
- 13 - Operator in U
- 14 - Address forward-dispatched
- 15 - Byte into C
- 16 - two bit into SACC } three = option 15 of
- 17 - byte into SACC } SACC mode bit 91 = 0
- 18 - SACC > THR: (once for entry, second passing)
- 19 - SACC becomes negative (on unapproved negativity)
- 20 - Match in W
- 21 - Match in X
- 22 - Match in Y
- 23 - Match in Z
- 24 - Non-match in W
- 25 - Non-match in X
- 26 - Non-match in Y
- 27 - Non-match in Z
- 28 - Match in both W and X (only one count)
- 29 - Match in both Y and Z (only one count)
- 30 - Non-match in both W and X (only one count)
- 31 - Non-match in both Y and Z (only one count)
- 32 - No matches in W, X, Y, Z (only one count)
- 33 - $A=0$
- 34 - $A=1$
- 35 - $A=0$
- 36 - $A=1$
- 37 - $m=0$
- 38 - $m=1$
- 39 - $v=0$
- 40 - $v=1$
- 41 - $F=0$
- 42 - $F=1$
- 43 - $G=1$
- 44 - $G=2$
- 45 - $G=3$
- 46 - $G=1$
- 47 - $G=2$
- 48 - $G=3$ (end of group)
- 49 - $F=0 \& v=0$
- 50 - $F=0 \& v=1$
- 51 - $F=1 \& v=0$
- 52 - $F=1 \& v=1$
- 53 - $F=0 \& v=0$
- 54 - $F=0 \& v=1$
- 55 - $F=1 \& v=0$
- 56 - $F=1 \& v=1$
- 57 - $F=0 \& v=0$
- 58 - $F=0 \& v=1$
- 59 - $F=1 \& v=0$
- 60 - $F=1 \& v=1$
- 61 -
- 62 -
- 63 -

CTR Reset: CTR is set to 0 at the following conditions:

- 0 - No reset
- 1 - Match in W
- 2 - Match in X
- 3 - Match in Y
- 4 - Match in Z
- 5 - \bar{A}, C
- 6 - SACC reset
- 7 - SACC becomes negative

DA 8/14/44 - 9-504 57

STREAM UNIT INDEXING [A,B,C]



Adkins - 9 Sept 57

STREAM OPERATIONS

#	L	R = 1 if	L = 1 if	M = 1 if
0-15	Logical Connections	0-15	Connection set all 0 or all 1	Connection all 1
16-31	Logical Connections	0-15	Connection even parity but not all 0	Connection odd parity
32	—	A > B	A = B	A < B
33	Max (A, B)	"	"	"
34	Max (A, B) if ≠ 0, otherwise —	"	"	"
35	Min (A, B)	"	"	"
36	Min (A, B) if ≠ 0, otherwise —	"	"	"
37	A if A = B, otherwise 0	"	"	"
38	A if A = B, otherwise —	"	"	"
39	A if A = B ≠ 0, otherwise —	"	"	"
40	A if A ≠ B, otherwise 0	"	"	"
41	A if A ≠ B, otherwise —	"	"	"
42	A - B if A ≥ B, otherwise 0	"	"	"
43	A - B if A ≥ B, otherwise —	"	"	"
44	A - B if A > B, otherwise —	"	"	"
45	B - A if B > A, otherwise 0	"	"	"
46	B - A if B > A, otherwise —	"	"	"
47	B - A if B > A, otherwise —	"	"	"
48	A + B mod M	A + B > M	A + B = M	A + B < M
49	A + B mod M if ≠ 0, otherwise —	A + B > M	A + B = M	A + B < M
50	A - B mod M	A > B	A = B	A < B
51	G - A mod M	A > B	A = B	A < B

- 52 INDIRECT LOAD AND STORE
- 53 STORE AND CLEAR SAIC-CTR
- 54 BRANCH
- 55 CONDITIONAL BRANCH
- 56 INCREMENT AND BRANCH
- 57 CONDITIONAL ADJUST
- 58 CLEAR MEMORY
- 59 MOVE
- 60 COLLECT

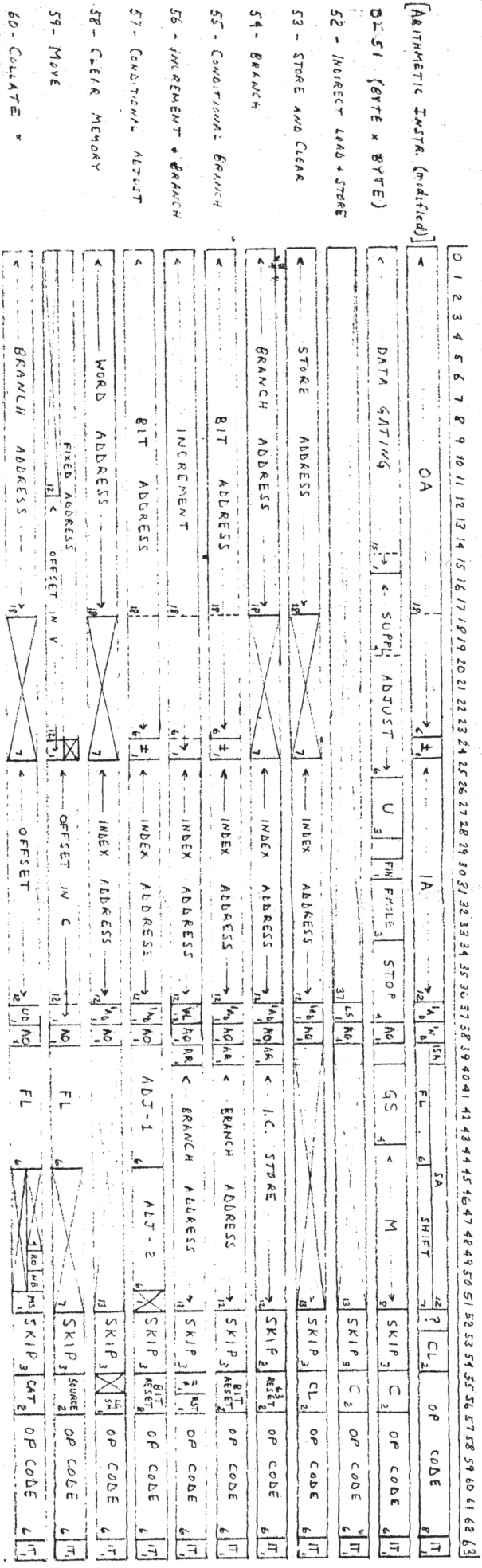
The Data Coding, [L,R,M] formalism, and other bit-by-bit specifications do not apply for these instructions. See format and explanations.

The 16 Logical Connections (A and B here and in the table at the left refer to the data entering LV thru gates 1, and 2 or 3, respectively.)

Connective	AB = 11	10	01	00
0 (0)	0	0	0	0
1 ($\bar{A} \cdot \bar{B}$)	0	0	0	1
2 ($\bar{A} \cdot B$)	0	0	1	0
3 ($A \cdot \bar{B}$)	0	0	1	1
4 ($A \cdot B$)	0	1	0	0
5 (\bar{B})	0	1	0	1
6 ($A \vee \bar{B}$)	0	1	1	0
7 ($\bar{A} \vee \bar{B}$)	0	1	1	1
8 ($A \cdot B$)	1	0	0	0
9 ($A \equiv B$)	1	0	0	1
10 (B)	1	0	1	0
11 ($\bar{A} \vee B$)	1	0	1	1
12 (A)	1	1	0	0
13 ($A \vee \bar{B}$)	1	1	0	1
14 ($A \vee B$)	1	1	1	0
15 (1)	1	1	1	1

Radl-H-9 Sept 57

STREAM INSTRUCTION FORMATS (1)



- 61 -
- 62 -
- 63 -

The Byte x Byte Format (0-51)

- a) Data Gating (See Data Path Diagram)
- O: B A CTR → 548
 - 1: A → LU
 - 2: B → LU
 - 3: E → LU
 - 4: A → TAA
 - 5: LU → TAA
 - 6: B → TAA
 - 7: TEU → TAA
 - 8: U → F 4 9
 - 9: L → 8 4 10
 - 10: 9 → 9
 - 11: LU → C
 - 12: TEU → C
 - 13: LU → SAC
 - 14: TEU → SAC
 - 15: (space)

- b) Supplementary Adjustment: 4-Stimulus - as below
- O: none
 - 1: U=1
 - 2: F=0
 - 3: F=1
 - 4: G=1 } attend if
 - 5: G=2 } group
 - 6: G=3 }
 - 7: Match in W
 - 8: Match in X
 - 9: Match in Y
 - 10: Match in Z
 - 11: End of Group
 - 12: STOP
 - 13: SA
 - 14: SA
 - 15: SA

- c) U: The 3 bits correspond to A, B, C. The signals corresponding to 15 in this field are mixed together to form the one-bit output of LU.

- d) F input: 0-U, 1-W
- e) F mode
- 0 Stay on 1 after bit 1
 - 1 Flip-Flop on 1
 - 2 1 if last bit was 0, correct 0
 - 3 1 " " " " 0
 - 4 1 " " " " 0
 - 5 1 " " " " 1
 - 6 either 2 or 5
 - 7 either 3 or 4
- f) STOP: 2-Level, 2-Unit
- 0 0 A
 - 1 0 B
 - 2 0 C
 - 3 0 E
- g) Arithmetic operation
- 0 Next instruction is Stream Mode
 - 1 Next instruction is hold mode
- h) Group Size - Same code as STOP
- 1) Skip
 - 000 +4
 - 001 +1
 - 010 +2
 - 011 +3
- i) C action
- 0 VFL Storage
 - 1 Error/Slide Storage
 - 0 C stand upon STOP
 - 1 C stand upon STOP

SA Address - 10 Sept 57

STREAM INSTRUCTION FORMATS (2)

Indirect Load and Store (52)

IS: 0 - Load : L1B → TAA, MEM → A address, A → C
 1 - Store : L1B → TAA, MEM → C address, A → C

TAA mode 0, 1: no memory ref, TAA → address
 2, 3: last 24 bits of TEU → address
 (counting or saving in 3)

AO, SKIP, C as in 1

Store and Clear (53)

Bits 0-40 of Setup word 18 stored in bits 0-40 of indirect store address. Bits 41-63 of latter mode 0.

INB with basis. CL: 00 Working cleared
 01 CR cleared
 10 SMC cleared
 11 CR and SMC cleared

Branch (54)

Unconditional Branch to indirect Branch Address, if AR=0
 Branch to (LS + indirect Branch Address) + AR=1

63 bits address bits of Store Interrupt Register
 0 - Leave unchanged
 1 - Invert
 2 - Set to 0
 3 - Set to 1

Old 1. word

SKIP effect is only if indirect branch address is 0.

Conditional Branch (55)

Test any (indirect) bit in new reg. Branch to pos. or neg. bit sign as here.

AR = absolute or relative as in (54). Bit reset as in reset side in (54).

Reset V if Bit 56=1.

Increment and Branch (56)

The given increment is added to the Value: VL=0 in the index word. Branch if VL=1. Bit 55=0. Absolute or relative branch.

Value: VL=0
 Length: VL=1

Conditional Adjust (57)

Test and reset any bit in (55). Adjust if parity error. 2 general purpose registers. If bit is no op, skip second.

Clear Branch (58)

Indirect WA may be any WA in class m by (branch). Bit 56=0 = Long Branch
 1 = Small Branch

All words in the sequence of indirected addresses are cleared. Bit 56 refers to one memory unit.

Move (59)

Source: 0: Fixed
 1: A
 2: B
 3: E

Begin fixed at fixed address or at spec field reset in A, B, E. Begin with word at specified offset.

S is reset in A, B, E but not in C.

Rotate (60)

MS: 0 - Merge
 1 - Search

Case: 0 Shift [offset for search]
 1 offset
 2 split
 3 split branch

UD: 0 Ascending order
 1 Descending order

RO: 0 No round of L2
 1 Auto round of L2

NB: 0 Skip end of this block (3rd level)
 1 go on to next block

Merge only. Search basically uses regular stream indexing.

Address 10 - 10 Sept 57

ADJUSTMENT FUNCTIONS

No. OP	FUNCTIONS 0-49	50-51	52-53	54-55	56-57	58-59	60-61	62-63
0	No. op (for singles); Sum of actions (for MUs)							
1	Go to next instruction							
2	" " " " " " " "							
3	" " " " " " " "							
4	" " " " " " " "							
5	Start C and go to next instruction							
6	Reset L1A							
7	Advance L1A							
8	Runout L1A							
9	Reset L2A							
10	Advance L2A							
11	Runout L2A							
12	Reset L3A							
13	Advance L3A							
14	Runout L3A							
15	Reset L1B							
16	Advance L1B							
17	Runout L1B							
18	Reset L2B							
19	Advance L2B							
20	Runout L2B							
21	Reset L3B							
22	Advance L3B							
23	Runout L3B							
24	Reset L1C							
25	Advance L1C							
26	Reset L2C							
27	Advance L2C							
28	Reset L3C							
29	Advance L3C							
30	Reset T7A (Correct Address)							
31	Reset L1E							
32	Advance L1E							
33	Runout L1E							
34	Reset L2E (Start Ref eq'n)							
35	Advance L2E (Get next ref immediately)							
36	Stop next reference							
37	Cancel L							
38	Insert A in place of L							
39	Insert B in place of L							
40	Insert E in place of L							
41	Insert M in place of L (M=E)							
42	Disable W for next byte							
43	Disable X for next byte							
44	Disable Y for next byte							
45	Disable Z for next byte							
46	Stop SACK (to 2)							
47	Reset SACK							
48	Stop CTR							
49	Reset CTR							

G

is a special memory device to infer and record the status of groups from analysis of the bytes within the groups. It has 4 states: 0 = waiting; 1 = the group statement equivalent to A; 2 = L; 3 = M. It is fed directly by A, E, M. Then on the different transition references depending upon the byte function involved:

1. Stream Logic Zero (0-15)

k=1	k=1	m=1
0	1	2
1	1	2
2	2	2
3	2	2

2. Stream Logic Priority (16-31)

k=1	k=1	m=1
0	1	2
1	1	2
2	2	2
3	3	3

3. Stream Select (32-47) and Mod Subtract (50-51)

k=1	k=1	m=1
0	1	2
1	1	1
2	1	2
3	3	3

4. Supplies an 8-bit byte. While waiting, it is all 0. Otherwise:

Code	State	Bit	Value
0	01-1	2	100
1	10-2	3	110
	11-3	4	010
		5	011
		6	001
		7	101

Selection is made by 8M and/or address.

12-14-57-10 Sept 57