Quadrature Bandpass $\Delta \Sigma$ Modulation for Digital Radio

Stephen A. Jantzi, Member, IEEE, Kenneth W. Martin, Fellow, IEEE, and Adel S. Sedra, Fellow, IEEE

Abstract—A quadrature bandpass $\Delta \Sigma$ modulator IC facilitates monolithic digital-radio-receiver design by allowing straightforward “complex A/D conversion” of an image-reject mixer’s $I$ and $Q$ outputs. Quadrature bandpass $\Delta \Sigma$ modulators provide superior performance over pairs of real bandpass $\Delta \Sigma$ modulators in the conversion of complex input signals, using complex filtering embedded in $\Delta \Sigma$ loops to efficiently realize asymmetric noise-shaped spectra. The fourth-order prototype IC, clocked at 10 MHz, converts narrowband 3.75-MHz $I$ and $Q$ inputs and attains a dynamic range of 67 dB in 200-kHz (GSM) bandwidth, increasing to 71 and 77 dB in 100- and 30-kHz bandwidths, respectively. Maximum signal-to-noise plus distortion ratio (SNDR) in 200-kHz bandwidth is 62 dB. Power consumption is 130 mW at 5 V. Die size in a 0.8-$\mu$m CMOS process is $2.4 \times 1.8$ mm$^2$.

Index Terms—Analog-digital conversion, CMOS analog integrated circuits, complex filters, digital radio, bandpass sigma-delta modulation, switched-capacitor circuits.

I. INTRODUCTION

CONSIDERABLE research effort pushes toward the realization of fully monolithic, chiefly digital, RF transceivers—with the ultimate objective being the implementation of small, inexpensive, low-power communication devices that are robust, testable, and capable of handling multiple communications standards. Two-path zero-IF architectures and single-path bandpass-$\Delta \Sigma$-based architectures strive to attain these dual goals, but neither effectively achieves both.

Low-IF receiver architectures have recently been proposed, which, with modern quadrature image-reject mixers and strategic IF placement, offer a viable solution for digital, monolithic receivers. A critical component of such a system—and indeed of any receiver that uses image-reject mixing to alleviate passive filtering requirements—is one that efficiently performs bandpass A/D conversion on quadrature signals. This paper describes such an IC, which is a quadrature variant of a bandpass delta–sigma ($\Delta \Sigma$) modulator.

II. TRADITIONAL RECEIVER ARCHITECTURES

A. Bandpass Delta–Sigma Modulation for IF Digitization

In a bandpass $\Delta \Sigma$ modulator [1], [2], bandpass filtering and feedback around a low-resolution quantizer (Fig. 1) shape the noise spectrum, facilitating accurate A/D conversion on narrow-band input signals. Bandpass $\Delta \Sigma$ modulators operate in much the same manner as conventional (low-pass) modulators and retain many of their advantages over conventional Nyquist-rate converters. These advantages include inherent linearity, reduced anti-alias filter complexity, and robust analog implementation [3].

Architectures similar to that shown in Fig. 2 have recently become popular, using bandpass $\Delta \Sigma$ modulation to perform accurate, narrow-band, A/D conversion at the IF [4], [5]. Compared with fully analog receiver implementations, the signal processing and narrowband channel-selectivity filtering are moved into the digital domain where testing is systematic and changing filter coefficients is trivial. Elimination of analog IF filters is also an important advantage when dealing with digital modulation schemes like those emerging for cellular telephones, because analog IF filters generally have poor (and poorly controlled) phase performance—and, hence, induce inter-symbol interference—whereas digital filters can have exactly linear, and well-controlled, phase.

In comparison with typical Nyquist-rate converters, bandpass $\Delta \Sigma$ converters gain an advantage in that they behave much more like analog circuits, having intermodulation-product levels that fall for reduced input levels\(^1\) (for example, the third-order IM products fall at a 3 dB per 1 dB rate) [1]. Their behavior in radio systems is, therefore, relatively easy to predict, while video converters can be expected to produce undesirable spurious effects [3].

A final beneficial characteristic of this receiver configuration is that such use of a bandpass $\Delta \Sigma$ modulator allows in-phase/quadrature ($I/Q$) decomposition to be performed in the digital world with arbitrary precision and perfect $I/Q$-channel matching [3], [5].

B. Single-Path Mixing

This single-path architecture, however, is not amenable to monolithic (single-chip) implementation. Fig. 3(a) shows the frequency spectrum at the mixer input, where the shaded trian-

\(^1\)In typical Nyquist-rate converters, such as flash converters, for example, distortion products tend to remain at a fixed level regardless of signal strength.
Fig. 2. IF digitization using a bandpass $\Delta\Sigma$ ADC.

Fig. 3. Downconversion in a single-path IF receiver: (a) mixer input spectra and (b) mixer output spectrum.

Fig. 4. Downconversion in a two-path system that uses image-reject mixing and zero IF: (a) mixer input spectra and (b) mixer output spectrum.

gular and rectangular shapes represent the desired and image spectra, respectively, at the antenna, and the two impulse functions represent the local oscillator (LO) spectrum, which is that of a cosine.

Whereas trigonometric operations describe the mixing operation in the time domain, frequency-shifting operations do so in the frequency domain. The multiplication-in-time between the LO and antenna signals is equivalent to a convolution-in-frequency of their spectra. Thus, the impulse function at $-f_{LO}$ shifts the antenna spectrum left by $f_{LO}$; that at $+f_{LO}$ shifts the antenna spectrum right by $f_{LO}$ (note the grey arrows). Fig. 3(b) shows the resulting mixing products at low frequencies.\(^2\) The frequency labeled $f_s$ signifies a possible sampling rate for A/D conversion of the mixer output.

Clearly, there is a range of image frequencies which mix down into the same IF band as do the desired signals, thereby corrupting wanted information. The need for the high-$Q$ front-end bandpass filter, centered at $f_0$, is obvious, since the image frequencies must be eliminated prior to the mixing operation and since the desired band and image band are separated by only twice the IF frequency. To meet the requirements, external high-$Q$ passive filters—surface-acoustic-wave (SAW) and ceramic filters, for example [6]—are typically required, consuming power for the purpose of taking signals on and off the chip.

C. Image-Reject Mixing and Direct-Conversion Receivers

An LO which has a pair of phase-quadrature outputs mixes in such a way that it shifts the antenna spectrum in only one direction and, thus, image frequencies will not (in the ideal case) fall into the same IF band as the desired signal. It is a cancellation effect of mixing with both a cosine and sine signal that performs the rejection of the image components. Fig. 4 shows this complex-exponential mixing for the case where the

\(^2\)The high-frequency components are removed by a post-filter and thus are not shown.
Fig. 5. Direct-conversion architecture.

Fig. 6. Downconversion in the low-IF receiver: (a) mixer input spectra and (b) mixer output spectrum.

single impulse function frequency-shifts the antenna spectrum to the left by \( f_{\text{LO}} = f_0 \). The mixer output, which is now obviously a complex signal,\(^3\) has a spectrum that, around dc, contains only the desired signal.

The spectrum shown is that of a direct-conversion receiver (Fig. 5), which uses image-reject mixing and a zero IF to shift the input spectrum directly to a complex baseband signal. This means that the receiver ideally has no image response and, thus, the narrowband, off-chip, image-rejection filter in the RF stage can be replaced with a broadband integrated filter. As such, this architecture is often considered for use in single-chip digital radio receivers [7]–[10].

The choice of zero IF poses considerable problems, however. DC offsets at the output of the two mixers can be much greater in magnitude than the desired baseband signal; ac coupling can be used, but this places a notch in the effective receiver passband which can adversely affect some modulation schemes. The zero-IF approach means that noise and dc offsets cause no problem, self-interference is not an issue (because the oscillator frequency is offset from the carrier frequency), and even-order distortion products have less effect—as is the case in any bandpass system. The resulting spectra appear as in Fig. 6.

B. Front-End Image-Rejection Considerations

In a nonideal front end, the quadrature oscillator signal leaks to positive frequencies, thereby mixing some of the image input into the signal band. This is not catastrophic in the zero-IF topology, since the image signal is equal to the desired signal (see Fig. 4), and a relatively small image rejection (\( \approx 25 \) dB) will suffice for many applications [12]; this level of performance is achievable from standard quadrature image-reject mixers. In the low-IF topology, in contrast, the image signal is not related to the desired signal (note the dissimilar rectangular and triangular spectra in Fig. 6), and can in fact be 20 dB, or more, larger [12], [13]. The nonideal mixing process produces the receiver spectra shown in Fig. 7. Note how some of the rectangular image spectrum has leaked into the desired signal band at \( +f_{\text{IF}} \).

In order to minimize this image interference, the front-end image-rejection requirements for low-IF receivers are typically in the 60–80 dB range [13]. Modern image-reject mixers—and

\(^3\) Complex signals have frequency spectra that are not symmetric about dc.
Fig. 7. Downconversion in a low-IF receiver with a nonideal image-reject mixer: (a) mixer input spectra and (b) mixer output spectrum.

Fig. 8. A low-IF system utilizing a quadrature bandpass $\Delta \Sigma$ modulator.

other promising mixing techniques, such as double quadrature downconversion [12]—approach the necessary performance levels, often exceeding 40-dB image-rejection performance [14], [15] and, recently, even approaching the 60-dB level [16].

Since image-reject mixer performance alone may fall short of some standards' requirements, a receiver's image can be strategically located in order to help alleviate concerns over image interference [13]. In GSM specifications, for example, there are guaranteed "holes" in the receive spectrum for two 200-kHz adjacent channels [17]. Choosing an IF such that images lie in this hole greatly reduces image concerns.

A final consideration for IF placement is the tradeoff between additional front-end image rejection and back-end circuit complexity: if the IF is large enough, a modicum of image rejection can be contributed from an integrated front-end filter, but ultimately, the IF is constrained to a level that allows straightforward A/D conversion to be performed in the receiver back-end.

Thus, combining modern image-rejection mixer techniques with strategic choice of IF points toward low-IF receivers as a viable solution for future monolithic radio receivers [12], [13].

IV. QUADRA TURE BANDPASS $\Delta \Sigma$ MODULATION

Modification of the direct-conversion structure of Fig. 5 to a low-IF variant means that the $I$ and $Q$ mixer outputs become narrow-band signals at an IF (rather than at baseband), and, after anti-alias filtering, they must be converted to digital signals. Thus, an integral component of such a low-IF receiver—and indeed of many systems that use quadrature paths in their signal chains—is a component that can perform A/D conversion on a pair of narrow-band $I$ and $Q$ input signals.

Replacing the low-pass $\Delta \Sigma$ converters in the zero-IF receiver of Fig. 5 with a pair of bandpass $\Delta \Sigma$ converters will suffice but brings a penalty of double modulator order (two low-pass modulators become two bandpass modulators); and double order means double area, power, etc. Furthermore, such a technique proves to be wasteful from a mathematical noise-shaping viewpoint, since half of the bandpass-noise-shaping notches would null noise in the unused band around $-f_{IF}$ (remember, the desired complex signal exists only at $+f_{IF}$) [18].

A. Quadrature-IF Digitization in the Low-IF Receiver

Fig. 8 shows the low-IF receiver modified to utilize complex, or quadrature, versions of both the anti-aliasing filter and the $\Delta \Sigma$ converter. In such a system, the quadrature bandpass

4To achieve the same-degree of in-band noise shaping, a bandpass modulator requires twice the order of a low-pass one. A fourth-order bandpass modulator, for example, has the same second-order noise-shaping as a second-order low-pass modulator.
ΔΣ modulator performs A/D conversion on the I and Q mixer outputs in concert [11], [18]–[22]. Obviously, the front-end could be replaced by similar functional blocks, such as a double quadrature downconverter [12], with the pictured back-end remaining intact—in general, any architecture that uses quadrature channels at some IF in its receive path would benefit from such a back-end combination of a complex anti-alias filter and a quadrature bandpass ΔΣ modulator. These benefits, and the ΔΣ modulator IC design and performance, are discussed below.

B. Quadrature ΔΣ Noise-Shaping

The traditional bandpass ΔΣ modulator of Fig. 1 takes in a real, analog, input and produces a single high-speed bit-stream output that is representative of the input within a narrow bandwidth. This is extended to the quadrature, or complex, case if a complex filter is placed in the ΔΣ loop (Fig. 9). The structure shown is symbolic in the sense that an actual modulator would likely feed both the input and output signals to various points within the loop filter. A quadrature ΔΣ modulator takes in a complex analog input and produces a complex digital output that is representative of the complex input within a narrow bandwidth. The spectrum of the output, being complex, may be asymmetric about dc.

Complex-valued signals are not particularly mysterious; rather, they are simply a convenient representation of pairs of real signals—one signal is interpreted as the real part and the other signal as the imaginary part of the combined complex signal. For example, the complex-exponential sinusoid (complex tone) LO in Fig. 6—which actually has frequency components at only one negative value—is made up of a (real-part) cosine signal and an (imaginary-part) inverted-sine signal, which have equal amplitudes.

Following this train of thought, the quadrature modulator can be thought of as performing a “complex A/D conversion” [23] on the complex analog input—which is just the analog inputs combined as \( I + jQ \). It has two high-speed bit-stream outputs; one represents \( I \), the other, \( Q \). When combined, again as \( I + jQ \), these outputs form a complex digital signal that accurately represents the complex input within a narrow frequency band.

C. Realizing Complex Poles

The block labeled as a complex resonator in Fig. 9 is a switched-capacitor (SC) complex filter—although it could be replaced with an appropriate continuous-time complex filter. A complex filter [24], [25] has a transfer function with complex-valued coefficients and is, thus, not constrained to having complex-conjugate pairs of poles or zeros or to having a symmetrical magnitude response around dc.

A real low-pass ΔΣ modulator contains integrators in its loop filter; a real bandpass ΔΣ modulator contains resonators in its loop filter; so it is understandable that the loop filter of the quadrature bandpass ΔΣ modulator in Fig. 9 comprises several complex integrators. The requisite complex integrators are simple complex filters that each form a complex pole on the unit circle. With feedback applied around the quantizer, these poles form the noise-shaping zeros responsible for nulling in-band quantization noise.

A complex filter with a single pole at real-axis coordinate \( (1 + d) \) and imaginary-axis coordinate \( e \) has the transfer function

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{z - 1 - d - je}.
\]

An efficient realization of this single-pole complex filter is possible since the equation clearly describes the simple feedback network of Fig. 10(a), in which double lines represent complex
signals [26]. This network can be constructed using real blocks in the two-channel system shown in Fig. 10(b). One of the cross-coupling values is negative since the imaginary term of the coefficient is being multiplied by the imaginary channel output—and $j \times j$ is equal to $-1$.

Fig. 10(c) shows that the $1/(1 - e^{-j})$ blocks are simply $(e^{-j})/(1 - e^{-j})$ delaying-type SC integrators, so a complex pole can be created in switched-capacitor technology by way of two cross-coupled integrators. The negative value for one of the capacitors, $C_i$, is easily realizable in a fully differential implementation.

D. A General Fourth-Order Complex $\Delta \Sigma$ Architecture

A fourth-order complex modulator, which contains four complex poles inside a global feedback loop, can be constructed as shown in Fig. 11. For clarity, the structure is shown in its single-ended, rather than the actual, fully differential, form; note its use of four of the complex integrators discussed above and shown in Fig. 10(c). The modulator input has complex feed-ins to each stage through the $C_{i1}$ and $C_{i2}$ capacitors. Each channel has a latched comparator that produces a one-bit output and drives the one-bit feedback DAC’s. The DAC output levels feed back into the modulator stages through the $C_{o1}$ and $C_{o2}$ capacitors.

This structure is actually the extension, to complex form, of a similar structure used in higher-order real $\Delta \Sigma$ modulators [1], [3], which is apparent from its signal-flow diagram pictured in Fig. 12. The structure is a general one—which comes at the penalty of an increased number of coefficients (capacitors) needed in the implementation—that allows independent positioning of all transfer function poles and zeros, which is advantageous since noise-shaping can then be performed at an arbitrary fraction of the sampling frequency and since noise-shaping zeros can be spread optimally across the band of interest. Delay-cell-based bandpass-$\Delta \Sigma$ structures do not have this design freedom, being constrained to having coincident noise-shaping zeros that are fixed at $f_s/4$ [4], [5].

Arbitrary band placement means that a sampling rate can be chosen in order to achieve the desired SNR performance over a specified bandwidth, without regard to center frequency. The latter can then be chosen as is optimal for the application at hand, perhaps to choose a specific IF to alleviate receiver image-rejection concerns, as discussed earlier. Certain restrictions in band location are wise; choosing $\omega_0$ equal to a simple fraction of $\pi$—such as $\pi/2$, $\pi/4$, $3\pi/4$, etc.—makes the first stage of modulator decimation particularly simple, allowing a complex demodulator to be implemented with relatively simple hardware [3], [5].

Optimal positioning of zeros within the band of interest significantly increases the SNR obtainable by a given modulator order [3]. For example, in the case of a modulator with three in-band zeros, optimal placement gives an SNR advantage of 8 dB over a design with coincident zeros [27]. Although general structures like Fig. 12 [1] are marginally more sensitive to capacitor-ratio mismatch than delay-cell-based structures [4], [5], optimal zero placement with a general
structure still provides superior noise-shaping in cases where three or more in-band zeros are present.\footnote{In modulators with only two in-band zeros, optimal zero placement buys only 3.5 dB SNR over a coincident-zero configuration [27]. Since the impact of structure on SNR is less severe, the choice of structure is usually determined by other issues.}

E. The Noise Transfer Function

The structure of Figs. 11 and 12 realizes a complex, fourth-order noise-shaping transfer function (NTF)—the transfer function from the quantization noise “input” to the modulator output. A generalized pole-zero optimizer known as filtorX [28] was used, along with Matlab [29] and closed-form expressions [27], to design the NTF.

The pole-zero placement is optimized for an angular center frequency of $3\pi/4$ and bandwidth of about $\pi/32$. The IC is ultimately tested at $f_s = 10$ MHz, which gives a center-frequency of $f_c = 3.75$ MHZ and an “optimized” bandwidth of $f_b \approx 156$ kHz. These specifications allow use in 200-kHz-bandwidth (GSM) systems—at slightly below the oversampling ratio used in the optimization—and also in lower-bandwidth systems such as CT2+ (100 kHz) or AMPS and IS-54 (30 kHz)—at slightly above it. If a design is required for use in one standard only, the NTF would be optimized for one bandwidth specification and would exceed this NTF’s performance for that specification.

The NTF was designed under the standard constraints of $\Delta \Sigma$ modulator design: maximum in-band attenuation for quantization-noise suppression; small out-of-band gain ($\approx 4$ dB) to help modulator stability; and a first NTF impulse-response coefficient of unity to avoid any delay-free loops containing the quantizer [3].

The resulting pole-zero plot is shown in Fig. 13(a), and the associated full-band magnitude response (i.e., from $-f_s/2$ to $f_s/2$) in Fig. 13(b), which includes an expanded view of the in-band region; note that the poles and zeros have no complex-conjugates and that the magnitude response is not symmetric about dc. Three zeros of the NTF are placed in the in-band region, to suppress quantization noise, while the fourth is placed in the center of the image band, as a technique to help minimize SNR and image-rejection degradation due to component mismatch [18], [30].

One pole is placed near the image-band zero in order to maintain the desired shape of the magnitude response out-of-
band, while the other three poles are placed in a Butterworth configuration around the in-band region.

F. The Signal Transfer Function

The signal transfer function (STF)—the transfer function from the modulator input to the modulator output—shares poles with the NTF in the structure shown in Figs. 11 and 12, which saves on hardware. The four complex inputs to the structure allow three STF zeros to be placed.

The STF pole-zero plot is shown in Fig. 14(a) and its magnitude response in Fig. 14(b). It has an in-band gain of 20 dB and out-of-band rejection of 30 dB (relative to the in-band gain). One STF zero is placed over the image-band pole to null its response, leaving two zeros available to effect shaping of the input spectrum. In this case, a complex bandpass filtering function is achieved by placing a zero at $\omega_0 = 2.5$ MHz and another at $\omega_0 = -1$ MHz.

G. SNR Superiority of a Quadrature $\Delta\Sigma$ Modulator Versus a Real-Bandpass $\Delta\Sigma$-Modulator Pair

The ability to place noise-shaping zeros in a complex configuration, and thereby perform asymmetric noise shaping, proves highly beneficial in the $\Delta\Sigma$ modulation of complex inputs. This is shown by an SNR performance comparison between the fourth-order quadrature modulator designed above and a pair of real fourth-order bandpass modulators designed for the same frequency specifications; both schemes use a total of eight filter orders.

An SNR histogram is shown in Fig. 15 for 1000 simulations of each system under the influence of 0.5%-peak random coefficient mismatch and amplifier dc gain between 50 and 60 dB—with 2-dB (i.e., about 25% linear gain) matching between a stage’s two amplifiers. The ninety-fifth percentile is 21 dB (3.5 b) higher for the quadrature modulator (at 67 dB) compared to the pair of real bandpass modulators (at 46 dB); Again, note that the large performance increase is for equal total modulator order.

The underlying reason for the superior performance of the quadrature modulator in converting complex inputs is that two zeros of each real bandpass-$\Delta\Sigma$-modulator are wasteful, shaping noise away from negative frequencies; they do not improve noise shaping within the desired band at positive frequencies, and in fact, they degrade it. This is because, as is well understood from filter theory, forcing attenuation on one half of the unit circle hurts attenuation on the other half [20]. The freedom to place notches on only one half of the unit circle means that quadrature $\Delta\Sigma$ modulators provide superior noise shaping for complex inputs.

Quadrature bandpass $\Delta\Sigma$ modulators also gain a stability-versus-bandwidth advantage over traditional bandpass modulators, in that their poles and zeros (which are not restricted to being in complex-conjugate pairs) are simply those of a rotated low-pass modulator [18]. Bandpass modulators—at least those near dc or $f_s/2$—are more akin to low-pass modulators that have been doubled in order.

V. CIRCUIT IMPLEMENTATION

The circuit is implemented in the CMOS-only portion of a 0.8-$\mu$m BiCMOS process [31]. System-level modulator simulations were run in Simulink [32] for $2^{20}$ time steps, using the optimized coefficients designed for the above NTF and STF. In an $L_\infty$-scaling procedure, the peak values obtained for each state—multiplied by 1.1 for a 10% safety margin—were used to scale down the input coefficients of the appropriate state (and scale up its output coefficients), so that each amplifier output will never exceed the reference levels.
The reference voltages (the levels fed back from the 1-b DAC’s in Fig. 11) are set at 1 and 4 V, centered around a common-mode (CM) level of 2.5 V (with 5-V supplies). Thus, each amplifier output is limited to 6-V differential swing—i.e., ±1.5 V around the 2.5-V CM level for each of the positive and negative amplifier outputs—and with the safety margin and coefficient scaling, should swing within about 90% of that range.

Absolute capacitor sizes set \( kT/C \) levels so that in-band noise requirements are met while minimizing capacitor area. The largest capacitors required in all stages are those responsible for setting noise-shaping zero locations (capacitors labeled as \( C_c, C_d, \) and \( C_f \) in Fig. 11)—which helps in positioning the notches accurately; these capacitors range in size from 0.7–2.7 pF. Conversely, the smallest (and thus least accurately implemented) capacitors in each stage realize a portion of either an \( A \) or \( B \) coefficient, which is propitious, since those coefficients are much more critical than the others.

### A. Switching Configuration

Fig. 16(a) shows the fully differential interconnection of the fourth-stage amplifier, switched capacitors, and latched comparator. A nonoverlapping clock generator produces the six necessary clock phases. Two versions of phase 1 (\( \phi_1 \) and \( \phi_1' \)), and four of phase 2 (\( \phi_2, \phi_2', \phi_2'', \) and their delayed counterparts) provide “early” and “late” clocking to minimize charge-injection. Transmission gates switch nodes with highly varying voltages. Integrators receive their input charge on the rising edge of phase 1 [note the clocking scheme in Fig. 16(b)] and have the entirety of that phase for settling. Phase 2’s rising edge then enables the comparator, whose output is latched into the RS flip-flop near the end of phase 2. This sets up the modulator feedback polarities for the following phase 1.

### B. Operational Transconductance Amplifier (OTA) Circuitry

1) **Main Stage:** The amplifiers (Fig. 17) are current-gain operational transconductance amplifiers [33] designed to drive the worst-stage capacitive load to 13-b settling in under 35 ns. In the main stage [Fig. 17(a)], the PMOS differential-pair (\( M_1-M_2 \)) converts the differential input voltage to a differential current, which is mirrored to the output, with a gain of two, by wide-swing cascode current mirrors (\( M_3-M_6 \) and \( M_7-M_{10} \)) [34]. \( M_{15}-M_{16} \) set the tail current for the input diff-pair, while devices \( M_{11}-M_{12} \) and \( M_{13}-M_{14} \) are cascoded active loads that help the amplifier achieve approximately 60-dB dc gain in simulations.

Volatges \( V_{n2}, V_{p1}, \) and \( V_{p2} \) are set by a separate bias stage, while \( V_{c1} \) is controlled by the common-mode feedback stage.

2) **Bias Stage:** A constant-\( g_m \) bias stage [Fig. 17(b)] [35] provides the bias levels for the main stage. The circuit is essentially a collection of high-swing cascode current mirrors connected in several feedback loops. The current in resistor \( R_b \) is set by the gate-source voltage differential between \( M_1 \) and \( M_2 \) which is defined by their aspect-ratio differential. This current flows in each of the transistor quads \( M_1-M_4 \) and \( M_5-M_8 \), which set the voltages \( V_{p1} \) and \( V_{n1} \) for the single-stacked devices in the main stage.

The same current is also mirrored to \( M_{15}-M_{16} \) and \( M_{12}-M_{13} \), which set the current in devices \( M_{11} \) and \( M_{14} \), respectively. The gate voltages of the latter devices, which are sized at one-quarter the width of the mirror devices driving them, define the appropriate bias levels \( V_{p2} \) and \( V_{n2} \) for the main stage’s “wide-swing” cascoded devices.

Thus, one high-resistance poly resistor sets the operating point for the amplifier. Furthermore, all device transconductances track, to a first degree, over power-supply, process, and temperature variations.
3) Common-Mode Feedback (CMFB) Stage: Switched-capacitor CMFB [36], shown in Fig. 17(c), maintains the average amplifier output level at 2.5 V. The amplifier outputs are ac averaged through the nonswitched capacitors $C_C$, whereas the (smaller) switched capacitors $C_S$ maintain the necessary dc levels. In brief, feedback forces $V_{c1}$ to equal $V_{p1}$, at which point the average of $V_{c1+}$ and $V_{c1-}$ is forced to equal the desired CM level ($V_{cm}$) of 2.5 V. Lead compensation is provided for the main amplifier by the resistors $R_k$ in series with the ac averaging capacitors in the CMFB block [37].

The CMFB has its own bias circuitry, shown in Fig. 17(d), which generates the CM level and supplies a replica of the $V_{p1}$ voltage that is generated in the main bias circuit. The separate bias circuitry keeps CMFB switching noise out of the main bias stage.

4) Performance: Simulations of the overall amplifier—with 2 pF input, integration, and load capacitors—indicate a unity-gain frequency of approximately 90 MHz, with greater than 70° phase margin and a smooth settling characteristic. It consumes 10.2 mW from 5 V supplies.

C. Comparator Circuitry

Fig. 18 shows the straightforward comparator circuitry [38], [39]; moderate offset and hysteresis effects are tolerable since they are either shaped out-of-band or cause artifacts at out-of-band frequencies.

The latched comparator is a simple CMOS comparator [Fig. 18(a)] followed by a clocked RS latch [Fig. 18(b)]. When phase 1 is high and, hence, phase 2 is low [see the clocks in Fig. 16(b)], the CMOS comparator is reset, since the NMOS latch ($M_1$–$M_4$) drains are tied together by $M_5$ and the PMOS latch ($M_5$–$M_8$) drains are pulled to the positive rail through $M_5$ and $M_1$. When the comparator is enabled on the rising edge of phase 2, these drains are released and the NMOS and PMOS latches latch preferentially to a polarity determined by the pull-down currents in the input NMOS devices ($M_1$–$M_2$).

Output inverters ($M_{12}$–$M_{15}$ and $M_{14}$–$M_{15}$) drive the S and R (set and reset) logic levels for the subsequent clocked RS latch. When the “latch” signal goes high, the $Q$ and $\overline{Q}$ levels are defined for the following clock cycle. This logic sets the appropriate levels for the reference signals fed back to the loop-filter capacitors.

VI. LAYOUT TECHNIQUES

Fully custom layout was generated with BALLISTIC [40], an analog-layout language that runs with Mentor Graphics’ GDT [41]. ASCII files containing code and parameters define device geometries and positions, spacing between objects, and
so on. A layout is constructed using both the user’s code and process-technology information as inputs, so that very little user effort (the proverbial “push of a button”) is required to generate new layouts. This is very useful for fast redesign in a new technology; modification of modulator specifications (order, sampling rate, bandwidth, etc.); modification of modulator flavor (real versus complex, low-pass versus bandpass); or for improved design of constituent circuitry (amplifiers, comparators, etc.).

The first implementation uses the CMOS-only portion of a 0.8-μm BiCMOS process [31]. Care was taken to ensure accurate capacitor ratioing: unit-sized capacitors and extra capacitors, all rimmed with dummy rings, set the necessary ratios. The nonunit extra capacitors maintain proper perimeter-to-area ratios.

A second layout was generated for a 0.5-μm CMOS process in only two weeks time. The fast turnaround time was possible with the coded-layout methodology, even though the second process has different design rules and layers than the first.

VII. EXPERIMENTAL RESULTS

A. Test Setup

A two-sided PCB (Fig. 19) houses the quadrature bandpass ΔΣ modulator IC and support circuitry. Standard shielding and ground-plane techniques isolate the digital and analog portions of the IC [42]. An RF Mini-Circuits 0/90° phase splitter converts the sinusoidal input into I and Q components, and 0/180° phase splitters convert each of these signals to fully differential form. A 10-MHz oscillator drives the IC clock, and a resistor chain sets the required bias voltages—1-V and 4-V references, and a 2.5-V common-mode level (with a 5-V supply). A second board contains two serial-to-parallel conversion blocks that buffer the single-bit I and Q streams from the modulator into 8-b wide words for collection by an HP-1664A logic analyzer. The data—64 kb per channel—is loaded into a Sun workstation for analysis using Matlab [29].

B. Measurements

An output spectrum, for zero input to the IC, is shown in Fig. 20(a). Note the wide-band noise-shaped region centered at 3.75 MHz—which is the in-band region—and the narrow notch at ~3.75 MHz—which is the image-band region. A similar plot for an input 8-dB below modulator full-scale (−8 dBFS) is shown in Fig. 20(b). Compare the noise-shaped output spectra with the NTF response shown in Fig. 13(b); clearly the IC performs the desired complex noise shaping.

The functionality of the STF is also apparent from Fig. 20(b). The input signal, a complex sinusoid positioned at slightly above 3.75 MHz, has passed through to appear in the modulator output spectrum with 20-dB gain (compared to the size of the input, which is not shown). This 20-dB in-band gain is expected from the STF response shown in Fig. 14(b).

A plot of measured SNDR versus input amplitude is shown in Fig. 21. The modulator attains a dynamic range of 67 dB (11 b) in 200-kHz bandwidth, increasing to 71 and 77 dB in the 100- and 30-kHz bandwidths, respectively. Maximum
SNDR is 62 dB (10 b) in 200 kHz; 65 dB in 100 kHz; and 69 dB in 30 kHz.

The histogram of Fig. 15 predicted a ninety-fifth-percentile for SNR of 67 dB (in 200-kHz bandwidth) for the quadrature $\Delta\Sigma$ modulator IC (with 0.5% coefficient mismatch and moderate amplifier nonideality), which falls marginally above the measured 62-dB peak value for SNDR. In addition, the increase in SNDR with oversampling ratio is less than is expected for ideal third-order noise-shaping. This is the result of excess in-band noise which is shaped to less than third degree, and which is, in fact, nearly white (note the approximately 3-dB/octave increase in SNDR with oversampling ratio). The presence of excess noise is confirmed by noting that the in-band noise-shaping in Fig. 20 does not contain the three distinct notches seen in the ideal NTF of Fig. 13(b). Some of the difference between expected SNR and measured SNDR can be attributed to in-band distortion products not seen in simulations, with the rest attributable to worse-than-predicted mismatch, circuit noise, etc.

C. Mismatch Effects

In an ideal complex filter structure, components exist as matched pairs in the $I$ and $Q$ channels in order to give a purely complex frequency response. In the circuit implementation of Fig. 11, coefficients are set by capacitor ratios—for example, the ratio of the feed-in capacitors $C_{\text{bi}}$ to their integrating capacitors $C_{\text{bi}}$ determine the loop-filter coefficients $b_4$ which appear once in each channel—so capacitor mismatch between channels unbalances the ideally matched coefficient pair; this mismatch causes a variety of deleterious effects [18], [30]. The effects are not catastrophic, but are discussed below, regardless, because of their interesting nature and their uniqueness to complex systems.

The most important type of mismatch occurs when the two paired components vary in a symmetric fashion about their nominal value. This differential error (not to be confused with errors between the single-ended half circuits of a differential structure) causes energy to alias from one frequency band to its conjugate band—such as aliasing from the band around $+3.75$ MHz to the conjugate band around $-3.75$ MHz, or vice-versa.

This phenomenon causes two troublesome effects: first, image-band quantization noise, which tends to be large since it is in the out-of-band region of a $\Delta\Sigma$ modulator, aliases into the in-band region, reducing SNR; second, any modulator input signals present in the image band alias to appear in the in-band region at the output, interfering with desired tones and reducing the image rejection of the modulator.

1) Mismatch-Induced SNR Degradation: A portion of the excess in-band noise in Fig. 20 is caused by out-of-band quantization noise around $-3.75$ MHz aliasing into the desired frequency band around $+3.75$ MHz by way of the mismatch-created INTF.

The magnitude of this effect can be inferred from Fig. 22(a). Here, 50 modulator simulations have been run with random 0.5% capacitor-ratio mismatch and moderate amplifier nonideality. The 50 resulting in-band INTF’s are superimposed on the 50 in-band NTF’s. Under the conditions described, the figure shows that aliased quantization noise will, in a typical simulation, tend to fill in the outer two notches of the NTF.

The transfer function responsible for this effect is called the image noise transfer function (INTF) since it provides a response from the image-band noise “input” to the desired band at the output; the in-band INTF gain is less than unity.

The transfer function responsible for this effect is called the image signal transfer function (ISTF) since it provides a response from the image-band signal input to the desired band at the output; the in-band ISTF gain is less than unity.
giving a slight SNR degradation. The effect is minimal, and therefore tolerable, since the notch placed in the image-band of the NTF has also placed a notch in the INTF, limiting the aliasing effect [30].

2) Mismatch-Induced Image-Rejection Degradation: The image-rejection effects of the ISTF are predicted in Fig. 22(b). The ideal STF has 20-dB in-band gain, whereas 50 ISTF’s, again generated in simulations with random mismatch, have between $-25$- and $-45$-dB in-band gain. So, equal-sized complex-tone inputs injected at $+3.75$ MHz and at $-3.75$ MHz will both appear in-band at the output, with the latter being 45–60-dB smaller than the former. This is an image-rejection figure.

In experimental tests, the major image-rejection limitation is not caused by the IC itself, but rather by the phase and amplitude imbalance of the phase-splitters used to drive the IC inputs. Specifications on these components list maximum amplitude/phase imbalances of $3^\circ/1.5$ dB and $2^\circ/0.1$ dB for the 90$^\circ$ and 180$^\circ$ splitters, respectively. Imbalances of even fractions of these values reduce image rejection to the neighborhood of 30 dB and cloud the performance of the IC. This matches measured values of just over 30 dB and leaves the simulated range of 45–60 dB as a best estimate for the actual image rejection of the IC.

The expected 45–60 dB modulator image rejection can be improved with improved matching accuracy and improved architecture [18] and may be sufficient in any case with strategic image placement (such that the rectangular image at $-f_{IF}$ is of limited size). It may also be possible to perform further $I/Q$ correction adaptively in the digital signal processor (DSP) [21].

Note that differential error also causes energy from the modulator input signal to appear in the image band at the output. The result of this is that, although the input was a pure complex-exponential tone, there is not only the desired tone near 3.75 MHz in the output spectrum of Fig. 20(b), but also a smaller tone in the image band near $-3.75$ MHz. Fig. 22(b) shows that the random ISTF’s have image-band gains between 0 and $-20$ dB—20–40-dB less than the 20-dB in-band STF gain. Indeed, the image-band tone in Fig. 20(b) is about 25 dB smaller than the in-band tone. The image-band tone is insignificant, since it is removed when the decimation filter eliminates all out-of-band frequency components, and thus, this effect is a harmless one.

D. Back-End Image Rejection and Anti-Alias Filtering

Note from Fig. 7(b) that even if the front-end quadrature mixer limits the extent to which images fall into the desired band at $+f_{IF}$, the (potentially) large image signal is mixed to $-f_{IF}$ and appears as an image-band input to the back-end blocks (anti-alias filters and A/D converters). Regardless of what type of filters and A/D converters are used, mismatch in amplitude and phase between the two paths of the complex back end causes some of that large image-band input to alias into the in-band region, thereby degrading useful information [18], [24], [25].

Histograms for image rejection were performed under the same mismatch conditions described above. The quadrature modulator realizes an image-rejection ninety-fifth-percentile of 45 dB, compared to 27 dB for a real-modulator pair. The quadrature $\Delta\Sigma$ modulator’s strong internal cross-coupling improves its image rejection over a noncoupled pair of bandpass modulators, since it maintains more symmetry within its pairs of transfer functions than is possible in a system of uncoupled real modulators. In fact, strongly cross-coupled complex systems consistently gain an advantage over systems that operate on $I$ and $Q$ paths in an uncoupled manner.

If required, a large improvement in back-end image rejection can be realized by applying complex-filtering techniques to the anti-alias filter block as well [21]. Fig. 23 shows how a complex filter centered at $+f_{IF}$ attenuates the image at $-f_{IF}$. Since the transition bands are much wider at this IF stage, even a low-order complex anti-alias filter can significantly improve back-end image rejection, to the point where it is insignificant next to the limitations of the receiver front end. Complex continuous-time filters exist in the literature and are reasonably straightforward to implement using standard techniques [24], [26].

Not only does complex anti-alias filtering offer substantial back-end image rejection, it also shows great efficacy in the attenuation of alias components. The complex anti-alias filter has a transition band equal to $2\pi f_s$, whereas the pair of real filters—designed for a signal band centered at

$^9$ For example, 0.5 dB and 0.5$^\circ$ of $I/Q$-input imbalance reduces image rejection to 30.7 dB.

$^{10}$ Note that use of a pair of real anti-alias filters provides no image attenuation, since each real filter is constrained to having a symmetric magnitude response; thus, since each filter must pass signals at $+f_{IF}$, it must pass the image signals at $-f_{IF}$ equally well.
Fig. 23. Complex anti-alias filtering in a complex-sampling system.

Fig. 24. Microphotograph of the 0.8-μm CMOS quadrature bandpass ΔΣ IC.

$3\pi/4 (3f_s/8)$—has a transition band equal to only $\pi/2 (f_s/4)$ [18], a substantial two-octave reduction.

E. IC Floorplan

The 0.8-μm CMOS IC occupies a die size of approximately 2.4 × 1.8 mm² and is shown in Fig. 24. The real channel lies horizontally along the upper portion of the die, with its four stages running left to right. The vertical symmetry within the channel is due to the differential nature of the design.

The similar imaginary channel lies below its real counterpart, with the two channels separated by a clock bus. The input-switching structure, placed at the left side of the die, feeds input samples into buses that run above and below each channels’ amplifiers. The comparators are located to the right of the channel with which they are associated, with the one-bit DAC’s between them. Digital support circuitry, such as the clock generator and pad drivers, is located at the far right of the die.

F. IC Performance Summary

Power consumption for the 0.8-μm CMOS IC is 130 mW for 5-V supplies. Its performance is summarized in Table I.

The IC uses standard switched-capacitor circuit techniques, and so can be pushed in performance as can any such system. Faster constituent circuitry (amplifiers, comparators, etc.) would allow higher sampling rates, which in turn would provide a higher degree of oversampling and a corresponding increase in SNR performance.

Switched-capacitor ΔΣ modulators in the literature have reached sampling rates in the 50-MHz range [43]–[45], and even an impressive 160 MHz [46]. At these rates, bandpass-ΔΣ-modulator center frequencies (and thus receiver IF’s) of 10 to 50 MHz are feasible: levels which provide even a moderate-Q front-end filter with enough of a transition band to contribute to image rejection. For example, a front-end second-order bandpass filter with a Q of 20 would provide more than 12 dB image attenuation with a 50-MHz IF.\(^{11}\)

In a similar fashion to traditional ΔΣ modulators, higher-order noise-shaping functions, or finer-resolution internal quantizers and feedback DAC’s, can also be used to improve modulator performance.

VIII. CONCLUSIONS

Low-IF receiver architectures, which use a nonzero IF to avoid the many problems of direct-conversion receivers, were discussed. Their two-path structure helps alleviate passive filter requirements, but means that they suffer from several unique and deleterious effects when subjected to path mismatch. Front-end mismatch concerns can be minimized with use of modern image-reject-mixer techniques and strategic image placement, making these architectures a viable solution for future-generation digital, monolithic, radio receivers.

Back-end mismatch between pairs of anti-alias filters and A/D converters is similarly a problem, but a quadrature version of a bandpass ΔΣ modulator was presented that uses strong internal cross-coupling and special transfer-function design to alleviate mismatch concerns. Complex anti-aliasing filtering, too, can prove helpful in meeting back-end requirements.

Quadrature bandpass ΔΣ modulators—which use complex filtering embedded in ΔΣ loops to efficiently realize asymmetric noise-shaped spectra—were shown to have superior

$^{11}$Integrated active-RLC bandpass filters from the literature use $Q$ enhancement to increase selectivity, and in fact have realized stable $Q$’s of nearly 500. At present, however, their overall performance is insufficient for digital radio systems [47], [48].
performance over pairs of real bandpass modulators when operating on narrowband complex input signals. The prototype IC realizes the predicted asymmetric noise shaping and offers 67-dB dynamic range for 200-kHz bandwidth complex (i.e., $I$ and $Q$) input signals centered at 3.75 MHz. Its implementation in standard CMOS, using switched-capacitor circuit techniques, suggests that quadrature bandpass $\Delta \Sigma$ modulator performance can increase in the manner that it has for traditional low-pass and bandpass $\Delta \Sigma$ modulators.

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REFERENCES


Stephen A. Jantzi (S’93–M’97) was born in London, ON, Canada, in 1966. He received the B.E.Sc. degree in electrical engineering from the University of Western Ontario, Canada, in 1989 and the M.A.Sc. and Ph.D. degrees from the University of Toronto in 1992 and 1997, respectively. He briefly joined Analog Devices Inc., Wilmington, MA, between his M.A.Sc. and Ph.D. studies, where he worked on $\Sigma\Delta$ data-converter design in the sound processing group. He has also been a consultant to several high-technology companies, specializing in the area of bandpass $\Sigma\Delta$ modulator design and implementation. He currently holds the position of Staff Scientist at Broadcom Corporation, Irvine, CA. His research interests include analog signal processing, high-performance integrated-circuit design, and the application of $\Sigma\Delta$ noise-shaping converters to wired and wireless communications systems.

Kenneth W. Martin (S’75–M’80–SM’89–F’91) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, Canada, in 1975, 1977, and 1980, respectively. From 1977 to 1978, he was a member of the Scientific Research Staff at Bell Northern Research, Ottawa, Canada, where he did some of the early research in integrated, switched-capacitor networks. Between 1980 and 1992, he was consecutively an Assistant, Associate, and Full Professor at the University of California at Los Angeles. In 1992, he accepted the endowed “Stanley Ho Professorship in Microelectronics” at the University of Toronto. He has also been a consultant to many high-technology companies including Xerox Corp., Hughes Aircraft Co., Intel Corp., and Brooktree Corp., in the areas of high-speed analog and digital integrated circuit design. He has ongoing research programs in the areas of integrated circuits and systems. Recently, most of his research has focused on data-communication systems, both wired and wireless, as well as CAD for analog IC design. Recently, he completed, along with co-author D. Johns, a textbook entitled Analog Integrated Circuit Design (Wiley, 1997). In addition, he has co-authored three other books in cooperation with former Ph.D. students.

Dr. Martin was appointed as the Circuits and Systems IEEE Press Representative (1985–1986). He was selected by the Circuits and Systems Society for the Outstanding Young Engineer Award that was presented at the IEEE Centennial Keys to the Future Program in 1984. He was elected by the Circuits and Systems Society members to their administrative committee (ADCOM 1985–1987). He served as an Associate Editor of the TRANSACTIONS ON CIRCUITS AND SYSTEMS from 1985 to 1987 and has served on the technical committee for many International Symposia on Circuits and Systems. He is currently an Associate Editor for the PROCEEDINGS of the IEEE and a member of the IEEE Circuits and Systems Board of Governors (1995–1997). He was awarded a National Science Foundation Presidential Young Investigator Award that ran from 1985 to 1990. He was a co-recipient of the Beatrice Winner Award at the 1993 ISSCC.

Adel S. Sedra (M’66–SM’82–F’84) received the B.Sc. degree from Cairo University, Egypt, in 1964, and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, in 1968 and 1969, respectively, all in electrical engineering. He joined the faculty of the University of Toronto in 1969 and was promoted to Associate Professor in 1972 and to Professor in 1978. During 1986–1993, he served as Chair of the Department of Electrical Engineering (now Electrical and Computer Engineering). On July 1, 1993, he assumed the position of Vice-President, Provost, and Chief Academic Officer of the University of Toronto. His research has centered on the theory and design of circuits for communication and instrumentation systems and has resulted in about 130 papers. He has co-authored three textbooks. One of his books, Microelectronic Circuits (Oxford University Press), which first appeared in 1982, is currently in its fourth edition and has been translated into eight languages and is currently in use at hundreds of Universities around the world. He has served as a consultant to industry and government in Canada and the United States.

Dr. Sedra has helped found two centers-of-excellence in information technology and microelectronics and currently serves on the board of directors of a number of organizations dedicated to the promotion and sponsorship of research. He has also been active in professional societies, most notably the IEEE, serving in a variety of roles. His research and educational activities have won him a number of awards and honors including the 1984 Darlington Award, the 1987 Guillemin-Cauer Award, and the 1994 Education Award, all of the IEEE Circuits and Systems Society; Fellow, Ryerson Polytechnic University (1989); the 1993 Information Technology of Canada/NSERC Research Excellence Award; and the 1996 IEEE Education Medal.