Pipelining

• Principles of pipelining
• Simple pipelining
• Structural Hazards
• Data Hazards
• Control Hazards
• Interrupts
• Multicycle operations
• Pipeline clocking
Sequential Execution Semantics

We will be studying techniques that exploit the semantics of Sequential Execution.

Sequential Execution Semantics:

instructions *appear* as if they executed in the program specified order and one after the other

Alternatively

At any given point in time we should be able to identify an instruction so that:

1. All preceding instructions have executed

2. None following has executed
Sequential Execution Semantics

• **Contract:** This is how the machine *appears* to behave

![Diagram](image-url)
Exploiting Sequential Semantics

• The “it should appear” is the key

• The only way one can inspect execution order is via the machine’s state

This includes registers, memory and any other named storage

We will looking at techniques that relax execution order while preserving sequential execution semantics
Instruction Classification

• One way or another most computers are capable of performing the following actions:

1. Move data from one location to another: memory or register read/write

2. Manipulate data: add, sub, etc.

3. Based on data decide what to do next: branch, jump, etc.
Steps of Instruction Execution

Instruction execution is not a monolithic action

There are multiple *micro-actions* involved

- Fetch
- Decode
- Read Operands
- Operation
- Writeback Result
- Determine Next Instruction
Pipelining: Partially Overlap Instructions

**Unpipelined**

- Instructions
- Time
- 1/Throughput
- Latency

**Pipelined**

- Instructions
- Time
- 1/Throughput
- Latency

**Ideally:** \( Time_{\text{pipeline}} = \frac{Time_{\text{sequential}}}{\text{PipelineDepth}} \)

This ignores fill and drain times
Pipelining is much more general

- No need to "break" at the micro-action level

- Logic (n gate delay) with BW = 1/n

- n/2 with BW = 2/n

- n/3 with BW = 3/n

• No need to “break” at the micro-action level
Sequential Semantics Preserved?

Two execution states:

1. **In-progress**: changes not visible to outsiders
2. **Committed**: changes visible
Principles of Pipelining: Ideal Case

Let $T$ be the time to execute an instruction.

Instruction execution requires $n$ stages, $t_1...t_n$ taking $T = \sum t_i$

W/O pipelining: $TR = \frac{1}{T} = \frac{1}{\sum t_i}$ \quad Latency = $T = \frac{1}{TR}$

W/ n-stage pipeline: $TR = \frac{1}{\max(t_i)} \leq \frac{n}{T}$ \quad Latency = $n \times \max(t_i) \geq T$

\[ Speedup = \frac{\sum t_i}{\max(t_i)} \leq n \]

If all $t_i$ are equal, Speedup is $n$

Ideally: Want higher Performance? Use more pipeline stages
Principles of Pipelining: Example

Overlap

Pick Longest Stage

Critical Path Determines Clock Cycle
Pipelining Limits

• After a certain number of stages benefits level off and start diminishing

• Pipeline utility is limited by:

1. Implementation
   a. Logic Delay
   b. Clock Skew/Jitter
   c. Latch Delay

2. Structures

3. Programs

2 & 3 will be called HAZARDS
Logic Delay: FO4

- How does the speed of a gate depend on technology?
- Use a Fanout of 4 inverter metric

![FO4 Diagram]

- Measure the delay of an inverter with $C_{out}/C_{in} = 4$

- Divide speed of a circuit by speed of FO4 inverter
  - Get delay of circuit in measured in FO4 inverters
  - Metric pretty stable, over process, temp, and voltage

Source: M. Horowitz
**FO4 Inverter Delay under Scaling**

- Device performance will scale
  - FO4 delay has been linear with tech
    Approximately $0.36 \text{nS/}\mu\text{m} \cdot L_{\text{drawn}}$ at TT
    (0.5nS/\mu m under worst-case conditions)
- Easy to predict gate performance
  - We can measure them
    - Labs have built 0.04\mu m devices
  - Key issue is voltage scaling

*Source: M. Horowitz*
Gates Per Clock

- Clock speed has been scaling faster than base technology
- Number of FO4 delays in a cycle has been falling

- Number of gates decrease 1.4x each generation
- Caused by:
  - Faster circuit families (dynamic logic)
  - Better optimization
- Approaching a limit:
  - <16 FO4 is hard
  - < 8 FO4 is very hard
Pipeline Limits: #1 Logic Delay

- $t_l$ = logic block’s worst case delay
- $T$ = clock period
- $T \geq t_l$
- Today’s Procs:
  6-12 2-input gates per stage
Pipelining Limits: #2 Clock Skew

**CLOCK SKEW**
- Clock takes time to travel
- Arrival depends on distance/load
- Skew amongst different connections
- Creates additional constraints

```
CLOCK Skew Diagram
```

```
DIE
```

```
Clock Skew
```

```
© 1998 by Hill, Wood, Sohi, Smith and Vijaykumar and Moshovos
```
Clock Skew contd.

- Output from stage with late clock feeds stage with early clock
Pipelining Limits: #3 Latch Overhead

- Latch takes time
  - Setup Time
    data must stay stable before clock edge
  - Hold Time
    data must stay stable after clock edge

computation starts should complete before this

\[ t_I \]

setup hold

\[ T \]
Impact of Clock Skew and Latch Overheads

Let $X$ be extra delay per stage for

- latch overhead
- clock/data skew

$X$ limits the useful pipeline depth

With $n$-stage pipeline (all $t_i$ equal) ($T = n \times t$)

- throughput $= \frac{1}{X + t} < \frac{n}{T}$
- latency $= n \times (X + t) = n \times X + T$
- speedup $= \frac{T}{(X + t)} \leq n$

Real pipelines usually do not achieve this due to Hazards
T = 500. A: X=100, B: X=10
Cost/Performance Tradeoff

\[ \text{Cost} = n \times L + B \]

where \( L = \text{cost of adding each latch} \)
\( n = \text{number of stages} \)
\( B = \text{cost without pipelining} \)

\[ \text{Performance} = \text{Throughput} = \frac{1}{(X + T/n)} \]

where \( T = \text{latency without pipelining} \)
\( n = \text{number of stages} \)
\( X = \text{overhead per stage} \)

Cost/Performance Trade-off

Cost/Perf = \[\frac{Ln + B}{\frac{1}{T/n + X}}\] = LT + BX + LXn + BT/n

Optimal Cost/Performance: \[\min \text{Cost/Perf}(n)\]

\[n_{\text{opt}} = \sqrt{\frac{BT}{LX}}\]
Cost/Performance Trade-off

\[ T = 500, B=200. A: X = 10 & L = 20, B: X = 20 & L = 40 \]
Pipelining Idealism

• **Uniform latency Micro-actions**

Perfectly balanced stages

• **Identical Micro-actions**

Must perform the same steps per instruction

• **Independence of micro-actions across instructions**

No need to wait for a previous instruction to finish

No need to use the same resource at the same time
Simple pipelines

F- fetch, D - decode, X - execute, M - memory, W - writeback

Classic 5-stage Pipeline
MIPS Actions per instruction

All need to be fetched and change the PC at the end

• integer/logic operations

add $11, $3, $7 --> read 2 regs, write one

• branches

beq $1, $7, LALA --> read 2 regs, compare, change PC

• load/store

lw $1, 7($3) --> read 1 reg, add, read memory, write reg
sw $5, 3($7) --> read 2 regs, add, write memory

• special ops: syscall, jumps, call/return

read at most 1 reg, write at most 1 reg, may change PC
Non-Pipelined Implementation
Pipelined Implementation

Pipelined Implementation: Ideally 5x performance
Pipelining as Datapaths in Time

Time

MEM → REG → MEM → REG → MEM → REG → MEM → REG
Hazards

Hazards

• conditions that lead to incorrect behavior if not fixed

Structural Hazard

• two different instructions use same resource in same cycle

Data Hazard

• two different instructions use same storage
• must appear as if the instructions execute in correct order

Control Hazard

• one instruction affects which instruction is next
Structural Hazards

When two or more different instructions want to use the same hardware resource in the same cycle

- e.g., load and stores use the same memory port as IF
Dealing with Structural Hazards

Stall:
+ low cost, simple
– decrease IPC
• use for rare case

Pipeline Hardware Resource:
• useful for multicycle resources
+ good performance
– sometimes complex e.g., RAM
– Example 2-stage cache pipeline: decode, read or write data (wave pipelining - generalization)
Dealing with Structural Hazards

Replicate resource

+ good performance
– increases cost
– increased interconnect delay?

• use for cheap or divisible resources
Impact of ISA on Structural Hazards

Structural hazards are reduced

- If each instruction uses a resource at most once
- Always in same pipeline stage
- For one cycle

Many RISC ISAs designed with this in mind
Data Hazards

When two different instructions use the same storage location it must *appear* as if they executed in sequential order.

```
add r1, r2, --
sub r2, --, r1
add r3, r1, --
or r1, --, --
```

- *read-after-write* (RAW, true dependence) -- real
- *write-after-read* (WAR, anti-dependence) -- artificial
- *write-after-write* (WAW, output-dependence) -- artificial
- *read-after-read* (no hazard)
Data Hazards
Examples of RAW

```
add r1, --, --         IF  ID  EX  MEM  WB
                        r1 written
sub  --, r1, --        IF  ID  EX  MEM  WB
                        r1 read - not OK
load r1, --, --        IF  ID  EX  MEM  WB
                        r1 written
sub  --, r1, --        IF  ID  EX  MEM  WB
                        r1 read - not OK
sw  r1, 100(r2)        IF  ID  EX  MEM  WB
lw  r1, 100(r2)        IF  ID  EX  MEM  WB
                  OK

unless 100(r2) is the PC of the load (self-modifying code)
```
Simple Solution to RAW

Hardware detects RAW and stalls

\[
\begin{align*}
\text{add } r1, --, -- & \quad \text{IF ID EX MEM WB} \\
\text{sub } --, r1, -- & \quad \text{IF stall stall IF ID EX MEM WB}
\end{align*}
\]

+ low cost, simple
– reduces IPC

Maybe we should try to minimize stalls
Stall Methods

Compare ahead in pipe

- if \( \text{rs1(EX)} = \text{Rd(MEM)} \) \( \lor \) \( \text{rs2(EX)} = \text{Rd(MEM)} \) then stall
- assumes MEM instr is a load, EX instr is ALU
- Use register reservation bits

one bit per register

set at ID stage  

\[ \text{clear at MEM stage} \]

loads reserve at ID stage
release at MEM stage

check source Reg bit
stall if reserved
Minimizing RAW stalls

Bypass or Forward or Short-Circuit

- Use data before it is in register
  + reduces/avoids stalls
  - complex
  - Deeper pipelines -> more places to bypass from
  • crucial for common RAW hazards
Bypass

Interlock logic

• detect hazard

• bypass correct result to ALU

Hardware detection requires extra hardware

• instruction latches for each stage

• comparators to detect the hazards
Bypass Example
Bypass: Control Example

Mux control

- if insn(EX) uses immediate then select IMM
- else if rs2(EX) == rd(MEM) then ALUOUT(MEM)
- else if rs2(EX) == rd(WB) then ALUOUT(WB)
- else select B
RAW solutions

Hybrid (i.e., stall and bypass) solutions required sometimes

\[
\text{load } r1, --, -- \quad \text{IF} \quad \text{ID} \quad \text{EX} \quad \text{MEM} \quad \text{WB} \\
\text{sub } --, r1, -- \quad \text{stall} \quad \text{IF} \quad \text{ID} \quad \text{EX} \quad \text{MEM} \quad \text{WB}
\]

DLX has one cycle bubble if load result used in next instruction

Try to separate stall logic from bypass logic

- avoid irregular bypasses
Pipeline Scheduling - Compilers can help

Instructions scheduled by compiler to reduce stalls

\[ a = b + c; \quad d = e + f \quad -- \text{Prior to scheduling} \]

\[
\begin{align*}
\text{lw} & \quad Rb, \quad b \\
\text{lw} & \quad Rc, \quad c \\
\text{stall} & \\
\text{add} & \quad Ra, \quad Rb, \quad Rc \\
\text{sw} & \quad a, \quad ra \\
\text{lw} & \quad Re, \quad e \\
\text{lw} & \quad Rf, \quad f \\
\text{stall} & \\
\text{sub} & \quad Rd, \quad Re, \quad Rf \\
\text{sw} & \quad d, \quad Rd
\end{align*}
\]
Pipeline Scheduling

After scheduling

lw Rb, b
lw Rc, c
lw Re, e
add Ra, Rb, Rc
lw Rf, f
sw a, ra
sub Rd, Re, Rf
sw d, Rd1

No Stalls
Delayed Load

Avoid hardware solutions - Let the compiler deal with it
Instruction Immediately after load can’t/shouldn’t see load result
Compiler has to fill in the *delay slot* - NOP might be necessary

```
lw Rb, b
lw Rc, c
nop
add Ra, Rb, Rc
sw a, Ra
lw Re, efs
lw Rf, f
nop
add Rd, Re, Rf ...
```

```
lw Rb, b
lw Rc, c
lw Rf, f
add Ra, Rb, Rc
lw Rf, f
sw a, Ra
sub Rd, Re, Rf
sw d, Rd
```
Other Data Hazards

WAR

\[
\begin{align*}
\text{add } & r1, r2, -- \\
\text{sub } & r2, --, r1 \\
\text{or } & r1, --, -- \\
\end{align*}
\]

Not possible in DLX - read early write late
Consider late read then early write
ALU ops writeback at EX stage
MEM takes two cycles and stores need source reg after 1 cycle

\[
\begin{align*}
\text{sw } & r1, -- \\
\text{add } & r1, --, -- \\
\text{MUL } & --, 0(r2), r1 \\
\text{lw } & --, (r1++) \\
\end{align*}
\]
Other Data Hazards

WAW

Not in DLX: register writes are in order

consider slow then fast operation

divf fr1, --, --

mov --, fr1

addf fr1, --, --

update r1 not OK
Control Hazards

When an instruction affects which instruction execute next or changes the PC

- \( \text{sw} \ $4, 0($5) \)
- \( \text{bne} \ $2, $3, \text{loop} \)
- \( \text{sub} - , - , - \)

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<td>sw</td>
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Control Hazards

Handling control hazards is very important

VAX e.g.,
- Emer and Clark report 39% of instr. change the PC
- Naive solution adds approx. 5 cycles every time
- Or, adds 2 to CPI or ~20% increase

DLX e.g.,
- H&P report 13% branches
- Naive solution adds 3 cycles per branch
- Or, 0.39 added to CPI or ~30% increase
Handling Control Hazards

Move control point earlier in the pipeline

• Find out whether branch is taken earlier
• Compute target address fast

Both need to be done

e.g., in ID stage

• target := PC + immediate
• if (Rs1 op 0) PC := target
### Handling Control Hazards

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<tr>
<td>N: sw</td>
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<tr>
<td>N+1: bne</td>
<td>F</td>
<td>D</td>
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<tr>
<td>N+2: add</td>
<td>F</td>
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<tr>
<td>Y: sub</td>
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<td>D</td>
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**Implies only one cycle bubble but**

- special PC adder required
- What if we want a deeper pipeline?
ISA and Control Hazard

Comparisons in ID stage

- must be fast
- can’t afford to subtract
- compares with 0 are simple
- gt, lt test sign-bit
- eq, ne must OR all bits

More general conditions need ALU

- DLX uses conditional sets
Handling Control Hazards

Branch prediction

- guess the direction of branch
- minimize penalty when right
- may increase penalty when wrong

Techniques

- static - by compiler
- dynamic - by hardware
- MORE ON THIS LATER ON
Handling Control Hazards

Static techniques

• predict always not-taken
• predict always taken
• predict backward taken
• predict specific opcodes taken
• delayed branches

Dynamic techniques

• Discussed with ILP
Handling Control Hazards

Predict not-taken always

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if taken then squash (aka abort or rollback)

- will work only if no state change until branch is resolved
- DLX - ok - why?
- VAX - autoincrement addressing?
Handling Control Hazards

Predict taken always

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For DLX must know target before branch is decoded

• can use prediction

• special hardware for fast decode

Execute both paths - hardware/memory b/w expensive
Handling Control Hazards

Delayed branch - execute next instruction whether taken or not

- i: \text{beqz r1, #8}
- i+1: \text{sub --, --, --}
- . . . .
- i+8: \text{or --, --, --} (reused by RISC invented by microcode)

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<td>i+1 (delay slot)</td>
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<td>M</td>
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<td>i+8</td>
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Filling in Delay slots

Fill with an instr before branch

• When? if branch and instr are independent.
• Helps? always

Fill from target (taken path)

• When? if safe to execute target, may have to duplicate code
• Helps? on taken branch, may increase code size

Fill from fall-through (not-taken path)

• when? if safe to execute instruction
• helps? when not-taken
Filling in Delay Slots cont.

From Control-Independent code:
that’s code that will be *eventually* visited no matter where the branch goes

Nullifying or Cancelling or Likely Branches:
Specify when delay slot is execute and when is squashed

**Why?** Increase fill opportunities

**Major Concern w/ DS:** Exposes implementation optimization
Comparison of Branch Schemes

Cond. Branch statistics - DLX

• 14%-17% of all insts (integer)
• 3%-12% of all insts (floating-point)
• Overall 20% (int) and 10% (fp) control-flow insts.
• About 67% are taken

Branch-Penalty = %branches x
(%taken x taken-penalty + %not-taken x not-taken-penalty)
## Comparison of Branch Schemes

<table>
<thead>
<tr>
<th>scheme</th>
<th>taken penalty</th>
<th>not-taken pen.</th>
<th>CPI penalty</th>
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<tbody>
<tr>
<td>naive</td>
<td>3</td>
<td>3</td>
<td>0.420</td>
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<td>fast branch</td>
<td>1</td>
<td>1</td>
<td>0.140</td>
</tr>
<tr>
<td>not-taken</td>
<td>1</td>
<td>0</td>
<td>0.091</td>
</tr>
<tr>
<td>taken</td>
<td>0</td>
<td>1</td>
<td>0.049</td>
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<tr>
<td>delayed branch</td>
<td>0.5</td>
<td>0.5</td>
<td>0.070</td>
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</tbody>
</table>

**Assuming:** branch% = 14%, taken% = 65%, 50% delay slots are filled w/ useful work

**ideal CPI is 1**
Impact of Pipeline Depth

Assume that now penalties are doubled

For example we double clock frequency

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<th>taken penalty</th>
<th>not-taken pen.</th>
<th>CPI penalty</th>
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<tbody>
<tr>
<td>naive</td>
<td>6</td>
<td>6</td>
<td>0.840</td>
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<td>fast branch</td>
<td>2</td>
<td>2</td>
<td>0.280</td>
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<tr>
<td>not-taken</td>
<td>2</td>
<td>0</td>
<td>0.182</td>
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<tr>
<td>taken</td>
<td>0</td>
<td>2</td>
<td>0.098</td>
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<tr>
<td>delayed branch</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>

Delayed Branches need special support for interrupts
Interrupts

Examples:

- power failing, arithmetic overflow
- I/O device request, OS call, page fault
- Invalid opcode, breakpoint, protection violation

Interrupts (aka faults, exceptions, traps) often require

- surprise jump (to vectored address)
- linking return address
- saving of PSW (including CCs)
- state change (e.g., to kernel mode)
Classifying Interrupts

1a. synchronous
   • function of program state (e.g., overflow, page fault)

1b. asynchronous
   • external device or hardware malfunction

2a. user request
   • OS call

2b. coerced
   • from OS or hardware (page fault, protection violation)
Classifying Interrupts

3a. User Maskable
   User can disable processing

3b. Non-Maskable
   User cannot disable processing

4a. Between Instructions
   Usually asynchronous

4b. Within an instruction
   Usually synchronous - Harder to deal with

5a. Resume
   As if nothing happened? Program will continue execution

5b. Termination
Restartable Pipelines

- Interrupts within an instruction are not catastrophic
- Most machines today support this
  Needed for virtual memory
- Some machines did not support this
  Why?
    Cost
    Slowdown
Key: Precise Interrupts
Will return to this soon
First let’s consider a simple DLX-style pipeline
Handling Interrupts

Precise interrupts (sequential semantics)

- Complete instructions before the offending instr
- Squash (effects of) instructions after
- Save PC (& next PC with delayed branches)
- Force trap instruction into IF

Must handle simultaneous interrupts

- IF, M - memory access (page fault, misaligned, protection)
- ID - illegal/privileged instruction
- EX - arithmetic exception
Interrupts

E.g., data page fault

```
  1  2  3  4  5  6  7  8  9
 i  F  D  X  M  W
i+1 F  D  X  M  W  <- page fault
i+2 F  D  X  <- squash
i+3 F  D  <- squash
i+4 F  <- squash
 x  trap -> F  D  X  M  W
 x+1 trap handler -> F  D  X  M  W
```
Interrupts

Preceding instructions already complete

Squash succeeding instructions
  • prevent them from modifying state (registers, CC, memory)

trap instruction jumps to trap handler

hardware saves PC in IAR

trap handler must save IAR
Interrupts

E.g., arithmetic exception

1  2  3  4  5  6  7  8  9
i  F  D  X  M  W
i+1  F  D  X  M  W
i+2  F  D  X
<- exception
i+3  F  D
<- squash
i+4  F
<- squash
x  trap ->  F  D  X  M  W
x+1  trap handler ->  F  D  X  M  W
Interrupts

E.g., Instruction fetch page fault

\[
\begin{array}{ccccccc}
1 & 2 & 3 & 4 & 5 & 6 & 7 \\
\hline
i & F & D & X & M & W \\
i+1 & F & D & X & M & W \\
i+2 & F & D & X & M & W \\
i+3 & F & D & X & M & W \\
i+4 & F & & & \text{<- page fault} \\
x & \text{trap ->} & F & D & X & M & W \\
x+1 & \text{trap handler ->} & F & D & X & M & W \\
\end{array}
\]
Interrupts

Let preceding instructions complete

No succeeding instructions

What happens if i+3 causes a data page fault?
### Interrupts

**Out-of-order interrupts**

- which page fault should we take?

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
</tr>
</thead>
<tbody>
<tr>
<td>i</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>i+1</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>i+2</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>i+3</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

page fault (Mem)

page fault (fetch)
Out-of-Order Interrupts

Post interrupts

• check interrupt bit on entering WB
• precise interrupts
• longer latency

Handle immediately

• not fully precise
• interrupt may occur in order different from sequential CPU
• may cause implementation headaches!
Interrupts

Other complications

- odd bits of state (e.g., CC)
- early-writes (e.g., autoincrement)
- instruction buffers and prefetch logic
- dynamic scheduling
- out-of-order execution

Interrupts come at random times

Both Performance and Correctness

- frequent case not everything
- rare case MUST work correctly
Delayed Branches and Interrupts

What happens on interrupt while in delay slot

- next instruction is not sequential

Solution #1: save multiple PCs

- save current and next PC
- special return sequence, more complex hardware

Solution #2: single PC plus

- branch delay bit
- PC points to branch instruction
- SW Restrictions
Multicycle operations

Not all operations complete in 1 cycle

- FP slower than integer
- 2-4 cycles multiply or add
- 20-50 cycles divide

Extend DLX pipeline

- EX stage repeated multiple times
- multiple, parallel functional units
  - not pipelined for now
Handling Multicycle Operations

Four functional units

- EX: integer
- E*: FP/integer multiplier
- E+: FP adder
- E/: FP/integer divider

Assume

- EX takes 1 cycle and all FP take 4 cycles
- separate integer and FP registers
- all FP arithmetic in FP registers

Worry about hazards

- structural, RAW (forwarding), WAR/WAW (between I & FP)
## Multicycle Example

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>int</td>
<td>F</td>
<td>D</td>
<td>X</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fp*</td>
<td>F</td>
<td>D</td>
<td>E*</td>
<td>E*</td>
<td>E*</td>
<td>E*</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>int</td>
<td>F</td>
<td>D</td>
<td>EX</td>
<td>M</td>
<td>W</td>
<td>(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fp/</td>
<td>F</td>
<td>D</td>
<td>E/</td>
<td>E/</td>
<td>E/</td>
<td>E/</td>
<td>M</td>
<td>W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>int</td>
<td>F</td>
<td>D</td>
<td>EX</td>
<td>M</td>
<td>W</td>
<td>(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fp/</td>
<td>F</td>
<td>D</td>
<td>--</td>
<td>--</td>
<td>E/</td>
<td>E/</td>
<td>(3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fp*</td>
<td>F</td>
<td>--</td>
<td>--</td>
<td>D</td>
<td>X</td>
<td>(4)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Simple Multicycle Example

Notes:

- (1) - no WAW but complicates interrupts
- (2) - no WB conflict
- (3) - stall forced by structural hazard
- (4) - stall forced by in-order issue

Different FP operation times are possible
- Makes FP WAW hazards possible
- Further complicates interrupts
FP Instruction Issue

Check for structural hazards
- wait until functional unit is free

Check for RAW - wait until
- source regs are not used as destinations by instrs in EX_i

Check for forwarding
- bypass data from MEM or WB if needed

What about overlapping instructions?
- contention in WB
- possible WAR/WAW hazards
- interrupt headaches
Overlapping Instructions

Contention in WB

- static priority
- e.g., FU with longest latency
- instructions stall after issue

WAR hazards

- always read registers at same pipe stage

WAW hazards

- divf f0, f2, f4 followed by subf f0, f8, f10
- stall subf or abort divf’s WB
Multicycle Operations

Problems with interrupts

• DIVF f0, f2, f4
• ADDF f2, f8, f10
• SUBF f6, f4, f10

ADDF completes before DIVF

• Out-Of-Order completion
• Possible imprecise interrupts

What if divf excepts after addf/subf complete?

Precise Interrupts Paper
Precise Interrupts

- Simple solution: Modify state only when all preceding insts. are known to be exception free.

Mechanism: *Result Shif Register*

<table>
<thead>
<tr>
<th>stage</th>
<th>FU</th>
<th>DR</th>
<th>V</th>
<th>PC</th>
</tr>
</thead>
<tbody>
<tr>
<td>oldest</td>
<td>1</td>
<td>div</td>
<td>R1</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td></td>
<td></td>
<td>...</td>
</tr>
<tr>
<td>n</td>
<td>add</td>
<td>R2</td>
<td>1</td>
<td>1001</td>
</tr>
</tbody>
</table>

Reserve all stages for the duration of the instruction

Memory: Either stall stores at decode or use dummy store
Reorder Buffer

<table>
<thead>
<tr>
<th>st.</th>
<th>FU</th>
<th>V</th>
<th>tag</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>add</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>div</td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

Reorder Buffer

<table>
<thead>
<tr>
<th>tag</th>
<th>DR</th>
<th>Result</th>
<th>V</th>
<th>E</th>
<th>PC</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>r1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>r2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

• Out-of-order completion
• Commit: Write results to register file or memory
• Reorder buffer holds not yet committed state

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Reorder Buffer Complications

- State is kept in the reorder buffer
- May have to bypass from every entry
- Need to determine the latest write
- If read not at same stage need to determine closest earlier write

Two Solutions:
- History Buffer
- Future File
History Buffer

- Allow out-of-order register file updates
- At decode record current value of target register in reorder buffer entry.
- On commit: do nothing
- On exception: scan following reorder buffer entries restoring register values
Future File

- Two register files:
  - One updated out-of-order (FUTURE)
    - *assume no exceptions will occur*
  - One updated in order (ARCHITECTURAL)
- Advantage: No delay to restore state on exception