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FUJITSU'S SPARC64 V IS REAL DEAL

Fujitsu's design differs from HAL's version; faster than US III

By Kevin Krewell {10/21/02-01}

At **Microprocessor Forum 2002**, Fujitsu stepped forward to carry the banner for the fastest SPARC processor, surpassing Sun's fastest UltraSPARC III on clock frequency and SPEC performance. In fact, at 1.35GHz, the Fujitsu processor has the highest clock frequency of any 64-bit server processor now in production. This clock-speed advantage—plus large on-chip caches; a fast system-crossbar switch; and a four-issue, out-of-order core—translates into good SPEC benchmark performance for Fujitsu's SPARC64 V processor. The SPARC64 V is an evolutionary step in Fujitsu's SPARC processor line instead of the more-radical approach proposed three years ago by HAL Computer at Microprocessor Forum 1999. This latest version of Fujitsu's SPARC processor family, revealed by Fujitsu's director of Development Department (Processor Development Division) Aiichiro Inoue, is based on an enhanced version of the previous SPARC64 GP processor core, with larger caches and advanced semiconductor process technology. The SPARC64 GP includes many conservative, but quite effective, RISC superscalar design techniques. SPARC64 V is a fresh implementation of the microarchitecture with improved out-of-order operations and enhanced mainframe-class reliability.

The Fujitsu SPARC processor now offers a clock-speed advantage of nearly 30% over its cousin processor, the Sun UltraSPARC III (US III). The fastest US III now clocks in at 1.05GHz. The Fujitsu processor's performance scales well with the higher clock frequency, placing it in SPEC-benchmark competition with other leading 64-bit processors.

Fujitsu Technology Solutions was formed by the merger of Amdahl Computer and Fujitsu in April 2002. The SPARC processor developments date to 1995 and were often designed by a Fujitsu acquisition, HAL Computer. At Microprocessor Forum 1999, Mike Shebanow, then vice president and CTO of the HAL Computer Division of Fujitsu, proposed a complex and very wide superscalar version of the SPARC64 V processor, with an instruction trace cache, superspeculation, and split L2 cache (see *MPR 11/15/99-01*, "Hal Makes Sparcs Fly"). Mike's innovative chip never made it to market, but the trace-cache idea became a mainstream processor feature, shipping in Intel's Pentium 4 microarchitecture. The Pentium 4 also paralleled another of Mike's

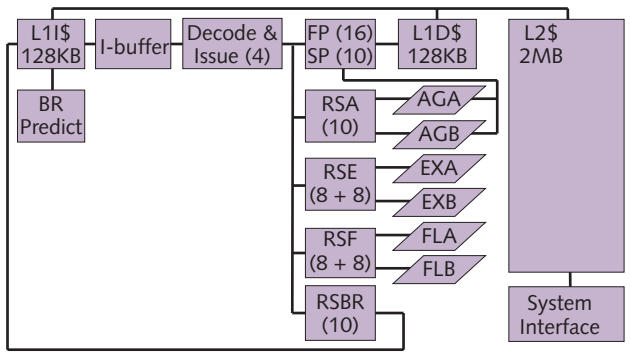

Figure 1. This figure shows a high-level block diagram of the SPARC64 V processor. The processor can decode and issue up to four instructions and execute up to six instructions in the out-of-order execution core. Noteworthy are the very large L1 and large L2 caches.

design choices for the SPARC processor, as Intel's design also specified a very small, but very fast 8K data cache. It now appears that the HAL design for the SPARC64 V disappeared with the division itself around mid-2001.

Fujitsu's design took a very different approach from HAL's on almost everything, including choices of L1 cache sizes. The Fujitsu SPARC64 V design, shown in Figure 1, uses conventional, but large, 128K L1 caches for both (totaling 256K of L1 cache). The instruction cache has a wide 32-byte instruction-fetch path. To keep the instruction-fetch path filled, the Fujitsu design uses speculative fetch logic with a sequential address generator. Fetched instructions are placed into a 192-byte I-buffer. The buffer can issue four instructions (16 bytes) to the reservation stations every cycle. This issue rate is the same as the sustained rate for Sun's UltraSPARC III (see *MPR 10/27/97-07*, "UltraSparc-3 Aims at MP Servers").

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Fujitsu's Aiichiro Inoue presents the SPARC64 V at MPF2002.

The rather large 128K data cache is dual ported and supports the five-cycle instruction- fetch sequence shown in Figure 2. This has always been an interesting processor design trade-off: the greater hit ratio of a large L1 cache versus the lower latency possible with a smaller cache.

HAL strove for lower latency at the price of cache size (and therefore cache hit rate). The HAL design had a very small 8K L1 data cache but with extremely quick access, and it was backed by a dedicated 512K L2 data cache. That design was unusual in splitting the L2 into separate data and instruction caches. The advantages of a split L2 cache, such as greater total L2 cache bandwidth, are often outweighed by the simplicity and flexibility of a unified cache, in which data and instructions are mixed. The Fujitsu processor supports the large L1s with a proportionately large (2M) unified L2 cache. The Fujitsu relies on the large-size caches, with higher hit rates, to reduce average memory-access delays without resorting to exotic designs.

The Sun UltraSPARC III design added an on-chip memory controller to reduce memory latency and provide aggregate memory bandwidth that would scale with the number of processors. The Fujitsu approach relies, in part, on a 128-bit-wide bus interface that can support double-data-rate operation, providing bandwidth that can exceed 16GB/s to main memory. The large 2M L2 cache, with a 256-bit bus to the L1 caches, also lowers average memory latency. The US III relies on an external L2 cache that can be as large as 8MB, but this cache lacks the latency and speed advantages of an on-die cache SRAM.

The SPARC-family register windowing is supported by eight register windows. The SPARC64 V has six main execution units, consisting of two address generators, two integer execution units, and two floating-point units. The address generators and integer execution units are shown in Figure 3. The joint window register (JWR) holds three windows: the current window, the last window, and the next window.

The SPEC benchmark results from the large L2 cache and higher clock frequency are significantly higher than those for the slower Sun UltraSPARC III and are reasonably competitive with other contemporary 64-bit processors. The SPEC2000_int base score of 747 is almost 40% higher than the score of the 1.05GHz US III (537). The Fujitsu score shows an 8% greater architectural performance over the US III core when nominalized for clock speed. The low-latency 2M L2 cache, out-of-order core, and fast system bus all contribute to the greater architectural efficiency of the Fujitsu design.

One strength of the SPARC64 V processor is its floating-point unit, shown in Figure 4. With up to two floating-point operations per cycle and with its higher clock frequency, the 1.35GHz SPARC64 V produces a good SPEC2000_fp base score of 935, 33% faster than the 1.05GHz US III. The Fujitsu chip shows an even greater advantage on the peak numbers, with a 46% increase (1,205 vs. 827). Although these numbers

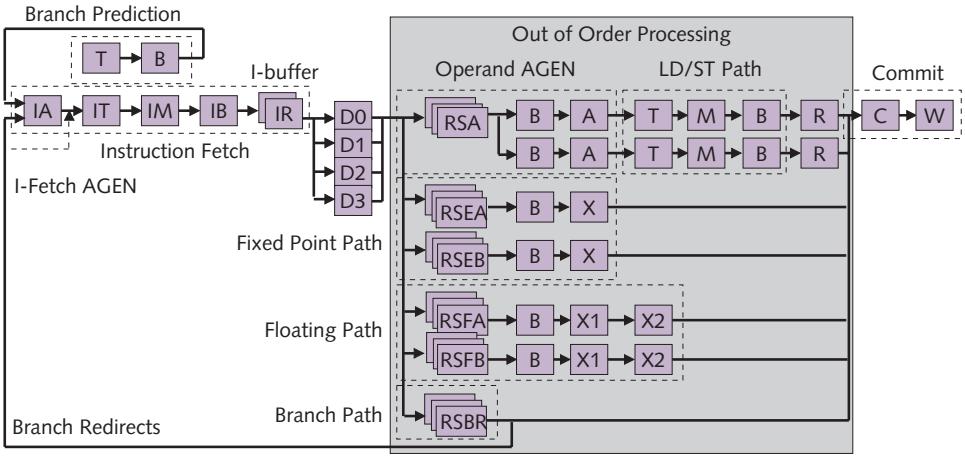

Figure 2. The SPARC64 V pipeline is nominally ten stages deep for integer operations if all the instruction-fetch stages (including IA) and the commit stage (not including the write-back stage) are included. The branch-mispredict penalty is six clock cycles for an unconditional branch and seven clock cycles for a conditional branch.

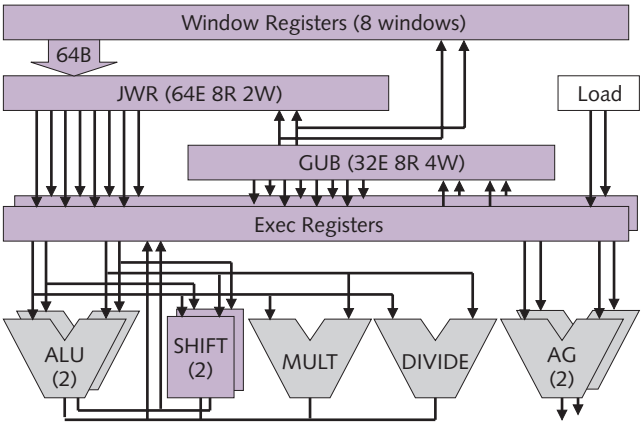

Figure 3. The fixed-point unit consists of the dual integer ALUs, dual shifters, a multiply unit, a divide unit, and two address generators. Up to four instructions per cycle can be issued to these units. The joint window register (JWR) holds the previous, current, and next windows.

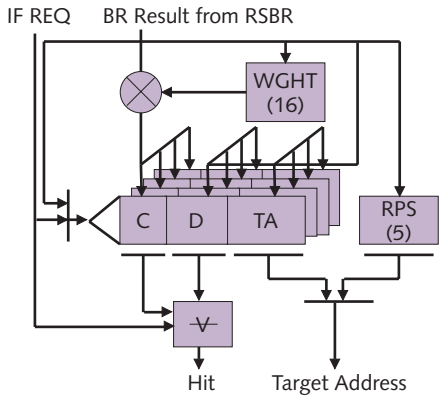

Figure 5. The branch-prediction logic is built around a large four-way, 16K-entry branch- history table. The write-cycle global history (WGHT) table tracks often-repeated branches. The return-prediction stack (RPS) provides return addresses for sub-routine calls.

are respectable, the SPARC64 V base score still lags behind the scores of the 1.3GHz Power4, the 1.25GHz Alpha EV68, and the 1GHz Itanium2. The peak score shows promise for future compiler improvements. With a new version of Fujitsu's Parallel-NAVI compiler in development, expect base scores soon that exceed 1,000.

The branch penalty is seven clock cycles for conditional branches (six cycles for unconditional branches), making good branch prediction essential. The branch-prediction unit, shown in Figure 5, is built around a four-way, 16K-entry history table. The table contains both the target address and outcome prediction. The write-cycle global history table (WGHT) is an awkwardly named table that tracks the deeper branch history of the 16 most-often-recurring branches. The WGHT holds the number of times the branch was taken and not taken. A five-entry return-prediction stack helps provide the return addresses for subroutine calls. The large table provides fast target-address prediction at the cost of large SRAM arrays.

The SPARC64 V is built in 0.13 micron, with eight-layer copper interconnect from an unnamed foundry; it is shipping now at 1.35GHz in PRIMEPOWER servers. The processor, shown in Figure 6, consists of 191 million transistors, most of which are in the caches. At about 50W at 1.35GHz, this is a very power-friendly processor that could be used in relatively dense designs. The on-die L2 cache allows the SPARC64 V to reduce the number of signal pins to only 269. The die size is 18.1mm x 16.0mm (289.6mm^2), larger than the US III (210mm^2).

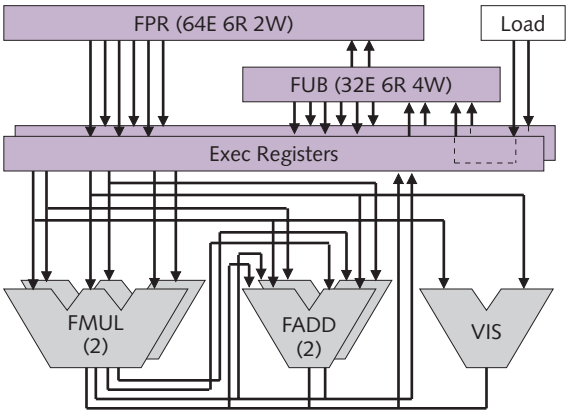

Figure 4. The floating-point execution unit supports up to two operations per cycle. The floating-point register (FPR) has 64 entries and supports six read ports and two write ports. The FPR update buffer (FUB) has 32 entries and supports six read ports and four write ports. The SPARC64 V also has a unit that supports VIS instructions.

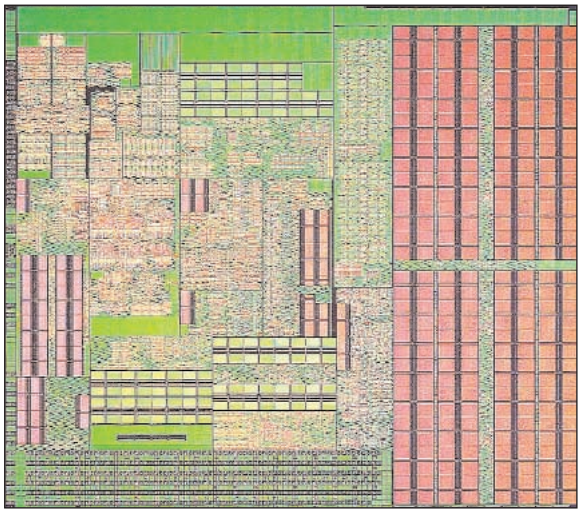

Figure 6. The die plot of the SPARC64 V. The processor is built in a 0.13-micron process with eight copper interconnect layers. The die size is 18.1mm x 16.0mm. Fujitsu specifies power at about 50W at 1.35GHz with a 1.2V core.

Price & Availability

Fujitsu has commenced shipments of PRIMEPOWER systems using the new SPARC64 V processors at 1.35GHz. Those systems include the PRIMEPOWER 900, 1500, and 2500 systems that can respectively support up to 16, 32, and 128 processors. Additional information on the PRIMEPOWER servers can be found at: *www.ftsi.fujitsu.com/services/products/primepower/index.html*

With much smaller caches, the HAL design concept had only 65 million transistors, but it would have required 380mm^2 of silicon in Fujitsu's 0.17-micron six-layer-copper CS85 process. Obviously, it didn't make it to production. The reasonable die size of the SPARC64 V makes it quite manufacturable, and with only 269 signal pins and a 50W power envelope, it eases system design.

Putting Mainframe Thinking Inside the Box

To connect multiple processors together, Fujitsu uses a dual-crossbar switch configuration. With up to eight processors per system board, the system design allows scalability up to 128 processors (PRIMEPOWER 2500). The relatively low power of the SPARC64 V processor allows Fujitsu flexibility in packing many processors together. Lower power consumption also contributes to more-reliable semiconductor operation.

The crossbar interface runs at 540MHz, using source-synchronous clocking, a technique also used in the EV6 Alpha processor. The crossbar is constructed in two sections to provide redundancy. The crossbar is also used as part of Fujitsu's Extended Partitioning (XPAR) feature, which allows the hardware isolation of processor clusters on a system board. On the PRIMEPOWER 2500 system, with up to eight processors on a system board, there are two XPAR partitions per system board.

The Fujitsu servers are targeted at the mainframe market and need mainframe-class reliability, availability, and serviceability (RAS). To guarantee datapath integrity, Fujitsu has parity-protected CPU registers, internal datapaths, and execution units. The data-cache and tag arrays and the translation lookaside buffer (TLB) have parity or ECC protection. The processor also provides automatic recovery through instruction retry for intermittent errors. Degraded functionality is provided when there are cache or TLB problems (a limp-along mode). Error information is accumulated in the background during system operation and is used to monitor the health of the server.

The SPARC64 V offers a faster alternative to Sun's UltraSPARC III while maintaining software compatibility with the SPARC V9 and JPS specs. It would have been interesting to see how the HAL Computer design performed, but it apparently fell victim to the complexities of its ambitious design. In this case, the more conservative approach of taking an existing good core, adding additional on-chip memory, and implementing it in a contemporary semiconductor process can produce a competitive processor. Sun may call its SPARC processor "Ultra," but Fujitsu's version is just plain faster.