Microarquiteturas de Alto Desempenho

MIPS R10000

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R10000 Memory Hierarchy

Parallelism in Data Cache
Data Cache Interleaving

CPU accesses one doubleword. Simultaneous tag check selects way.

External Interface accesses quadword as two doublewords in parallel.

System Configurations

Secondary Cache
512K to 1MB dynamic DRAM
2-way set associative

R10000

Display/Bus

System Interface Bus
- 16-bit external address
- 28-bit external data
- 20-bit external address with parity
- 32-bit internal address bus with 8-bit ECC
- 64-bit external address with parity
- 32-bit external data bus with parity
- Cache Datar 1, 1.5, 2, 2.5, 3, 3.5, 4 supported
System Interface Block Diagram

R10000 Die Photo

This sheet shows physical placement of major blocks.
(Full color photo slide will be shown at Red Chips.)