Parallelized Analytic Placer

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Introduction

- Analytic Placement is a CAD algorithm for ASIC placement
- Takes arbitrary circuit netlist and finds physical location of each element
- Attempt to minimize wire-length, maximize performance
Introduction

- Each block treated as a physical element
- Each interconnect treated as a spring that exerts force
Introduction

- Algorithm creates a set of force equations for each node

\[ F_j = \sum_{i=1}^{N} k_{ij} (x_j - x_i) \]
Introduction

- Steady state location found when net forces are 0
- Creates a system of linear equations
- Solving X matrix gives position of all elements

\[
\begin{bmatrix}
  k_{11} & \cdots & k_{iN} \\
  \vdots & \ddots & \vdots \\
  k_{N1} & \cdots & k_{NN}
\end{bmatrix}
\begin{bmatrix}
  x_1 \\
  \vdots \\
  x_N
\end{bmatrix} = 0
\]
Introduction
Parallelization

- Uses Gaussian Elimination to compute X and Y coordinate matrices
- Gaussian Elimination is composed of two stages, and each stage is parallelized independently
  - Upper-Triangular Reduction
  - Back-Substitution
Parallelizing Upper-Triangular Reduction

- Perform row elimination on entire bottom right corner of the pivot at once
  - Iterate only number of row times
  - Reduced the number of threads spawned by ignoring left side of pivot

- Augmented A, xB and yB matrices
  - The same row operation is performed on all three matrices
  - Reduced number of row elimination calls
Parallelizing Back-Substitution

- Improved efficiency by decoupling dependency between rows
  - Original (serial) algorithm computes final result for one row by another
  - Compute partial results for entire rows at once for efficiency
- Minimized the number of threads spawned by ignoring zero columns
Measurements (First Cut)
Measurements (First Cut)

![Graph showing speedup vs netlist size in blocks]
No row swaps necessary

- Row swapping only required if pivot entry is missing
- This only happens if net-lists form a disjoint subgraph
- This never happens, so row swapping unnecessary
Measurements (No row swapping)
Measurements (No row swapping)
Future Work

- Further coalesce global memory accesses
  - Access patterns already fairly coalesced
- Take advantage of shared memory
  - Possibly caching pivot value