

ECE-451: VLSI Systems and Design

This course provides an introduction to the design and implementation of VLSI circuits for complex digital systems. The focus is on CMOS technology. Issues to be covered include deep submicron design, clocking, power dissipation, CAD tools and algorithms, simulation, verification, testing, and design methodology. The course includes a laboratory component in which you will design and layout a small 4-bit microprocessor.

Course Outline

Lecture	Reading	Assignments
01. Introduction	Notes	Lab0 out (1 wk)
02. CMOS Circuits Basics	Rabaey Ch. 1, insert A, 5.2, 6.2	
03. Layout	Rabaey Ch. 1, insert A, 5.2, 6.2	
04. Overview of Lab Projects	N/A	Lab1 out (1 wk)
05. Pass-Transistors and Transmission Gates	Rabaey 6.2, 7.1, 7.5, 10.3	
06. System Timing, Memory Elements	Rabaey 6.2, 7.1, 7.5, 10.3	
07. Memory Elements	Rabaey 6.2, 7.1, 7.5, 10.3	Lab2 out (3 wks)
08. Dynamic CMOS	Rabaey 7.2, 7.3, 6.3	Hwk1 out (1 wk)
09. IC Fabrication, Design rules	Rabaey 2.2, 2.3	
10. MOSFET Operation	Rabaey 3.3, 4.3	
11. Capacitance in MOSFET Circuits	Rabaey 3.3, 4.3	
12. Resistance, Switching, Delay	Rabaey 4.3, 5.4	
13. Delay Estimation, Gate Sizing	Rabaey 4.4, 5.4, 6.2	
14. Physical Design	Rabaey 3.3, 8.4, insert D, notes	
15. Adders	Rabaey 11.3	
16. Adders and Related Functions	Rabaey 11.3	Lab3 out (3 wks)
17. Multipliers, Counters	Rabaey 11.4, 11.6, notes	
18. PLAs and FSMs	Rabaey 12.6, notes	
[Reading Week, Feb. 20–24]		
19. Semiconductor Memory	Rabaey 12.2, 12.3	
• Midterm Exam (covers lectures 1–17) (Feb. 29, 2–4pm, in UC-266 and UC-273)		
20. Reliability, Latchup, Power	Rabaey 5.5, notes	Lab4 out (2 wks)
21. Faults and Testing	Rabaey insert H, notes	
22. Testing and Design for Testability	Rabaey insert H, notes	
23. Scan Design and BIST	Rabaey insert H, Abramovici 10.6	
24. LFSR	Abramovici 10.6	
25. Design Methodology and Design Styles	Rabaey 8.3, 8.4, 8.5	
26. Introduction to CAD	Rabaey insert C, notes	Lab5 out (2 wks)
27. Logic Synthesis	Rabaey insert F, notes	Hwk2 out (1 wk)
28. Placement, Floorplanning	Rubin 4.3.2, Preas Ch. 4	
29. Global and Detailed Routing	Rubin 4.3.1, Ullman 9.5, Preas Ch. 5	
30. Architectural Synthesis	De Michelli Ch. 4–6, notes	Hwk3 out (1 wk)
31. Layout Representation, Extraction	Ullman 9.1–9.2, Rubin 3.6, 5.1–5.6, Preas 8.1–8.7	
32. Design Rule Checking	Ullman 9.3, Rubin 3.6, 5.1–5.6, Preas 8.1–8.7	Lab6 out (1 wk)
33. Fault Simulation	Breuer & Friedman, Chap. 4	
34. Logic Simulation	Breuer & Friedman, Chap. 4	
35. Circuit Simulation	Ullman 9.4, notes	
36. Switch-Level Simulation	Ullman 9.4, notes	
• Final Exam, date and time to be announced later (covers all course material).		

• **Text (recommended, not required):** J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits - A Design Perspective*, 2nd Edition, Prentice-Hall, 2003.

• **Class notes:** Copies of all lecture transparencies are available as a book of class notes that you can purchase at any time from the ECE copy center in SF-B540. You are highly encouraged to do this.

General Course Information

- Instructor: Farid N. Najm, SF-1024, (416) 946-5175, f.najm@utoronto.ca, www.eecg.utoronto.ca/~najm
- Course Home Page: - use the BlackBoard system -
- Lab Location: GB-251 (ECE Unix Lab) is available exclusively during your assigned lab hours. You can also use GB-243 to run the design tools at any time, but this is an “open lab,” available to others as well.

Laboratory Work

This course has a computer laboratory component, consisting of one lab tutorial (Lab0) and six lab assignments (Labs 1–6). You will work in teams of two, and you will carry out VLSI subsystem and chip design using the Micromagic, Cadence, and Synopsys CAD tools available on the ECE Unix machines. Lab0 will serve as a tutorial to acquaint you with the Micromagic design system. In Lab1, you will design and layout a CMOS adder circuit. In Lab2–5, you will design and layout a CMOS 4-bit microprocessor, the AMD 2901. You will complete the datapath in Lab2 & Lab3 using a custom design approach. The control logic will be designed in Lab4 using a standard-cell design approach, using the Synopsys Design Analyzer for logic synthesis. In Lab5, Cadence First Encounter will be used for placing and routing the synthesized control logic and finally connecting the control logic to the datapath to complete the design. In Lab6, you will perform static timing analysis to verify the performance (speed) of your design.

Marks and Exams

The final course mark is based on your performance on the mid-term exam (20%), the final exam (40%), and the lab work + homework (40%). Note that Lab0 will not be marked, but you are required to do it and to turn in the results. All exams in the course will be open-book/open-notes, and you may use any type of calculator. The complete break-down of your course mark will be as follows:

Homework (3)	6%
Mid-term exam	20%
Final exam	40%
Labs (6)	34%
Lab1 (4%), Lab2 (9%), Lab3 (6%), Lab4 (6%), Lab5 (6%), Lab6 (3%)	

Penalty

Assignments should be handed in *at the beginning of class* on the scheduled due date. Penalty for late submission of homework and lab work is 5% per day (maximum 25%). Submissions more than 5 days late will not be accepted. To turn in an assignment at other than the scheduled time, you should hand-deliver it to the instructor, who will date and initial it.

Additional (optional) Reference Reading

- [1] Weste and Harris, *CMOS VLSI Design*, 4th Edition, Addison-Wesley, 2011.
- [2] Weste and Eshraghian, *Principles of CMOS VLSI Design*, 2nd Edition, Addison-Wesley, 1993.
- [3] D. Harris, *Skew-Tolerant Circuit Design*, Morgan Kaufmann, 2000.
- [4] G. DeMicheli, *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994.
- [5] G. D. Hachtel and F. Somenzi, *Logic Synthesis and Verification Algorithms*, Kluwer, 1996.
- [6] N. Sherwani, *Algorithms for VLSI Physical Design Automation*, 3rd Edition, Kluwer, 1999.
- [7] Mead and Conway, *Introduction to VLSI Systems*, Addison-Wesley, 1980.
- [8] B. Preas & M. Lorenzetti, *Physical, Design Automation of VLSI Systems*, Benjamin-Cummings, 1987.
- [9] S. M. Rubin, *Computer Aids for VLSI Design*, Addison-Wesley, 1987.
- [10] J. D. Ullman, *Computational Aspects of VLSI*, Computer Science Press, 1983.
- [11] Breuer and Friedman, *Diagnosis & Reliable Design of Digital Systems*, Computer Science Press, 1976.
- [12] M. Abramovici, M. A. Breuer, and A. D. Friedman, *Digital Systems Testing and Testable Design*, IEEE Press, 1990.
- [13] F. N. Najm, *Circuit Simulation*, John Wiley & Sons, 2010.