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Novel physics-based tool-prototype for electromigration assessment in commercial-grade power delivery networks

Running title: EM assessment in power delivery networks

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A recently developed novel methodology for electromigration (EM) failure assessment in power/ground grids of integrated circuits is employed in the EDA tool-prototype. The tool performs analysis of stress evolution in interconnect trees for detecting EM-induced voiding locations and tracks resistance increase of the voided wires based on a physics-based model of voiding kinetics. Increased resistances of the branches of power/ground networks lead to a voltage drop increase in grid nodes. The instance in time when a designer-specified voltage-drop threshold is reached defines the EM induced time-to-failure (TTF). Monte-Carlo (MC) simulation, performed around the core engine that simulates the stress over time using randomly-generated atomic diffusivities and critical stress values, leads to the mean-time-to-failure (MTTF) of the grid, along with voiding probabilities of the interconnect branches.

I. INTRODUCTION

Due to technology scaling, the continuous reduction in interconnect critical dimensions, which is accompanied by increased current densities in metal lines, has led to a situation where it is very difficult to achieve EM sign-off using traditional methods. Two main drawbacks of the existing approach of designing EM-immune on-chip power/ground (p/g) grids were pointed out recently[1]. The first has to do with the fact that individual metal lines are treated separately, and in isolation, using Blech-Black empirical relations. However, interconnect wires in each layer of metallization connected by underlying vias in dual-damascene technology lead to a p/g grid architecture represented by so-called interconnect trees[1,2]. These continuously-connected highly conductive metal segments terminated by diffusion barriers allow atomic transport between segments, so that an analysis of the grid based on individual isolated segments is highly unrealistic. The absence of diffusion barriers at one or both ends of a metal branch prevents the accumulation/depletion of atoms at the branch ends, which makes the traditional approach to EM assessment groundless. The second issue is related to the currently accepted grid failure criteria, which defines the TTF of the whole grid as the instance in time when any interconnect branch fails due to EM-induced voiding. However, modern power grids use a mesh structure, so that there are many paths for current to flow from the flip-chip bumps to the underlying logic, a characteristic which is referred to as a redundancy. As such, it is highly pessimistic to assume that a single branch failure will always cause the whole grid to fail.

Both drawbacks result in overdesign of the grid, and can make the chip performance worse. An efficient assessment of EM failure time of p/g networks must verify the ability of nets to provide reliable voltage delivery to operational units during

the intended chip lifetime. This target was achieved in the recently developed novel methodology[1], which computes the p/g IR-drop degradation based on analysis of the EM-induced voiding of interconnect wires, while accounting for the redundancy of voltage delivery paths in the network. EM induced failures in power nets (usually called VDD) and in ground nets (VSS) can be treated independently. The TTF of each net is computed as the time when voltage variations, which are decreases in VDD or increases in VSS, reach a designer specified threshold, say 10% of the supply voltage. The tool-prototype presented in this paper was developed based on this simulation methodology and optimized for EM assessment in large p/g grids of commercial chips.

Interconnect trees are characterized by the number of branches, branch sizes, as well as current densities and current directions in each branch. Because the EM-induced stress in a metal line depends on the topology of the whole interconnect tree, which can be arbitrary, it is not possible to come out with simple lookup table-like EM design rules for general interconnect trees. Therefore, EM analysis should employ the physical models of stress build-up caused by the electric current driven atomic transfer. This stress evolution can be described by Korhonen's model[3], which allows to calculate an instant in time t_{nucl}, when the tensile stress near cathode end of any branch of interconnect tree achieves a critical value σ_{crit}, required for metal voiding. Voiding changes the existing stress distribution. The zero normal stress component at the void surface is responsible for atomic transfer from the void surface into the metal bulk, which governs the post-voiding stress and therefore the void shape and size evolution.

The rate of void growth is an important factor, which regulates the resistance increase of voided segments. Large stress gradient near the void surface drives the

surface atoms into the metal bulk, thus enlarging the void and reducing tensile stress in the surrounding metal. If the void spans the wire cross-section, the electric current continues to flow through the thin high-resistance barrier layer that encapsulates the copper wire. When the void length is large enough to cause a significant increase of the wire's resistance, a notable change in voltage drop is observed. The combination of the void nucleation time and the time of void growth, which results in, say 20% increase of line resistance depends on the applied current density, temperature and residual stress, as it was shown in experiments for extracting the MTTF of the standard single link metal-via structures[4]. Physics based simulations provide these times in a self-consistent way. The EM assessment methodology enhanced by accounting for the void evolution kinetics in MTTF calculation, which was ignored previously[1], is demonstrated in this paper.

Our EM assessment methodology employs the 1-D Korhonen's equation for calculating the stress evolution[3] and voiding dynamics[5] in each interconnect tree. In the framework of a 1-D approximation where voids occupy the whole wire cross-section, only void length can be calculated. The one-dimensional approximation enables the analysis of a large number of interconnect trees in the p/g grid. The finite difference method (FDM) employed for numerical solution of a system of stress equations allows fast and accurate EM analysis in p/g grids of large commercial chips[1]. The random nature of EM degradation, caused by random distribution of atomic diffusivity in different branches and randomly varying critical stresses in grid nodes, is accounted for by using (MC) simulation. It allows us to simulate a sequence of grid TTFs, which eventually converge to the desired MTTF.

II. EM MODEL IN INTERCONNECT TREES

The EM model is based on the concept of divergence of atomic transport, caused by electron wind force, and the hydrostatic stress gradients in the confined metal. Atomic flux is described by the expression

$$\Gamma = \frac{D_a}{\Omega k_B T}\left(\Omega \frac{\partial \sigma}{\partial x} - q^* \rho j\right). \quad (1)$$

Here, D_a is the effective atomic diffusivity, q^* is the effective charge of migrating atoms, Ω is the atomic lattice volume, ρ is the metal resistivity, j is the current density, k_B is the Boltzmann constant, T is the temperature, and σ is the hydrostatic stress. The flux divergence caused by the coordinate dependent stress gradient and exacerbated by spatial variation in atomic diffusivity is responsible for a volumetric dilatation θ:

$$\frac{\partial \theta}{\partial t} = \Omega \frac{\partial \Gamma}{\partial x} \quad (2)$$

which generates the hydrostatic stress through the interaction with the rigid confinement. A diffusion type equation for the evolution of stress $\sigma = B\theta$, where B is the effective bulk modulus, has been proposed by Korhonen[3]:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\kappa\left(\frac{q^* \rho j}{\Omega} - \frac{\partial \sigma}{\partial x}\right) \quad (3)$$

where $\kappa = D_a B \Omega / k_B T$.

When equation (3) is employed for analysis of the stress build up in an interconnect tree, the corresponding boundary conditions (BC) should be defined at the terminal nodes representing diffusion barriers and at internal nodes, which are the junctions between neighboring branches. An example of an interconnect tree in the lowest metal layer, which is a part of the VDD network of a test design, is shown in

Fig.1. It consists of a long horizontal power rail and short vertical branches, which provide connections to operational cells.

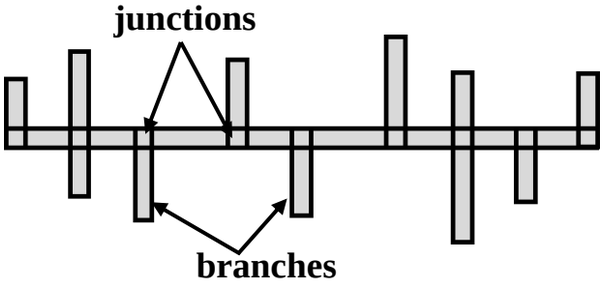


Fig. 1. Schematics of interconnect tree in M1 layer of the test design.

For EM analysis, the tree is considered as an oriented graph, consisting of nodes, which are wire junctions, and branches, which are the sections of wires between nodes. Nodes are electrically connected to interlayer vias. The value and direction of electric current in each branch is defined by the node voltages. Therefore, equation (3) should be applied to each branch, and internal boundary conditions are defined by continuity of the atomic flux (1) and stress. For the i-th node, the mass conservation law yields[2]:

$$\sum_k w_{ik}\kappa_{ij}\left(\frac{\partial\sigma_{ik}}{\partial x}\Big|_{x=x_i} - \frac{q^*\rho j}{\Omega}\right) = 0 \qquad (4)$$

where the indices ik denote k-th branch connected to i-th node; w_{ik} is the k-th branch width (note that all branches in a tree are in the same metal layer hence have the same thickness). Wire-to-wire variation of the parameter $\kappa = D_a B\Omega/k_B T$ caused by the random distribution of atomic diffusivity is governed by the variation of metal microstructure.

For the terminal nodes (with coordinates $x = x_t$) which have only one connected branch, the condition (4) is reduced to

$$\left.\frac{\partial \sigma_k}{\partial x}\right|_{x=x_t} - \frac{q^* \rho j}{\Omega} = 0 \qquad (5)$$

This equation describes blocking boundaries, where the flux vanishes, since diffusion barriers (e.g. TaN or TiN liners) prevent diffusion of atoms. Existence of these boundaries results in atomic accumulation/depletion at interconnect wire ends and causes stress build-up there. Thus, equations (3)-(5) form an initial value boundary problem (IVBP), which describes stress evolution in the tree and allows one to find the instance in time when stress achieves a critical value σ_{crit} required for void formation.

We accept that a defect in metal can be transformed into a void, when the tensile stress achieves some critical value. According to thermodynamics of void nucleation process[6], critical stress is defined by the defect size a: $\sigma_{crit} = 2\gamma/a$, where $\gamma \sim 1\ J/m^2$ is the energy per area of void surface. Assuming a defect size of ~10 nm, critical stress value is obtained: $\sigma_{crit} = 500\ MPa$. However, we take into account a random distribution of defect sizes for statistical analysis of EM failure, as it is described in Section IV.

Equation (5) is the basis for steady state analysis providing a stress σ_{SS} distribution, which is achieved when atomic flux vanishes in any point of the metal due to balance of EM and stress gradient induced fluxes. For each branch it gives:

$$\sigma_{ss}^{i,\ cathode} - \sigma_{ss}^{i,\ anode} = \frac{q^* \rho (j_i L_i)}{\Omega} \qquad (6)$$

where L_i is the length of the i-th branch. For finding the steady-state stress values for all nodes of a tree, the atomic conservation condition should be added to the set of equations (6)[2]:

$$\sum \left(\sigma_{ss}^{i} - \left[\sigma_{res} + \frac{eZ^* \rho (j_i L_i)}{2\Omega} \right] \right) L_i = 0 \qquad (7)$$

where σ_{res} is the average value of residual stresses in the tree. Equations (6) and (7) represent an extension of Blech's law for interconnect trees, and allow one to define EM-immune trees: if σ_{SS} doesn't exceed the critical stress σ_{crit} in any junction, the tree can be considered as immortal.

III. POST-VOIDING STRESS EVOLUTION AND VOID GROWTH

The formulated IVBP (3)-(5) is valid while the stress in any node does not exceed the critical value σ_{crit}. When σ_{crit} is achieved, the node boundary conditions is changed due to the emergence of the void free surface. The large stress gradient formed near the void causes migration of atoms located at the void surface into the metal bulk, which results in an increase of the void size and reduction of the tensile stress. This stress gradient near the void surface ($x = x_s$) can be found by introducing an effective thickness of the void interfacial layer δ[5],

$$\left.\frac{\partial\sigma(t)}{\partial x}\right|_{x=x_s} = \frac{\sigma(t)}{\delta} \qquad (8)$$

For a single wire, an analytical solution of (3) with BC (5) at the anode node and (8) at the void edge results the stress relaxation kinetics, which yields a linear stress distribution with zero stress at the via edge in the steady state limit[5].

In the one-dimensional case under consideration, where a void spans the entire wire cross-section, the void growth accompanied by tensile stress relaxation is described as[2]

$$l_v = -\frac{1}{B}\int_0^L \sigma(x,t)dx \qquad (9)$$

where $l_v(t)$ is the time-dependent void length.

Post-voiding stress evolution in interconnect trees is described by the same equations (3)-(5), but the BC at the voided nodes must be replaced by (8). In the multi-voiding case when several voids are nucleated in the same tree, equation (9) describes the total length of all voids. A separate growth kinetics of each void can be derived by calculating atomic fluxes from each void to the metal bulk. Thus, the growth rate of each void can be defined as

$$v = \Omega\Gamma(x_s) = \frac{D_a\Omega}{kT}\left(\frac{\partial\sigma}{\partial x}\Big|_{x=x_s} - \frac{q^*\rho}{\Omega}j\right) \qquad (10)$$

Simulation of the stress evolution based on equations (3)-(5) and (8) and void length evolution based on (10) are used for analysis of EM-induced voltage drop increase in p/g grid, as described in the next section.

IV. NUMERIC ANALYSIS AND EM ASSESSMENT FLOW

Numerical integration of Korhonen's equation (3) is performed using the finite difference method[1]. Each branch is uniformly discretized into *N* equal segments, and the spatial partial derivatives are approximated using the central difference formula. Backward differentiation formula is employed for the time derivative. Taking into account that the current density *j* is constant within each branch, we get:

$$\frac{\sigma(x,t+\Delta t)-\sigma(x,t)}{\Delta t} = \kappa\frac{\sigma(x+\Delta x,t)+\sigma(x-\Delta x,t)-2\sigma(x,t)}{(\Delta x)^2} \qquad (11)$$

where $\Delta x = L/N$, and Δt is the time step. The boundary conditions (4) and (5) are used to get proper transformation of the right-hand side of (11) at nodes, as described in details in[1]. For a tree with a number of branches B, the discretization scheme (11) results in a set of $(NB + 1)$ linear equations, which must be solved on each time-step.

In the employed methodology, each branch of the tree is characterized by its own constant diffusivity, thus only tree nodes, which are the branch junctions, represent sites of the possible flux divergence leading to tension build up and void nucleating. If void is nucleated, the increment in its length during each time step is defined by means of (10): $\Delta l = v\Delta t$. In the finite-difference approach, the stress gradient near the void surface can be calculated by an extrapolation formula that involves the stress value near the surface, σ_0, and the stresses in two neighboring grid points, σ_1 and σ_2:

$$\Delta l_v = \frac{D\Omega}{kT}\left(\frac{-3\sigma_0 + 4\sigma_1 - \sigma_2}{2\Delta x} - \frac{q^*\rho}{\Omega} j\right)\Delta t \qquad (12)$$

A check of the resistance growth of voided branches for all trees, and calculation of consequent increase of voltage drop in grid nodes are performed periodically with a time step T. Since the electric current in the voided branch flows through the liners (diffusion barriers), the resistance change depends on the liner resistivity ρ_{liner}, and cross-sectional area S_{liner}:

$$\Delta R(t) = \left(\frac{\rho_{liner}}{S_{liner}} - \frac{\rho_{Cu}}{S_{Cu}}\right) l_v(t) \qquad (13)$$

Figure 2 demonstrates the simulation flow employed in the tool-prototype, which was developed for performing the p/g grid EM assessment, MTTF estimation and predicting the probability of voiding in different branches. As an input, the tool accepts a netlist of resistors and voltages in all nodes of the grid, provided by a power analysis tool.

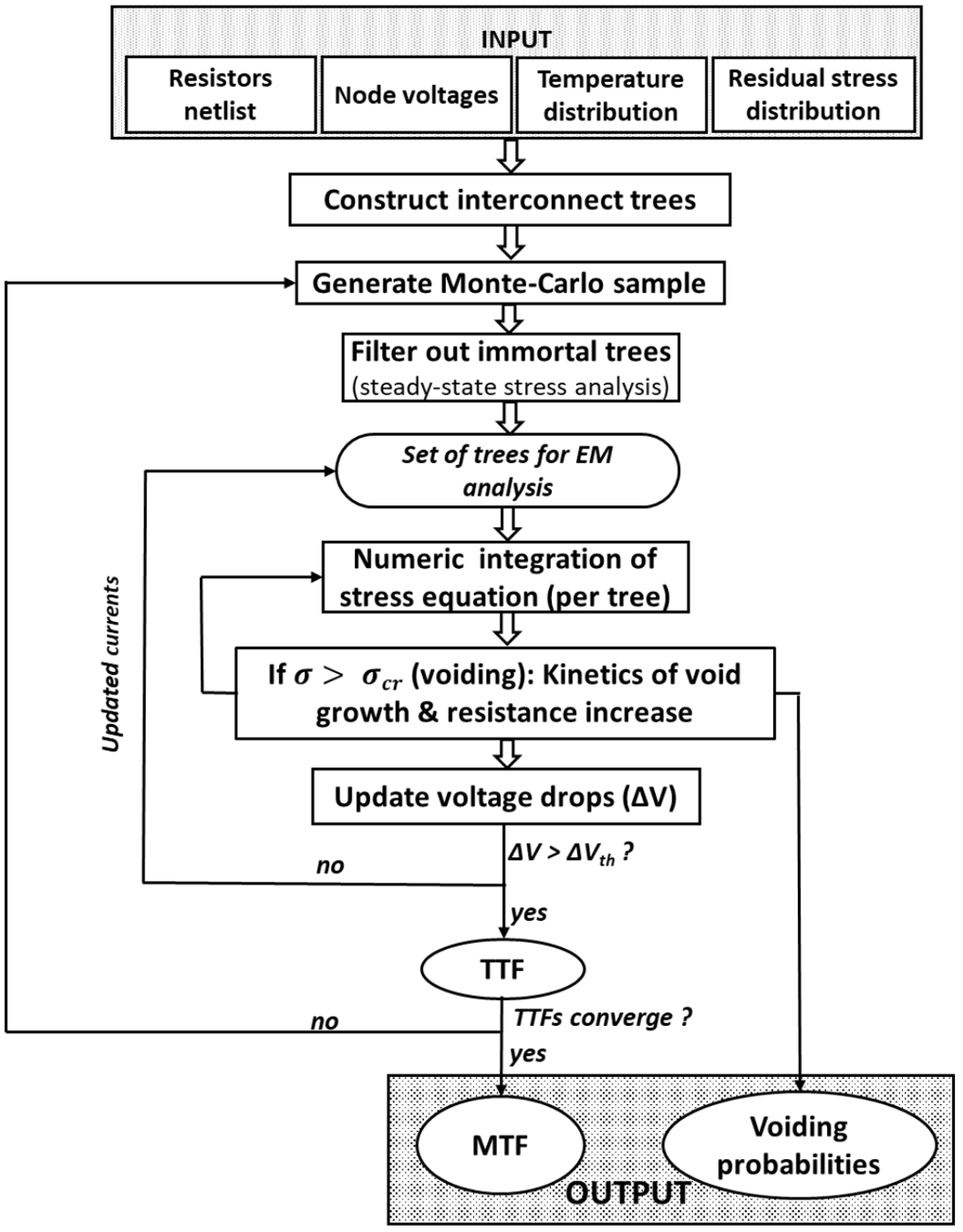


Fig. 2. Schematics of the tool flow.

Temperature and residual stress distributions can be used by the tool for more accurate analysis. For this propose, EM assessment flow is linked with existing

simulation capabilities for extraction temperature and stress caused by chip-package interaction in the chip interconnects[7]. The residual stress $\sigma_{res}(x, y)$ represents an initial level for further stress evolution: development of the stress $(\sigma_{crit} - \sigma_{res})$ due to EM is required for a void formation.

Based on the netlist, the tool constructs interconnect trees. Each tree is located within one metal layer, which allows for parallel processing of the interconnect layers. Calculation of current densities in the branches of the trees is performed using the input node voltages, cross-sectional areas of the branches, and reference direction prescribed to each tree.

For statistical analysis of EM failure, simulations of stress evolution and voiding should take into account variations of atomic diffusivity and critical stress values across the interconnect trees, which are caused by randomness in metal texture and defects size distribution in the wires. The effective diffusivity D_a which is employed in Korhonen's equation (3), includes atomic diffusion in metal bulk, in grain boundaries (GB), and along interfaces (IF). Since the bulk diffusivity is much smaller than the other two, the effective diffusivity can be expressed as

$$D_a = (1 - f_c) D_a^{IF} \frac{\delta^{IF}}{h} + f_c D_a^{GB} \frac{\delta^{GB}}{d}$$

where δ^{IF} and δ^{GB} describe correspondingly the widths of the interface and the grain boundary, d is the grain size, and h is the line thickness. The parameter f_c is the average length fraction of the cluster segment (the section composed of poly-crystalline grains), which represents the relative contribution of GB and interface diffusion to overall drift velocity for a Cu interconnect line[6]. Since the grain size distributions follow the lognormal distribution[8], it is also valid for the distribution of the diffusivity. This

effective diffusivity is described by thermal activation mechanism, $D_a = D_0 \exp(-E_a/k_B T)$. In our simulations D_0 is assumed to be a constant, and the effective activation energy E_a is considered as a random quantity. We consider normal distribution of E_a, which results in lognormal distribution of D_a:

$$f(E_a) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{1}{2}\left(\frac{E_a - E_a^m}{\sigma}\right)^2\right) \quad (14)$$

where E_a^m is the mean value of activation energy, and σ is the variance. Simulations employed the parameters values $E_a^m = 10^{-19} J$, $\sigma = 1.5 \cdot 10^{-19} J$, $D_0 = 10^{-4}\, m^2/s$.

The random distribution of critical stress is caused by its inverse proportionality to the precursor size *a*, as it has been discussed in Section II. We choose Weibull distribution for characterization of σ_{crit}, which reflects low probability of appearance of large defects, resulting in low probability of small critical stress values:

$$f(\sigma_{crit}) = \frac{\beta}{\eta}\left(\frac{\sigma_{crit} - \mu}{\eta}\right)^{\beta-1} \exp\left(-\left(\frac{\sigma_{crit} - \mu}{\eta}\right)^{\beta}\right) \quad (15)$$

The parameters of Weibull function $\beta = 2.25$, $\eta = 1.08$, and $\mu = 5.2 \cdot 10^8$ where used in simulations, providing mean value of critical stress of ~500 MPa and variance ~100MPa.

The statistical EM analysis is performed by means of MC simulations, as it is described in flowchart of Fig. 2. Generation of a MC sample implies prescription of E_a value to each branch, and σ_{crit} value to each junction of all interconnect trees, based on equations (14) and (15) correspondingly.

Before performing a time-dependent analysis of the stress evolution, the tool performs fast analysis of the steady-state stress σ_{ss} in the junctions of all trees, based on equations (6) and (7). If a tree meets the condition: $\max(\sigma_{ss}) < \sigma_{crit}$, then it is immortal, and isn't a subject for further analysis. The efficiency of this steady-state

filtering procedure can be seen by the results obtained on a typical VDD net of a commercial design, consisting of $1.25 \cdot 10^7$ resistors. This net is denoted as "Grid2" in Table1. The total number of interconnect trees was $2.78 \cdot 10^6$. After steady-state filtering, the number of "suspicious" trees, which were subject of further detailed analysis, was reduced to $8 \cdot 10^5$. Hence, we get almost 70% reduction of the number of trees to be analyzed, substantially decreasing the runtime, and providing the possibility of overnight analysis of very large designs.

For the set of trees which remains after the filtering procedure, accurate numerical integration of the stress equation (11) is performed, Fig. 2. Evolution of the stress distribution in an interconnect tree, found while accounting for temperature and residual stress variations, allows us to determine the void nucleation sites and a sequence of void nucleation times.

The resistance increase of a voided branch is obtained from equations (12) and (13). This resistance evolution is accompanied by a redistribution of the electric current within interconnect trees and between trees. The resulted change of grid node voltages are computed using the CHOLMOD solver[9]. If the voltage drop at any node of the analyzed grid exceeds a user-specified threshold value, ΔV_{th}, the instant in time when it is happened is reported as TTF.

Results shown in Fig. 3 demonstrate the effect of redundancy in the p/g network on the TTF. Indeed, as it is adopted in the series model, a power grid is deemed to have failed as soon as any one of its branches has failed. But, the formation of the first void, as demonstrated in Fig. 3b, does not result in a grid failure, which requires 10% increase of the voltage drop. Increase of voltage drop in the grid nodes was caused mainly by voiding

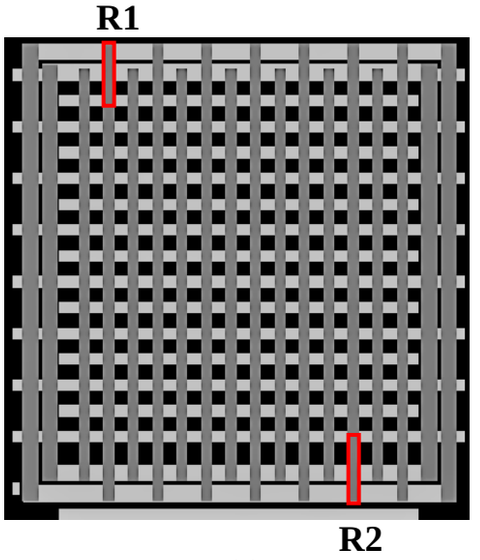
of the resistors R1 and R2 in an upper metal layer (Fig. 3a). At $t_1 \sim 6.4\ years$, when the resistor R1 was voided, maximal voltage drop increase was 1.1% (Fig. 3b). Further increase of ΔV up to 3.5% at $t_2 \sim 8.6\ years$ was caused by the void growth (Fig. 3c). Voiding of the second resistor R2 at t_2 resulted in more abrupt increase of ΔV, and the failure criteria of 10% voltage drop increase was met at $t_f \sim 11\ years$ due to the cumulative effect of growing voids in these two failed wires. Such behavior of ΔV reveals an essential contribution of voiding kinetics into TTF.

Table.1 Dependency of the tool performance on power grid sizes.

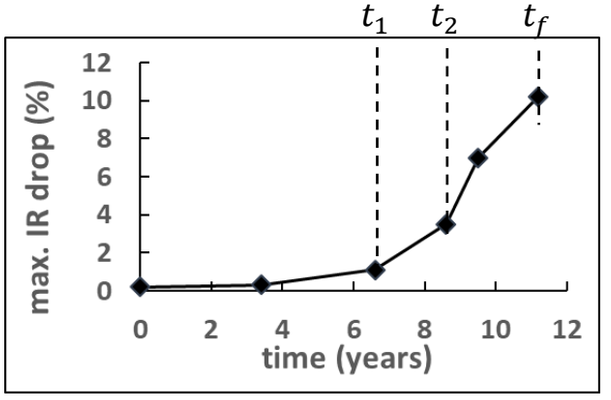
Power Grids				**Performance**
Grid	**Num. of nodes**	**Num. of branches**	**Num. of trees**	**CPU time**
Ibmpg1	$6 \cdot 10^3$	$1.1 \cdot 10^3$	709	0.5 min
Ibmpg2	$6.2 \cdot 10^4$	$6.1 \cdot 10^3$	462	1 min
Ibmpg3	$4.1 \cdot 10^5$	$4.01 \cdot 10^3$	$8.1 \cdot 10^3$	3.8 min
Ibmpg4	$4.75 \cdot 10^5$	$4.65 \cdot 10^5$	$9.6 \cdot 10^3$	6.2 min
Ibmpg5	$2.49 \cdot 10^5$	$4.96 \cdot 10^5$	$2 \cdot 10^3$	1.4 min
Ibmpg6	$4.04 \cdot 10^5$	$7.98 \cdot 10^5$	$1.2 \cdot 10^4$	12.0 min
Grid1	$1.32 \cdot 10^7$	$1.07 \cdot 10^7$	$2.49 \cdot 10^6$	3.5 h
Grid2	$1.6 \cdot 10^7$	$1.25 \cdot 10^7$	$2.78 \cdot 10^6$	5.5 h

Statistical analysis with Monte-Carlo loops, around the stress simulation core, accurately extracts the MTTF by proper statistical averaging the failure times[1] and detects the wires that are most vulnerable to EM failure. Parallel processing of different MC

samples is performed, which provide good performance of the tool-prototype. Table1 summarizes the runtime dependency on number of nodes, resistors, and interconnect trees in power grids, obtained for IBM power grid benchmarks[10] and for two commercial power grids. Here, "Grid1" and "Grid2" represent VDD nets of two different designs of 45 nm and 28 nm technologies, correspondingly.



(a)



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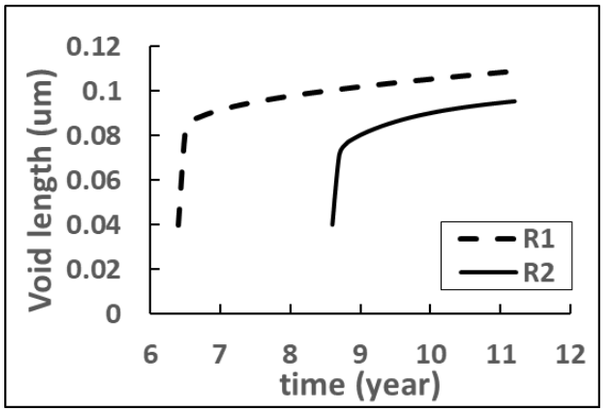

(c)

Fig. 3. Failure of the power grid: (a) – layout of metal layer containing two voided resistors R1 and R2; (b) – voltage drop evolution; (c) – voiding kinetics of the resistors R1 and R2.

Figure 4 shows a voided metal line segment as the highlighted feature in the metal layer layout. High voiding probability of 90.625% for this resistor was caused by the specific configuration of electric currents in branches of the corresponding tree. Sure, high voiding probability doesn't imply by itself a crucial impact of the resistor on the grid failure, combining this analysis with the voltage drop tracking is required for detecting the most EM-vulnerable resistors, which can violate performance of p/g network.

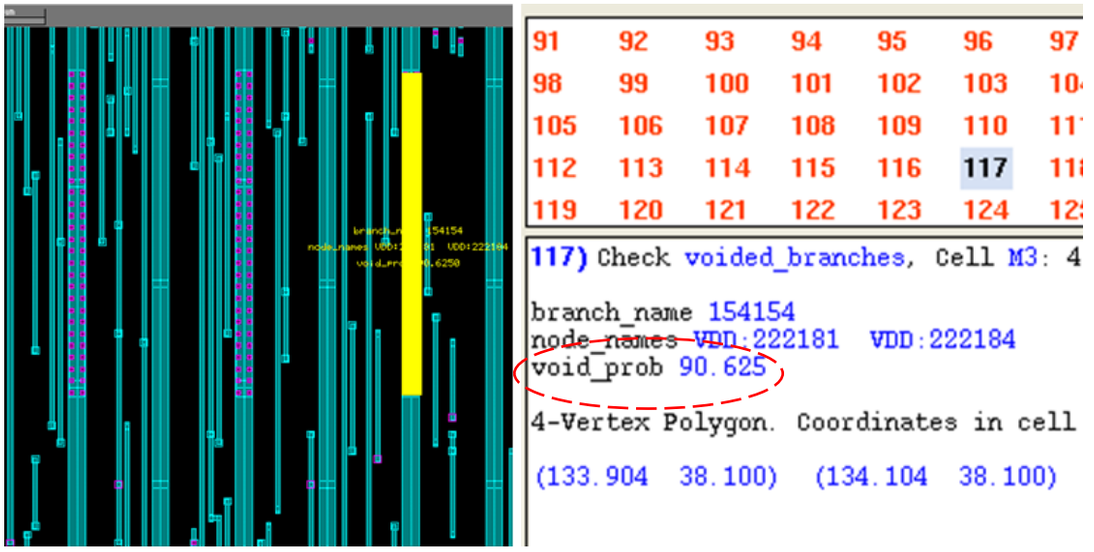

Fig. 4. Highlighted wire with high voiding probability on layout of a metal layer.

V. SUMMARY AND CONCLUSIONS

The tool-prototype presented in this paper was developed for EM assessment of p/g grids of large ICs. The failure of the grid happens when the required level of voltage cannot be delivered to any operational unit of the IC due to increase of resistances in the voided interconnect branches. A physics-based model of stress evolution in interconnect trees providing the voiding site locations coupled with models describing void evolution kinetics allows an accurate simulation of voltage evolution in VDD/VSS networks.

Despite the one-dimensional character of the void growth model, a significant contribution of the void growth time to the grid TTF was shown. Further improvement of modeling the voiding kinetics including an effect of different types of voids nucleated in metal line – via structures on the resistance degradation[11] will be a subject for future research.

Data Availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

[1]S. Chatterjee, V. Sukharev and F. N. Najm, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **37**, 1317 (2018).

[2]X. Huang, A. Kteyan, S. Tan, and V. Sukharev, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems **35**, 1848 (2016).

[3]M. A. Korhonen, P. Borgesen, K. N. Tu, and C.Y. Li, J. Appl. Phys. **73**, 3790 (1993).

[4]M. Hauschildt, C. Hennesthal, G. Talut, et al, 2013 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, 2013, pp. 2C.1.1-2C.1.6.

[5]V. Sukharev, A. Kteyan, and X. Huang, IEEE Transactions on Device and Materials Reliability **16**, 50 (2016).

[6]Z. Suo, "Reliability of Interconnect Structures" in *Volume 8: Interfacial and Nanoscale Failure*, edited by W. Gerberich, W. Yang, Comprehensive Structural Integrity, Elsevier, Amsterdam, 2003, pp. 265-324

[7]V. Sukharev, A. Kteyan and J.-H. Choy, *Proc. International 3D Systems Integration Conference (3DIC), Sendai, Japan*, 1 (2019).

[8]L. Cao, K. J. Ganesh, L. Zhang, O. Aubel, C. Hennesthal, M. Hauschildt, P. J. Ferreira, and P. S. Ho, Appl. Phys. Letters **102**, 131907 (2013).

[9]Y. Chen, T. Davis, W. Hager, and S. Rajamanickam, ACM Trans. Math. Softw. **35**, 3, (2008).

[10]S. R. Nassif, "Power grid analysis benchmarks," in Proc. Asia South Pacific Design Automation Conf. (ASPDAC), 376 (2008).

[11]C. Zhou, R. Fung, S-J Wen, R. Wong, and C. H. Kim, IEEE Transactions on Device and Materials Reliability **20**, 74, 1317 (2019).

Figure captions

Fig. 1. Schematics of interconnect tree in M1 layer of the test design.

Fig. 2. Schematics of the tool flow.

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Fig. 4. Highlighted wire with high voiding probability on layout of a metal layer.

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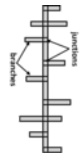

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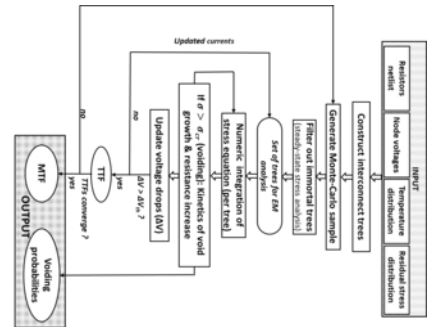

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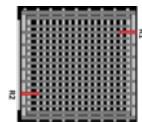

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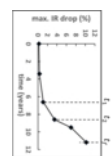

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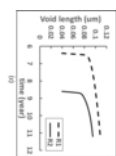

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