Microelectronics Reliability 123 (2021) 114200

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Equivalent circuits for electromigration☆

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ARTICLE INFO

Keywords:
Electromigration
Integrated circuits
Metal interconnect
Stress
Flux
Equivalent circuit

ABSTRACT

Electromigration continues to be a major concern for integrated circuit design. The susceptibility to electromigration is assessed by tracking the stress in metal lines under the influence of applied currents, which can be computationally expensive for large chips. Over the last few years, an efficient approach for tracking stress in large interconnect networks has been developed, and well-received, in part because it provides a model for stress dynamics in the form of a standard linear time-invariant dynamic system. In the context of this model, we will show that the dynamic behavior of the stresses and fluxes in metal lines is exactly identical to the dynamic behavior of voltages and currents in certain RC circuits that can be easily constructed for the metal lines. Thus, electromigration assessment for any metal interconnect structure can be done by simply simulating the corresponding equivalent RC circuit. This opens the door for benefiting from well-known techniques for fast circuit simulation, as well as methods for macro-modelling and analysis of RC circuits, in order to improve the performance and capacity of practical methods for electromigration assessment in large circuits.

1. Introduction

In a metal line carrying significant current density, the free electrons push and move the metal atoms in the direction of the electron wind, i.e., towards the anode end of the line; hence the name *electromigration* (EM) for this effect. The resulting atomic flow increases compressive stress at the anode and tensile stress at the cathode, which creates a stress gradient that presents an opposing driving force that retards EM [1]. If the levels of stress become high enough, a void may be created due to high tensile stress near the cathode, or a hillock (extrusion of metal through cracks in the dielectric) may form due to high compressive stress near the anode, which can either way result in circuit failure. With the confinement of metal lines in today's metal technology, voids are much more likely than hillocks and so one is often more concerned with the buildup of tensile stress. We will follow the common convention that tensile stress is positive and compressive stress is negative. A void is created once the stress exceeds a certain level of stress, called the *critical stress*, denoted σ_{crit}, which is an effective parameter that depends on a number of factors. Stress is measured in units of pascal (Pa), and a typical value of the critical stress today [2] is about 500 MPa.

We focus on the on-chip power distribution network (PDN) because it is generally more susceptible to EM due to the fact that it carries mostly uni-directional currents. The PDN consists of the power grid and the ground grid. Modern grids span multiple layers (often all the layers) of metallization and they consist of meshes of power and ground lines. Without loss of generality, we will focus on the power grid. Under the influence of EM, metal atoms can travel between different connected branches on the same layer. However, in the modern dual-damascene semiconductor process, they cannot travel through a via to other metal layers above and below, because of the metal liner under every via which acts as a barrier to atomic movement but allows electron movement. As a result, EM-induced metal transport within a layer remains within that layer, so that the overall analysis problem is decomposed into sub-problems on different layers. Within any given layer, one will typically find a large number of such physically disconnected portions of the power grid. The vast majority of these structures turn out to be trees, i.e., they have no cycles. So, it is typical in the field to simply use the term *interconnect tree* to refer to these metal islands.

For any given interconnect tree under the influence of EM, the time duration before any voids have nucleated (i.e., formed) is called the *nucleation phase*. In this phase, the resistance of a line remains the same as that of a fresh (undamaged) line. Once a void has nucleated, the *void growth phase* begins and the void starts to grow. The growth rate is initially fast and can in some cases, depending on layout geometry, quickly cause an open circuit leading to early failures. In other cases, the line may continue to conduct current after void nucleation, and the void continues to grow in the direction of the electron flow until it saturates at some steady-state size. Correspondingly, the line resistance also

☆ This research was supported in part by the Semiconductor Research Corporation (SRC) and by the Natural Sciences and Engineering Research Council of Canada.
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https://doi.org/10.1016/j.microrel.2021.114200
Received 2 December 2020; Received in revised form 14 May 2021; Accepted 6 June 2021
Available online 24 June 2021

increases towards some steady-state value. In order to track the evolution of the line (and tree) towards voiding and beyond, one needs to simulate and track the values of stress in the lines over time.

We will see in this paper that the relationship between stress and atomic flux in metal lines is identical to that between voltage and current in electrical circuits. Indeed we will see that, for any interconnect tree, we can construct an RC circuit whose voltage evolution over time is identical to the stress evolution in the tree. The two systems of equations are exactly identical, so that the RC circuit is an *equivalent circuit*. This is not simply an interesting curiosity; it can be very useful to draw on the extensive research and knowledge in the art of simulation of electronic circuits in order to improve the capabilities for EM assessment. For one thing, this would allow easy simulation of stress in interconnect trees using standard simulators like SPICE, thus benefiting from the many techniques that circuit simulators use to speed up the analysis. Also, as we will see, the stress analysis of a metal line can be replaced by the voltage analysis of an RC-chain, which is a very well-studied circuit structure, with many theoretical and numerical techniques for analysis and modelling, including reduced-order modelling and macromodelling.

2. Background

We will give a detailed review of the one-dimensional (1D) EM model developed by M. A. Korhonen [3], which we will refer to as the *Korhonen model*. Consider a metal line carrying current density j, with uniform height h and width w, confined in a rigid dielectric material with line length along the x axis, as shown in Fig. 1. By necessity, a 1D model assumes that there is uniformity across the other two dimensions, i.e., across the metal line cross-section in this case. Specifically, we assume that stress, electric current density, material density, as well as atomic transport rates are all uniform across the wire cross-section. This assumption is central to the Korhonen model, but it is only valid for interior sections of uniform metal lines, which excludes certain layout features of interconnect trees. Specifically, three layout features of the metal interconnect merit attention [4]: (*i*) the case where one or more lines on the same metal layer are all connected to a via that provides electrical conductivity to another layer, above or below; (*ii*) the case where three or more lines on the same layer are connected at the same physical location, without necessarily a via to another layer; and (*iii*) the case where one metal line connects to another line of different width. Because voids are commonly found at vias, the first case is of special importance and merits special case treatment. The other two cases also require special case treatment because of the abrupt changes in electrical current and, therefore, in atomic flux that are exhibited in these structures. We refer to the layout features of these three special cases as a layout *junctions*, and we categorize them according to the number of lines involved, so-called the *degree* of the junction. Following the terminology of [4], as shown in Fig. 2, a degree-1 junction (i.e., a junction of degree 1) is called a *diffusion barrier*, a degree-2 junction is called a *dotted-I* junction, a degree-3 junction is a *T-junction* and a degree-4 junction a *plus-junction*.

Because of the metal liner and the capping layer around every metal line, mass is conserved inside an interconnect tree, so that any change of material density in a metal line results in a change of the stress (pressure) in that line. Specifically, with $C(x,t)$ as the atomic concentration in

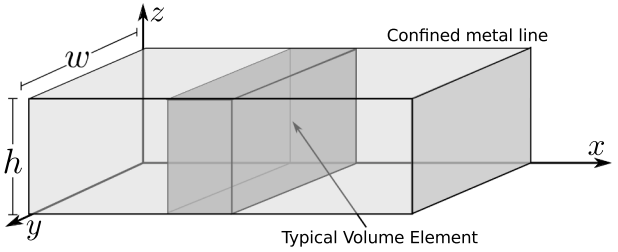

Fig. 1. Schematic for a confined metal line.

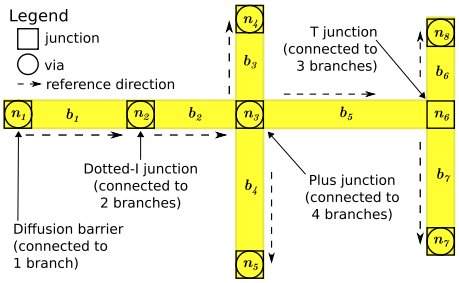

Fig. 2. Typical interconnect tree with various junction types.

the line and $\sigma(x,t)$ as the stress, at distance x from one end of the line at time t, a relative change in concentration corresponds to an incremental change of stress, i.e.,

$$\frac{dC}{C} = -\frac{d\sigma}{B}, \tag{1}$$

as shown by Korhonen [3] based on the early work of Eshelby [5], where B is the *effective bulk modulus* [6], which depends on metal line geometry and microstructure. It has a typical value [2] of about 30 GPa in modern technology. Let C_0 be the concentration under zero stress, so that $C_0 = 1/\Omega$, where Ω is the atomic volume for the metal in the line, which is $\approx$1.66E-29 m^3 for Copper. Integrating Eq. (1) from $(0, C_0)$ to (σ, C) gives $C = C_0 e^{-\sigma/B}$. But, because typically $\sigma/B \leq \sigma_{\text{crit}}/B = 0.0166$ is very small, we can use the approximation $e^{-\sigma/B} \approx 1 - \sigma/B$ to write

$$C \approx C_0(1 - \sigma/B). \tag{2}$$

The Korhonen model is a combination of two equations, an *atomic flux equation* that keeps track of atomic mass transport, and a *continuity equation* that enforces mass conservation, as we will review and sketch in the following *simplified* description.

2.1. Atomic flux equation

The first equation is based on the consideration that migration of metal atoms is primarily the result of (*i*) atomic drift due to the bombardment by the electron wind arising from the electric field in the metal line, $E = \rho j$, where ρ is the metal resistivity and j is the current density, and (*ii*) atomic diffusion due to the *stress gradient* $\partial\sigma/\partial x$, resulting in an opposing flux. We will use $\phi(x,t)$ to denote the *atomic flux* in the line, whose units are number of atoms per second per unit cross-sectional area. The distance variable x, the electric current in the line (of density j) and the atomic flux ϕ are all assumed to have the same *reference direction*. So, *both current and flux are positive when they are in the positive x direction*. Considering the two opposing fluxes, one arrives at[1]

$$\phi = \frac{DC}{k_b T}\left(\Omega\frac{\partial\sigma}{\partial x} - q^* \rho j\right), \tag{3}$$

where D is the coefficient of atomic diffusion, also simply called the *diffusivity*. Its value depends on the material properties and on temperature as $D = D_0 \exp(-E_a/k_b T)$, where $D_0 \approx 5.20 \times 10^{-5}$ m^2/s in modern technology and E_a is the *activation energy* for atomic diffusion, typically taken as $E_a \approx 1$ eV, so that $D \approx 1.31 \times 10^{-17}$m^2/s is typical today. Other terms include T as the metal line temperature in Kelvin; $k_b = 1.380\,649 \times 10^{-23}$ J/K is Boltzmann's constant; $q^* = |e|Z$ is the *effective charge*, where $|e| = 1.602\,176\,634 \times 10^{-19}$ C is the absolute value of the electron charge, and Z is the *effective valence*, which is a scalar whose value

[1] Eq. (2) in [3] for atomic flux is in terms of the divergence of the chemical potential function, but it's also provided in terms of stress, and because divergence in 1D is simply the derivative, one gets the expression shown here as Eq. (3).

justifies the measured driving forces exhibited in metal lines under the applied electric fields [7]. In modern chip technology, it's typical [2] to use $Z \approx 10$ so that $q^* \approx 1.60 \times 10^{-18}$ C. Finally, $\rho = 3.0 \times 10^{-8}$ ohm.m (Copper) at 400 K, with a temperature dependence of $\Delta\rho/\rho = 0.0039(T - 400)$ around that value [2]. These various values are summarized in Table 1. Appealing to Eq. (2) and further considering that $\sigma/B \ll 1$, so that $C \approx C_0 = 1/\Omega$, one arrives at the expression for flux as used by Korhonen,

$$\phi = \frac{D}{k_b T}\left(\frac{\partial\sigma}{\partial x} - \frac{q^*\rho}{\Omega} j\right). \tag{4}$$

2.2. Continuity equation

The second part of the Korhonen model is a continuity equation that describes the stress evolution over time in response to the material transport. It expresses a simple balance: the more material that flows out of a region, the less material there is inside it over time. This may be tracked using the mathematical concept of *divergence* of a vector field. Divergence measures the net rate of reduction of a certain quantity (in this case, the number of atoms) within an infinitesimal region around a point, per unit volume. Divergence has both a differential form and an integral form. In 3D space, with orthonormal unit vectors u_x, u_y and u_z, the flux Φ is a vector quantity with three components, so that $\Phi = \phi_x u_x + \phi_y u_y + \phi_z u_z$, and the differential form of the divergence of Φ is the scalar

$$\nabla\cdot\Phi = \frac{\partial\phi_x}{\partial x} + \frac{\partial\phi_y}{\partial y} + \frac{\partial\phi_z}{\partial z}. \tag{5}$$

The integral form of the divergence operator ∇ in 3D relates to an arbitrary closed surface that is the boundary of a spatial region $\mathscr{R}$ that includes a point of interest, so that the surface is denoted $\partial\mathscr{R}$, in which case the divergence of Φ at that point is the limit of a *surface integral*, as

$$\nabla\cdot\Phi = \lim_{|\mathscr{R}|\to 0} \frac{1}{|\mathscr{R}|} \oiint_{\partial\mathscr{R}} \Phi\cdot\mathbf{n}\, ds, \tag{6}$$

where '·' denotes the vector dot-product, $\mathbf{n}$ is the outward unit normal vector at the surface element ds and $|\mathscr{R}|$ is the volume of the region. For our EM problem, for a certain net atomic flux leaving the region, we get a corresponding rate of reduction in the material in that region, which can be expressed in terms of the atomic concentration in that region as

$$\frac{\partial C}{\partial t} + \nabla\cdot\Phi = 0. \tag{7}$$

Based on Eq. (2), we have $\partial C/\partial t = -(C_0/B)(\partial\sigma/\partial t)$, so that

$$\frac{\partial\sigma}{\partial t} = B\Omega\nabla\cdot\Phi. \tag{8}$$

In general, the divergence can be computed using either the differential or integral form. In the 1D case, the differential form is convenient, so that

$$\nabla\cdot\Phi = \frac{\partial\phi}{\partial x} \tag{9}$$

Table 1
A number of physical constants in SI units.

Name	Symbol	Value	Units
Boltzmann's constant	k_b	1.380649E−23	J/K
Elementary charge	$\|e\|$	1.602176634E−19	C
Effective valence	Z	10.00	–
Effective charge	q^*	1.60E−18	C
Atomic volume	Ω	1.66E−29	m^3
Temperature	T	400.00	K
Resistivity (Copper)	ρ	3.00E−08 @400 K	ohm.m
Activation energy	E_a	1.00	eV
Diffusivity factor	D_0	5.20E−05	m^2/s
Atomic diffusivity	D	1.31E−17 @400 K	m^2/s
Effective bulk modulus	B	3.00E10	Pa

where ϕ is the scalar component of Φ in the 1D x-direction of interest, leading to the continuity equation in the form used by Korhonen,

$$\frac{\partial\sigma}{\partial t} = B\Omega\frac{\partial\phi}{\partial x}. \tag{10}$$

2.3. The full model

Putting together the two Eqs. (4) and (10) results in *Korhonen's equation*

$$\frac{\partial\sigma}{\partial t} = \frac{B\Omega}{k_b T}\frac{\partial}{\partial x}\left\{D\left(\frac{\partial\sigma}{\partial x} - \frac{q^*\rho}{\Omega} j\right)\right\}, \tag{11}$$

which, assuming the diffusivity is constant along the length of the line, as is typically assumed in the field, takes the more commonly used form

$$\frac{\partial\sigma}{\partial t} = \frac{B\Omega D}{k_b T}\frac{\partial}{\partial x}\left(\frac{\partial\sigma}{\partial x} - \frac{q^*\rho}{\Omega} j\right). \tag{12}$$

According to [8], "*The Korhonen model has been successfully used to explain a wide range of experimental behavior*," and they cite [9–12] for this. Throughout this paper, we will assume that the applied currents, and therefore *the currents in all branches, are constant over time*. For a uniform line under constant current, the model takes the simpler form

$$\frac{\partial\sigma}{\partial t} = \frac{B\Omega D}{k_b T}\frac{\partial^2\sigma}{\partial x^2} \tag{13}$$

which is basically the *heat equation*.

2.4. Extended Korhonen model (EKM)

The Korhonen model is a 1D model that applies at interior points of metal lines, but not at junctions. Before one can extend that model to multi-line interconnect trees, a model is needed for junctions that can be combined with the 1D model of the metal lines. This has been done in the so-called *extended Korhonen model* (EKM) [4]. The method assumes that a junction is a zero-volume *point*, and enforces mass conservation at that point so that the incoming and outgoing mass transport rates balance out. Then, and even though it's not strictly applicable, Korhonen's equation is applied at the junction anyway, with the hope that the error would be small because the equation is applicable nearby, in the lines. The method performs well in practice in spite of this approximation. The scheme also requires tracking the stress at "ghost points" around the junctions, which disturbs the structure of the system matrix in ways that are not desirable for numerical work.

Nevertheless, the artificial step of applying Korhonen's equation right at the junction is a shortcoming of this approach. Furthermore, while junctions are often small in size, they are sometimes designed to have considerable volume so as to act as reservoirs of atoms that can fill nearby micro-voids, if they form. EKM cannot handle such layout features, so this is another shortcoming of the method. In this paper, we will propose a new junction model that eliminates both these shortcomings, which will also turn out to be useful for development of an equivalent circuit.

In EKM, the junction model is used to stitch up and combine the various instances of Korhonen's equation applied to every line into a set of dynamic (ODE) equations for the whole metal structure under consideration. A preliminary step is to create *reference directions* for all the branches, which are generated by a breadth-first search graph traversal algorithm. These directions can be arbitrary, but must remain fixed throughout the analysis.

In general, voids can nucleate in many different places in interconnect trees, very often at junctions, but also internal to metal lines. The data seem to suggest [8] that internal voids appear mostly because of pre-existing micro-voids internal to the line as a result of the fabrication process. The EKM framework [4] assumes that there are no pre-existing voids, and no internal voids ever, so that all voids are assumed to

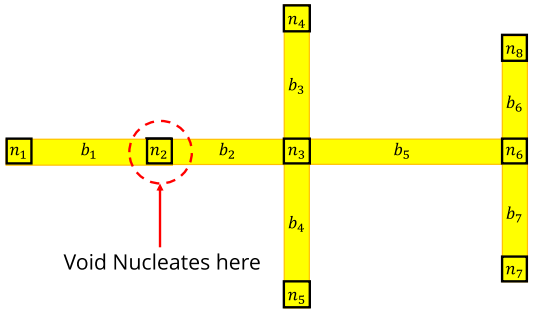

Fig. 3. A tree with a void at a dotted-I junction.

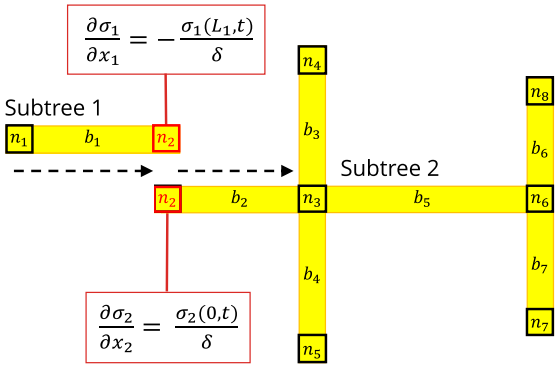

Fig. 4. A tree with a void is broken up into two sub-trees.

nucleate at junctions. Furthermore, the treatment of voids in EKM depends on whether the void is at a degree-1 junction, which we will also call a *terminal junction* or *terminal node* of the tree, or at a junction with degree of more than 1 (non-terminal junctions). If the void forms at a non-terminal junction, such as in Fig. 3, the tree is broken up into multiple sub-trees [13], as in Fig. 4, by (*i*) tearing out that node from the tree graph, which creates multiple disconnected sub-trees, (*ii*) creating new copies of the original node for each of these sub-trees and reinstating in each of them the edge that was originally connected to that node, and (*iii*) applying a boundary condition at each of these duplicate nodes that represents the presence of a void there. As a result, we end up with a situation where multiple voids have been created at these (new) terminal junctions in the separate sub-trees. Therefore, for void analysis in the context of EKM, voids (once they have formed and the tree has been partitioned) will exist only at terminal junctions of interconnect trees. This also means that a void belongs to only a single metal line in a given sub-tree. It also means that no single line can have more than one void at a time. We adopt this tree partitioning approach of the EKM framework for treatment of voids in this paper. We will also expand on that approach, as described below.

2.5. Void analysis

The treatment of voids in EKM has one shortcoming which we will briefly describe then replace with better void models from the literature, as we will review below.

2.5.1. Void model

Voids are complex features of EM-induced damage. They are best described by a detailed 3D analysis [14–16]. In addition, there are various approaches for more efficient simplified models, including [17–20].

Voids can be partial or full (blocking the full cross-section of the line), they can increase in size until they reach a saturated size, or they can reverse course and decrease in size (healing) if the current changes direction, and they can move along the length of a metal line [8,21]. A simplified model that is suitable for 1D analysis was given in [18] (pg. 53), by making use of a phase field model [22], and this was the basis for the EKM work [4]. However, the implementation of the void model in [4] was based on the assumption that the void growth phase is very short relative to the nucleation phase, and so only the saturated void volume was part of the implementation, with no tracking of the void growth over time. More recently, it has become clear that void growth rates nowadays are such that the time to reach void saturation is not negligible [2], and so the 1D void model as implemented in the EKM framework should be improved so as to incorporate void growth tracking. We will see how this is done, leading to an equivalent circuit model that can track void growth.

According to the 1D void model in [18], the stress profile along the length of the line near the void is as shown in Fig. 5 for a void at the near end of the line ($x \approx 0$), and in Fig. 6 for a void at the far end ($x \approx l$). Right after the void is formed, with the stress having reached σ_{crit} at that point in order for the void to nucleate, the stress right at the void surface must clearly be zero, as there is no confinement there at all. But the stress inside the metal very close to the void surface cannot change instantaneously and so must still be at σ_{crit} initially (right after the void has formed) and will then decrease over time as the void grows and relieves the tensile stress. The distance between these two points is called the *effective thickness of the void interface* [18] and is shown in the two figures as the distance between the two dashed vertical lines, denoted by δ_s, and described [18] as being "*infinitely small in comparison with all other involved lengths*." One can think of this as the thickness of a very thin "*skin layer*" – it was set at $\delta_s = 1$ nm in [18], and we will use that value as well. The inner boundary of this skin layer is denoted by the $x_s(t)$ position in the figures, and the stress at that point is denoted $\sigma_s(t) \triangleq \sigma(x_s, t)$. The length of the void, denoted $l_{vd}(t)$ is indicated in the figures as the distance to the mid-point of the skin layer, but that is debatable as this is not a precise distance in the actual 3D void. For simplicity, in our work, it is estimated as $l_{vd}(t) \approx x_s(t)$, for a void at the near end, and $l_{vd}(t) \approx l - x_s(t)$ at the far end. The model assumes that the stress is linear throughout the skin layer, so that the *stress gradient in the skin layer* is given by

$$\frac{d\sigma}{dx} = \pm\frac{\sigma_s}{\delta_s}, \tag{14}$$

where the '+' is for a void at the near end and the '−' at the far end. This gradient increases the magnitude of the atomic flux flowing out of the void into the bulk of the metal (which is the reason for void growth), and that flux can now be written, based on Eq. (4), as

$$\phi(x_s) = \frac{D}{k_b T}\left(\pm\frac{\sigma_s}{\delta_s} - \frac{q^*\rho}{\Omega} j\right). \tag{15}$$

2.5.2. Void length

The rate of change of the void size is proportional to the rate at which material is transported off the void surface and into the bulk of the

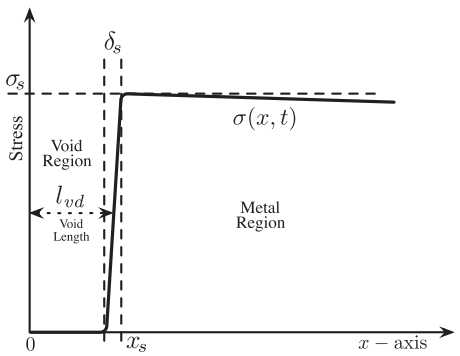

Fig. 5. The stress profile around a void at the near end of the line (x=0).

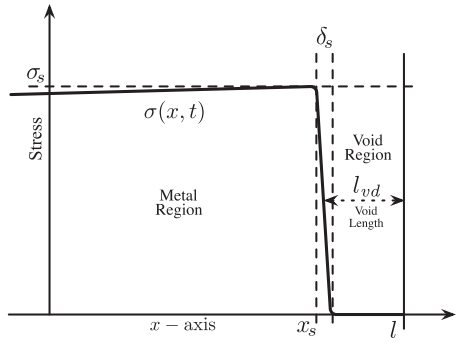

Fig. 6. The stress profile around a void at the far end of the line ($x = l$).

metal. This leads to [18] (pg. 56),

$$\frac{dx_s}{dt} = \Omega\phi(x_s). \tag{16}$$

Thus, for a void at the near end of line, we get

$$\frac{dl_{vd}}{dt} = \frac{D\Omega}{k_b T}\left(\frac{\sigma(0)}{\delta_s} - \frac{q^*\rho}{\Omega} j\right), \tag{17}$$

while for a void at the far end of the line,

$$\frac{dl_{vd}}{dt} = \frac{D\Omega}{k_b T}\left(\frac{\sigma(l)}{\delta_s} + \frac{q^*\rho}{\Omega} j\right). \tag{18}$$

For terminal voids, and because the void length is very small relative to the line length (typically under 2%), the common approach in the field is to numerically solve for the stress in the line while (*i*) assuming the length of the metal in the line remains fixed at its original length, and (*ii*) assuming $\sigma(x_s) \approx \sigma(l)$ or $\sigma(x_s) \approx \sigma(0)$, depending on the location of the void, and this constitutes the boundary condition at that junction, which is needed for the solution.

2.5.3. Resistance change

Once a void has formed, the metal line resistance is impacted and the new resistance value depends on the void length, so that it is time-dependent and grows towards a saturated value. The easiest way to think of this is to consider the voided line to be the series connection of two wires. The first, corresponding to the un-voided length of wire $l - l_{vd}(t)$, has a resistance that depends only on the Copper (ignoring the liner, whose resistivity is much higher), so it is given by $\rho(l - l_{vd})/wh$, where ρ, w and h are as defined earlier. The second is due to the void, where electric current flows only through the liner, so that the resistance is $\rho_{\text{lin}} l_{vd}/h_{\text{lin}}(w + 2h)$, where ρ_{lin} is the resistivity of the liner material, h_{lin} is the thickness of the liner and $(w + 2h)$ is the sum of line dimensions around the cross-section of the wire, as in Fig. 3 of [18]. As a result, the resistance of the voided line is

$$R(t) = R_0 + \left(\frac{\rho_{\text{lin}}}{h_{\text{lin}}(w + 2h)} - \frac{\rho}{wh}\right) l_{vd}(t), \tag{19}$$

where $R_0 = \rho l/wh$ is the resistance of the original (un-voided) line. Typical values for the metal parameters are given in [18] as $h = 120$nm, $h_{\text{lin}} = 10$nm and $\rho_{\text{lin}} = 2.5\mu\Omega$·m, while $\rho = 0.03.\mu\Omega$·m. For a 1μm wide line, the term inside the large parentheses on the right is about $200\Omega/\mu$m, while the resistance per unit length for the un-voided section of the line is about $0.25\Omega/\mu$m.

3. New junction model

We will introduce a new junction model that overcomes the shortcomings of the model used in EKM as described in Section 2.4. Recall the *divergence theorem*, also known as the *Gauss-Ostrogradsky theorem*, which states that the surface integral of the flux through a closed surface is equal to the volume integral of the divergence of that flux over the region inside that surface. We normalize this by the volume, to state the theorem in this form

$$\frac{1}{|\mathscr{R}|}\iiint_{\mathscr{R}} \nabla\cdot\boldsymbol{\Phi}\, dv = \frac{1}{|\mathscr{R}|}\oiint_{\partial\mathscr{R}} \boldsymbol{\Phi}\cdot\mathbf{n}\, ds. \tag{20}$$

So, the *average flux divergence* over a given finite volume can be found by tallying up the *net outgoing flux* through the surface bounding it, normalized by the volume. Based on this, let $\mathscr{R}$ be the 3D spatial region of some junction, and $\mathscr{V}$ be the volume of that region, then using Eq. (8) with $\sigma_{\mathscr{R}}(x, y, z; t)$ as the stress in the 3D region, we can write

$$\frac{1}{\mathscr{V}}\iiint_{\mathscr{R}} \frac{\partial\sigma_{\mathscr{R}}}{\partial t} dv = \frac{B\Omega}{\mathscr{V}}\oiint_{\partial\mathscr{R}} \boldsymbol{\Phi}\cdot\mathbf{n}\, ds, \tag{21}$$

so that the average value of $\dot{\sigma}_{\mathscr{R}}$ throughout the junction volume is proportional to the surface integral of the fluxes flowing across the junction boundary. It is reasonable to choose this average value of $\dot{\sigma}_{\mathscr{R}}$ over the junction volume to be *the* value of $\dot{\sigma}(t)$ for this junction in the context of a 1D model, to be used along with the Korhonen model. Indeed, 1D models are often constructed based on average quantities. Therefore, our new junction model will be based on the requirement,

$$\dot{\sigma}\left(t\right) = \frac{B\Omega}{\mathscr{V}}\oiint_{\partial\mathscr{R}} \boldsymbol{\Phi}\cdot\mathbf{n}\, ds. \tag{22}$$

Because the flux across the boundary is only non-zero where a branch connects to the junction, and assuming that the fluxes in the lines are perpendicular to the boundary where they cross the junction region boundary, which is a reasonable simplification, then Eq. (22) provides

$$\left(\frac{\mathscr{V}}{B\Omega}\right)\dot{\sigma}(t) = \sum_{k\in\mathscr{B}_{\text{out}}} a_k\phi_k(0) - \sum_{k\in\mathscr{B}_{\text{in}}} a_k\phi_k(l_k), \tag{23}$$

where a_k and l_k are the cross-sectional area and the length of branch k, respectively, while $\mathscr{B}_{\text{out}}$ ($\mathscr{B}_{\text{in}}$) is the set of branches incident on this junction whose reference direction is away from (towards) the junction. Note that if we set $\mathscr{V} = 0$, this equation reduces to that used in EKM [4]. In many cases, the junction volume is negligible compared to the volume of metal in the lines, so that this setting becomes reasonable. However, we have hereby given a more rigorous justification for this more general 1D junction model that allows for junctions that have significant volume and does not artificially apply Korhonen's equation at junctions.

4. Distributed equivalent circuit

This section contains the bulk of our contribution. We will develop and describe a number of equivalent circuits that make use of *distributed* RC transmission lines, whose simulated solution can give us the desired stresses for the whole interconnect tree, including junctions as well as interior points of metal lines, covering both the void nucleation and void growth phases.

4.1. Equivalent circuit for the nucleation phase

Consider first an interconnect tree without any voids. We start by identifying the connection between the equations for stress in a metal line and those for voltage in a distributed RC transmission line. Recall that Korhonen's equation for a uniform metal line with fixed current density Eq. (13) is given by

$$\frac{\partial^2\sigma}{\partial x^2} = \tau_l\frac{\partial\sigma}{\partial t}, \tag{24}$$

where $\tau_l \triangleq k_b T/(B\Omega D)$ which, it's easy to verify using Table 2, has units of s/m^2. This special case of the *heat equation* is also called the *diffusion equation* and it happens to also be the governing equation for a *distributed*

RC *transmission line*, i.e., a transmission line with no series inductance and no shunt conductance. This can be seen by starting from first principles and considering an infinitesimal section of the line, as in [23]. Another, indirect approach starts with the *general transmission line equations*[2] [24] (pg. 438),

$$\frac{\partial v}{\partial x} = -ri - l\frac{\partial i}{\partial t} \tag{25}$$

$$\frac{\partial i}{\partial x} = -gv - c\frac{\partial v}{\partial t} \tag{26}$$

where $v(x,t)$ and $i(x,t)$ are the voltage and current along the line (i is positive in the positive x direction), r and l are the series resistance and inductance per unit length, and c and g are the shunt capacitance and conductance per unit length. Then, we set l and g to zero, corresponding to a simple RC line with no inductance and no leakage, to get

$$\frac{\partial v}{\partial x} = -ri \quad \text{and} \quad \frac{\partial i}{\partial x} = -c\frac{\partial v}{\partial t}. \tag{27}$$

Differentiating the first equation with respect to x and substituting from the second equation provides

$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t}, \tag{28}$$

where rc has units of (ohm/m)(F/m) = s/m^2, just like τ_l in Eq. (24). The two Eqs. (24) and (28) are virtually identical, so that it should be possible to use a transmission line to model and simulate the stress in a metal line, as we will see below.

4.1.1. Line equivalent circuit

For a uniform metal line, let this be the kth line in the interconnect tree, we now define the following per-unit-length parameters,

$$r_k = \frac{k_b T}{D_k a_k \psi} \quad \text{and} \quad c_k = \frac{a_k \psi}{B\Omega}, \tag{29}$$

where $\psi \triangleq 0.01\,\mathrm{C}^2/\mathrm{m}^3$ is a scale factor that provides desirable unit conversion and helps avoid running into numerical errors due to very small or very large numbers. It is easy to verify, using Table 2, that r_k has units of resistance per unit length (ohm/m), c_k has units of capacitance per unit length (F/m) and

$$\tau_k \triangleq r_k c_k = \frac{k_b T}{B\Omega D_k} = \tau_l, \tag{30}$$

which is the same τ_l in Eq. (24).

Next, let $\xi \triangleq 1\mathrm{V/MPa}$ be another scale factor, which we use to define

$$v(x,t) \triangleq \xi\sigma(x,t) \tag{31}$$

as the *voltage associated with the stress* $\sigma(x,t)$ at every point in the interconnect tree, then multiply both sides of Eq. (24) by ξ and use Eq. (30) to get

$$\frac{\partial^2 v}{\partial x^2} = \tau_k \frac{\partial v}{\partial t}. \tag{32}$$

Thus, indeed the governing equation for stress in a uniform metal line is identical to the governing equation for voltage in a distributed RC transmission line with the parameters r_k and c_k defined in Eq. (29). Formally, with $\tau_l = \tau_k$ from Eq. (30),

$$\frac{\partial^2 \sigma}{\partial x^2} = \tau_l \frac{\partial \sigma}{\partial t} \iff \frac{\partial^2 v}{\partial x^2} = \tau_k \frac{\partial v}{\partial t}. \tag{33}$$

Such a transmission line can be either solved analytically or simulated numerically in simulators like HSPICE® that comprehend transmission line models. The resulting voltages can be directly translated to stress by dividing by ξ.

It remains to consider the flux dynamics and whether they can be equally well represented in an equivalent circuit. To that end, notice that the first equation in Eq. (27) translates to $\partial\sigma/\partial x = -r_k i/\xi$ from which, using Eq. (4), we have

$$\phi(x) = -\frac{1}{\xi a_k \psi} i(x) - \frac{D_k}{k_b T}\frac{q^* \rho}{\Omega}\frac{I_k}{a_k}, \tag{34}$$

where $I_k \triangleq a_k j_k$ is the current in the kth branch of the original interconnect tree corresponding to the current density j_k. To simplify the notation, we will define the following current notation for the kth branch,

$$I_{S_k} = \frac{\xi}{r_k}\frac{q^* \rho}{\Omega} j_k = \left(\frac{\xi \psi D_k}{k_b T}\frac{q^* \rho}{\Omega}\right) I_k, \tag{35}$$

where I_{Sk} has units of current (A) with the same sign as j_k, and we can write

$$\phi(x) = \frac{-1}{a_k \xi \psi}\left(i_k(x) + I_{S_k}\right). \tag{36}$$

Thus, flux can be easily found from current in the transmission line, via an affine relationship Eq. (36) that includes the constant I_{Sk}.

The above relations for flux and stress motivate the definition of the *line equivalent circuit* shown in Fig. 7, which includes both the RC transmission line, with parameters r_k and c_k, as well as an *ideal current source* carrying the current I_S defined above. At any value of x, the stress in the metal line corresponds to the voltage in the transmission line at that point, while the flux is the (scaled) sum of the current in the transmission line at that x position *and* the current in the current source.

4.1.2. Junction equivalent circuit

Using Eq. (36) for the atomic flux, we can write the intensity of the atomic transport (number of atoms going through a cross-section of a metal line per second) as

$$a_k \phi(x) = -\frac{1}{\xi\psi}\left(i_k(x) + I_{S_k}\right). \tag{37}$$

The subscript k will be dropped when there's no risk of confusion, such as for a single isolated line. Combining this with the junction model (23), we get

$$\left(\frac{\mathscr{V}}{B\Omega}\right)\dot{\sigma}(t) = -\frac{1}{\xi\psi}\sum_{k\in\mathscr{B}_{\text{out}}}\left(i_k(0) + I_{S_k}\right) + \frac{1}{\xi\psi}\sum_{k\in\mathscr{B}_{\text{in}}}\left(i_k(l_k) + I_{S_k}\right) \tag{38}$$

and multiplying both sides by $\xi\psi$ converts $\dot{\sigma}$ to $\dot{v}$ and gives

$$\left(\frac{\mathscr{V}\psi}{B\Omega}\right)\dot{v}(t) = -\sum_{k\in\mathscr{B}_{\text{out}}}\left(i_k(0) + I_{S_k}\right) + \sum_{k\in\mathscr{B}_{\text{in}}}\left(i_k(l_k) + I_{S_k}\right). \tag{39}$$

This is the motivation for defining what we will call the *junction*

Table 2
Some derived SI units in terms of base SI units, where the symbol A stands for ampere.

Name	Symbol	Quantity	In SI base units
Pascal	Pa	Pressure, stress	$\mathrm{kg \cdot m^{-1} \cdot s^{-2}}$
Joule	J	Energy, work	$\mathrm{kg \cdot m^2 \cdot s^{-2}}$
Coulomb	C	Electric charge	s · A
Volt	V	Voltage	$\mathrm{kg \cdot m^2 \cdot s^{-3} \cdot A^{-1}}$
Farad	F	Capacitance	$\mathrm{kg^{-1} \cdot m^{-2} \cdot s^4 \cdot A^2}$
Ohm	Ω	Resistance	$\mathrm{kg \cdot m^2 \cdot s^{-3} \cdot A^{-2}}$

[2] Sometimes referred to as the *telegrapher's equations* or the *telegraphist's equations*.

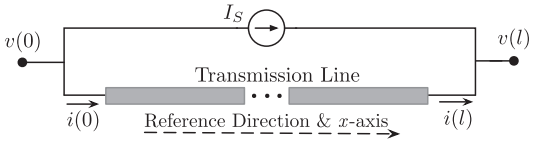

Fig. 7. The equivalent circuit for a metal line.

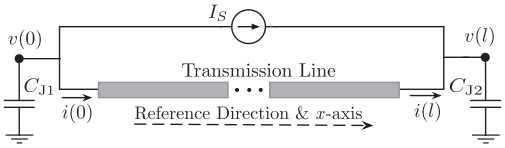

Fig. 8. The distributed equivalent circuit for the case of a single isolated line, redrawn.

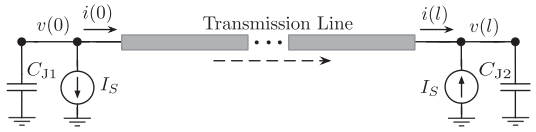

Fig. 9. The distributed equivalent circuit for the case of a single isolated line.

capacitance

$$C_J = \frac{\mathscr{V}\psi}{B\Omega} \tag{40}$$

which, it's easy to verify using Table 2, indeed has units of capacitance (F). Thus, the stress-flux model (23) for a junction is equivalent to the voltage-current model

$$C_J\dot{v}(t) = \sum_{k\in\mathscr{B}_{\text{in}}} \left(i_k(l_k) + I_{S_k}\right) - \sum_{k\in\mathscr{B}_{\text{out}}} \left(i_k(0) + I_{S_k}\right) \tag{41}$$

which we would like to reproduce at the corresponding node in the equivalent circuit. Because this is basically the result of the applying Kirchhoff's current law (KCL) at a node with capacitance C_J, then the equivalent circuit for a junction is simply a node with capacitance C_J to ground, fed by currents from its connected branches in accordance with Eq. (41). Note that, as defined, the junction capacitance is proportional to the junction volume, so that it represents the *capacity* of the junction to hold a certain number of atoms at a given stress value. As we develop the model further, we will see that C_J will often be set to zero, because it will be negligible in relation to the total line capacitances tied to that node. But, in general, it may be specified in the circuit description file whenever it's available, based on the junction volume extracted from the chip layout database.

4.1.3. Tree equivalent circuit

We will now combine the equivalent circuits for lines with the equivalent circuits for junctions to get an equivalent circuit for the whole interconnect tree. To start, for the case of a single isolated metal line, terminated by two degree-1 junctions, we will see that the equivalent circuit is as shown in Fig. 8, where the line equivalent circuit has been simply connected to the two junction equivalent circuits at its terminals. From basic circuit theory, this circuit can be redrawn as in Fig. 9 for simplicity, without any impact on the circuit currents and voltages. We can easily show that this circuit realizes the combination of the line Eq. (32) and the junction Eq. (41). All internal points of the line obviously satisfy Eq. (32), so that equivalence is established due to Eq. (33). As for the two junctions, apply KCL at the node at $x = 0$, i.e., at junction 1 with capacitance C_{J1}, to get $C_{J1}\dot{v}(0) = -(i(0) + I_S)$, while for the node at $x = l$, i.e., at junction 2 with capacitance C_{J2}, get $C_{J2}\dot{v}(l) = (i(l) + I_S)$, both of which satisfy Eq. (41) for the case of a single isolated line, so that equivalence is established due to Eq. (23) being equivalent to Eq. (41).

For interconnect trees consisting of multiple lines, multiple instances of the above line equivalent circuit can be connected in the same way as the actual metal lines are connected in the interconnect tree. Then, any junctions whose volumes are deemed significant would be represented by additional junction capacitances at the relevant line terminations, based on Eq. (40). An example is shown in Fig. 10 for the case of two metal lines connected at a dotted-I junction.

Furthermore, the equivalent circuits for multiple trees that form a whole power grid can be jointly simulated in order to find the stresses everywhere, in all trees. Very little extra work is needed for this extension, for simulation of the nucleation phase. Things get a bit more complicated when the void growth phase simulation is to be extended to whole power grids, as we will briefly describe at the end of the next section.

4.2. Equivalent circuit for the void growth phase

Consider next the case of an interconnect tree in which a void has formed, say at the far end of the line, at $x = l$. Recall that, as in the EKM framework, this means that this is a terminal junction of the tree, i.e., a junction of degree-1. We will define a few scaling factors and parameters that are needed for developing an equivalent circuit for the void end of the line. First let $\eta \triangleq 1\text{V/nm}$, which we will use as a conversion factor in order to track void length by means of a node voltage in the equivalent circuit. Then, define the following conductance G_s and capacitance C_v,

$$G_s = \frac{\psi D w h}{k_b T \delta_s} \quad \text{and} \quad C_v = \frac{\xi\psi w h}{\Omega\eta} \tag{42}$$

where δ_s is the void-metal interface thickness defined earlier. It is easy to verify, using Tables 1 and 2, that G_s and C_v indeed have units of conductance and capacitance, respectively.

For a void at the far end of the line, consider now the circuit in Fig. 11 which includes a *voltage-controlled current source* (VCCS) carrying the current $G_s v(l)$. As we will see, the new (relative to Fig. 7) circuit portion on the far right will provide (through G_s) enforcement of the void boundary condition (14) and will give us the ability (through C_v) to track the void length evolution over time, based on Eq. (16), i.e., $l_{vd}'(t) = -\Omega\phi(l)$. Recall, using Eq. (37) that

$$\phi(l) = \frac{-1}{\xi\psi w h}\left(i(l) + I_S\right). \tag{43}$$

Because KCL at the node marked $v(l)$ provides $i(l) = G_s v(l)$, then Eqs. (43) and (4) lead to

$$G_s v(l) + I_S = -\xi\psi w h \frac{D}{k_b T}\left(\frac{\partial\sigma(l)}{\partial x} - \frac{q^*\rho}{\Omega} j\right). \tag{44}$$

Using the expressions for G_s Eq. (42) and I_S Eq. (35), we get

$$\left(\frac{\xi\psi D w h}{k_b T}\right)\frac{v(l)}{\xi\delta_s} + I_S = -\left(\frac{\xi\psi D w h}{k_b T}\right)\frac{\partial\sigma(l)}{\partial x} + I_S \tag{45}$$

from which, using $v(l) = \xi\sigma(l)$,

$$\frac{\partial\sigma(l)}{\partial x} = -\frac{\sigma(l)}{\delta_s}, \tag{46}$$

so that the boundary condition (14) is enforced. As for the void length, KCL at the capacitor node provides

$$C_v\dot{v}_v = i(l) + I_S \tag{47}$$

where we have again used the fact that $i(l) = G_s v(l)$. Substituting for C_v

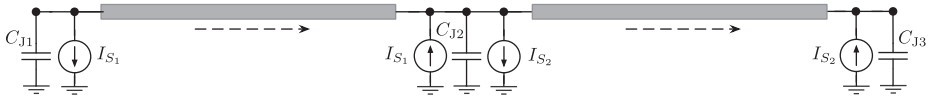

Fig. 10. The distributed equivalent circuit for the case of two lines in a dotted-I arrangement.

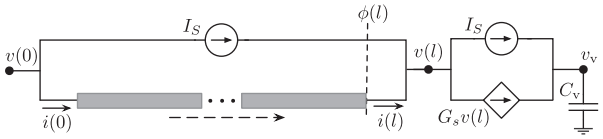

Fig. 11. Equivalent circuit (version 1) for a line with a void at $x = l$.

Fig. 13. Equivalent circuit (version 3) for a line with a void at $x = l$.

and using Eq. (43), we get

$$\frac{\dot{v}_v}{\eta} = -\Omega\phi(l) = i'_{vd}(t) \tag{48}$$

so that we can indeed track the void length by monitoring the voltage v_v in the equivalent circuit, as

$$l_{vd}(t) = v_v(t)/\eta. \tag{49}$$

This equivalent circuit can be simplified somewhat using simple circuit transformations to get the circuit shown in Fig. 12, and then again into the final form in Fig. 13. Finally, in case the void has nucleated at the near end of the line, i.e., at $x = 0$, then the same analysis provides the equivalent circuit diagram in Fig. 14.

Once these equivalent circuits for individual lines are used in the context of a simulation of a multi-line tree or for multiple trees in a larger power grid, the impact of void growth on line resistance, via Eq. (19), and therefore on branch currents must be taken into account. This can be done by customization of the overall circuit simulation, in order to recompute the currents (j_k and therefore I_{Sk}) for every line whenever a significant change of resistance has occurred. These details are beyond the scope of this paper.

Fig. 14. Equivalent circuit for a line with a void at $x = 0$.

5. Lumped equivalent circuit

As mentioned earlier, transmission lines can be solved analytically, but that is just as complex as solving the original Korhonen's equation analytically. Transmission lines can also be simulated using existing tools like HSPICE®, but this can be expensive, and the detailed high-frequency analysis performed by the simulator is not needed for the slow EM system. Instead, and as is often done in practice, RC transmission lines can be approximated, with very good accuracy, by a *lumped* RC line, as shown in Fig. 15. The lumped line is composed of N segments, each of which is a π-RC approximation of a short segment of the original line. A segment of the line of length δ_k, corresponding to a total resistance of $R_k = \delta_k r_k$ and total capacitance of $C_k = \delta_k c_k$, is approximated by the combination of a single (lumped) series resistor R_k and two (lumped) shunt capacitors to ground of value $C_k/2$ each. Internal nodes of the line end up with a capacitor C_k each, while the two line terminal nodes get only $C_k/2$ each. Thus, if line k has length l_k, then $\delta_k = l_k/N$ and the line is characterized by the lumped-element values

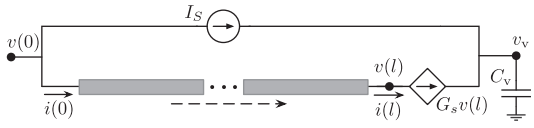

Fig. 12. Equivalent circuit (version 2) for a line with a void at $x = l$.

$$R_k = \frac{k_b T \delta_k}{D_k a_k \psi} \quad \text{and} \quad C_k = \frac{a_k \delta_k \psi}{B\Omega}. \tag{50}$$

Note again that capacitance is representative of the volume of a metal region (in this case the segment volume $a_k\delta_k$) and represents the capacity of that region to contain metal atoms. The HSPICE® user guide [25] (pg. 203) recommends as default a number of $N = 20$ segments for lumped element RC approximations of transmission lines. Beyond this, it says, one gets negligible improvement for the increased simulation time. It is interesting that this guidance is independent of the line length. We have found $N = 20$ to work very well in practice, as also observed in [13] where an even smaller N of 16 was used. With this, the equivalent circuit for a single isolated metal branch in the nucleation phase becomes as shown in Fig. 16. Similarly, the corresponding circuits for lines with voids are shown in Figs. 17 and 18. These lumped equivalent circuits can then be interconnected in the same way as the original metal branches, possibly combined with junction capacitors (at non-voided junctions), in order to represent the whole interconnect tree.

6. Validation

We will give a number of simulation results that demonstrate the validity of this approach, covering both the void nucleation phase and the void growth phase.

6.1. Nucleation phase

We will describe the implementation of the above approach and give comparisons to exact solutions from [3,17]. We have developed a generic SPICE sub-circuit, an example of which is shown in Fig. 21. The figure shows a sub-circuit type consisting of 20 π-RC segments, called PIRC20, which makes use of another sub-circuit for a single π-RC link, called pirc_seg and included at the bottom of Fig. 21. The PIRC20 sub-circuit captures the contributions of a single metal line to the equivalent circuit of an interconnect tree, based on the equivalent circuit shown in Fig. 16. This sub-circuit can be used to construct the equivalent circuit for any given interconnect tree, by connecting multiple instances of the PIRC20 sub-circuit in the same way as the metal branches are connected. Additional capacitors to ground may then be added for any junctions whose volumes are deemed to be significant. An example is shown in the SPICE circuit description given in Fig. 19, for the 4-line interconnect tree with a plus-junction shown in Fig. 20. Circuit simulation can then be

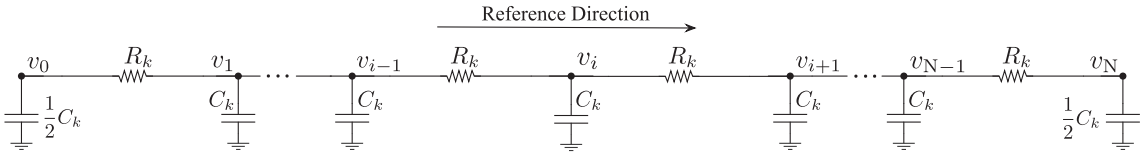

Fig. 15. Lumped RC approximation of a distributed transmission line.

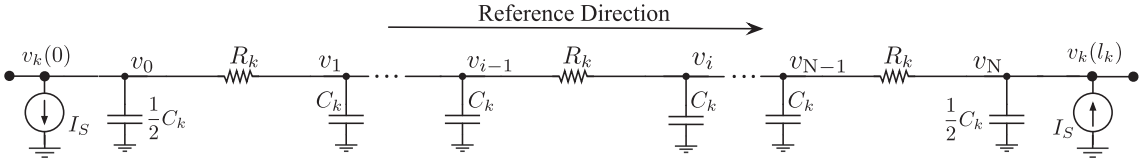

Fig. 16. Contribution of a metal branch to the tree equivalent circuit, in the nucleation phase.

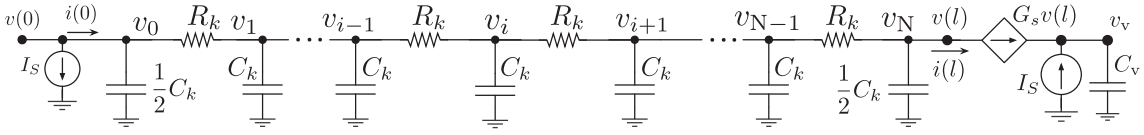

Fig. 17. Lumped equivalent circuit for a line with a void at $x = l$.

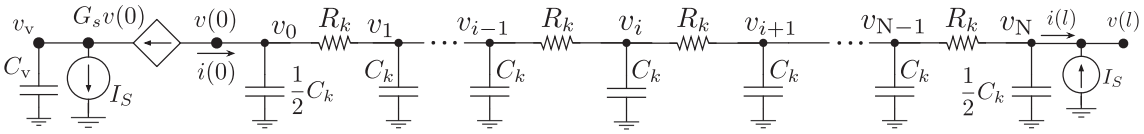

Fig. 18. Lumped equivalent circuit for a line with a void at $x = 0$.

```
**********************************************************
* Circuit: Equivalent circuit for a 4-line tree.
************************ Main Circuit Netlist **********
.PARAM TEMP = 400 Kb = 1.380649E-23 BULKMOD = 3.00E+10
+ PSI = 1E-2 XSI = 1E-06 QSTAR = 1.60E-18
+ OMEGA = 1.66E-29 RHO = '3E-8*(1+0.0039*(TEMP-400))'
+ DIFF0 = 5.2E-5 EA = 1.602176634E-19 HEIGHT = 1E-6

.PARAM sigma0 = 0
.include pirc20.sp

X1 N1 N0 PIRC20 Length=150u Width=1u JK= 1E9 DIFF0=DIFF0
X2 N0 N2 PIRC20 Length= 30u Width=1u JK=-2E9 DIFF0=DIFF0
X3 N0 N3 PIRC20 Length=250u Width=1u JK=-4E9 DIFF0=DIFF0
X4 N4 N0 PIRC20 Length= 50u Width=1u JK= 3E9 DIFF0=DIFF0

.IC N0=sigma0 N1=sigma0 N2=sigma0 N3=sigma0 N4=sigma0

.OPTION INGOLD            $ For scientific notation.
.PRINT TRAN V(N0)
.TRAN 86400 315360000     $ Time steps of 1 day.

.END
**********************************************************
```

Fig. 19. SPICE equivalent circuit for a 4-line interconnect tree.

applied to the circuit to find all voltages, therefore all stresses.

The exact solution can be found analytically in certain special cases. For the simple case of a single isolated line, the exact solution is available from both [3,17], as

$$\sigma(x,t) = \sigma_0 - \frac{q^* \rho j l}{\Omega}\left(\frac{1}{2} - \frac{x}{l} - 4\sum_{n=0}^{\infty}\frac{1}{s_n^2} r_{x,t}(n)\right), \tag{51}$$

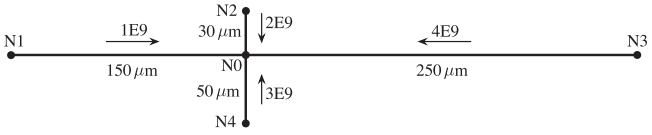

Fig. 20. Layout for a 4-line configuration at a plus-junction.

```
********************* Start Sub-circuit for PIRC20 *********
* NOTE: The way you call this SUBCKT determines the reference
* direction for current density JK. If "X1 N1 N2 PIRC20",
* then the reference direction is N1->N2.
*
.SUBCKT PIRC20 N00 NNN Length=100u Width=1u JK=1E9 DIFF0=52u

.PARAM NSEG = 20  $There are 20 segments in this sub-circuit.
.PARAM SEGLEN = 'Length/NSEG'
.PARAM DIFF = 'DIFF0*EXP(-EA/(Kb*TEMP))'
.PARAM RK = 'Kb*TEMP*SEGLEN/(DIFF*Width*HEIGHT*PSI)'
.PARAM CK = 'PSI*SEGLEN*Width*HEIGHT/(BULKMOD*OMEGA)'
.PARAM IS = 'XSI*PSI*DIFF*QSTAR*RHO*Width*HEIGHT/
+ (Kb*TEMP*OMEGA)*JK'

************* Start of Junction at 0 ********
IS0 N00 GND IS

************* End of Junction at 0; Start of RC-Chain  *****
XRC01 N00 N01 pirc_seg Rval=RK Cval=CK
.IC N01=sigma0
XRC02 N01 N02 pirc_seg Rval=RK Cval=CK
.IC N02=sigma0
XRC03 N02 N03 pirc_seg Rval=RK Cval=CK
.IC N03=sigma0
XRC04 N03 N04 pirc_seg Rval=RK Cval=CK
.IC N04=sigma0
XRC05 N04 N05 pirc_seg Rval=RK Cval=CK
.IC N05=sigma0
XRC06 N05 N06 pirc_seg Rval=RK Cval=CK
.IC N06=sigma0
XRC07 N06 N07 pirc_seg Rval=RK Cval=CK
.IC N07=sigma0
XRC08 N07 N08 pirc_seg Rval=RK Cval=CK
.IC N08=sigma0
XRC09 N08 N09 pirc_seg Rval=RK Cval=CK
.IC N09=sigma0
XRC10 N09 N10 pirc_seg Rval=RK Cval=CK
.IC N10=sigma0
XRC11 N10 N11 pirc_seg Rval=RK Cval=CK
.IC N11=sigma0
XRC12 N11 N12 pirc_seg Rval=RK Cval=CK
.IC N12=sigma0
XRC13 N12 N13 pirc_seg Rval=RK Cval=CK
.IC N13=sigma0
XRC14 N13 N14 pirc_seg Rval=RK Cval=CK
.IC N14=sigma0
XRC15 N14 N15 pirc_seg Rval=RK Cval=CK
.IC N15=sigma0
XRC16 N15 N16 pirc_seg Rval=RK Cval=CK
.IC N16=sigma0
XRC17 N16 N17 pirc_seg Rval=RK Cval=CK
.IC N17=sigma0
XRC18 N17 N18 pirc_seg Rval=RK Cval=CK
.IC N18=sigma0
XRC19 N18 N19 pirc_seg Rval=RK Cval=CK
.IC N19=sigma0
XRC20 N19 NNN pirc_seg Rval=RK Cval=CK

************* End of RC-Chain; Start of Junction at N ******
ISN GND NNN IS

.ENDS
******************** End of Sub-circuit for PIRC20 **********

********************* Start Sub-circuit for RC-segment *****
.SUBCKT pirc_seg N1 N2 Rval=880K Cval=151m
CapN1 N1 GND 'Cval/2'
Resistor  N1 N2  Rval
CapN2 N2 GND 'Cval/2'
.ENDS
********************* End of Sub-circuit for RC-segment ****
```

Fig. 21. A SPICE sub-circuit for a metal line using 20 π-RC segments.

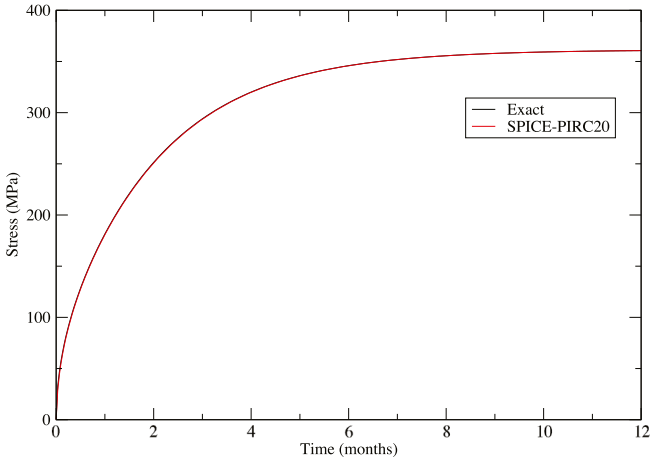

Fig. 22. Stress evolution at the cathode for a single isolated 250 μm long metal line.

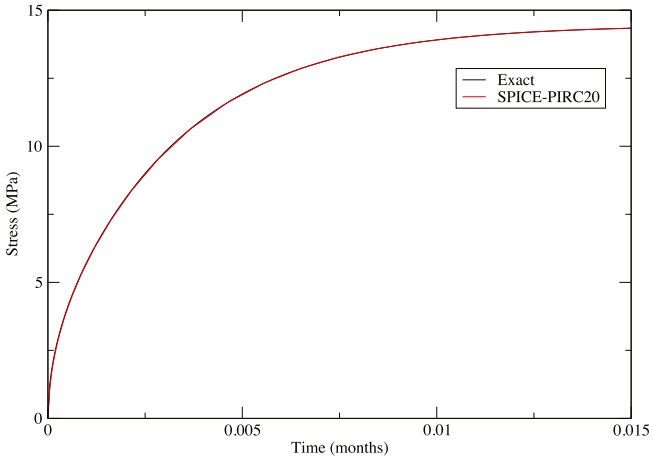

Fig. 23. Stress evolution at the cathode for a single isolated 10 μm long metal line.

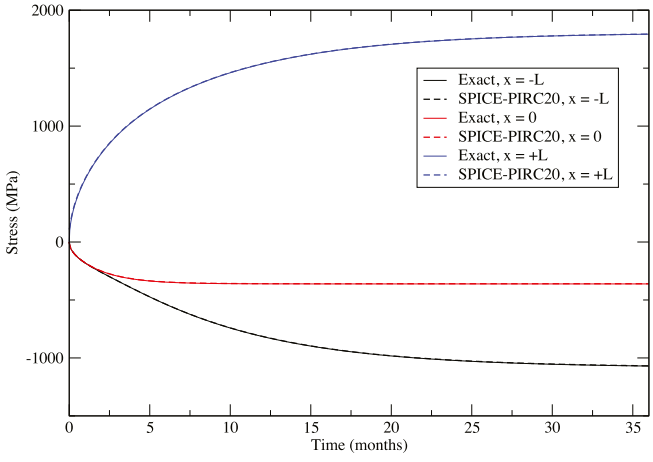

Fig. 24. SPICE v.s. the exact solution for the dotted-I arrangement, with equal widths.

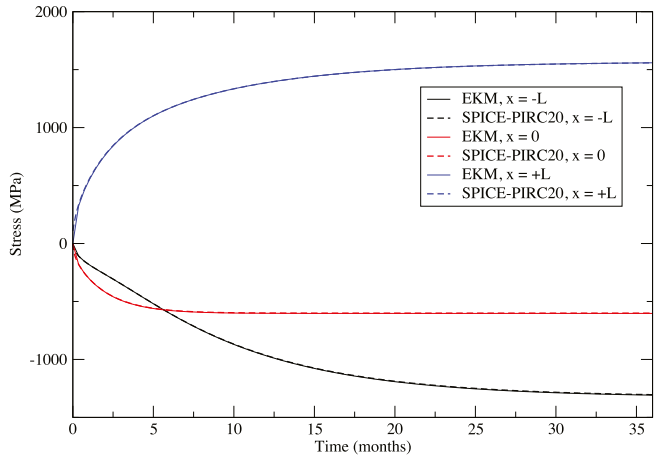

Fig. 25. SPICE v.s. the EKM solution for the dotted-I arrangement, with $w_2 = 2w_1$.

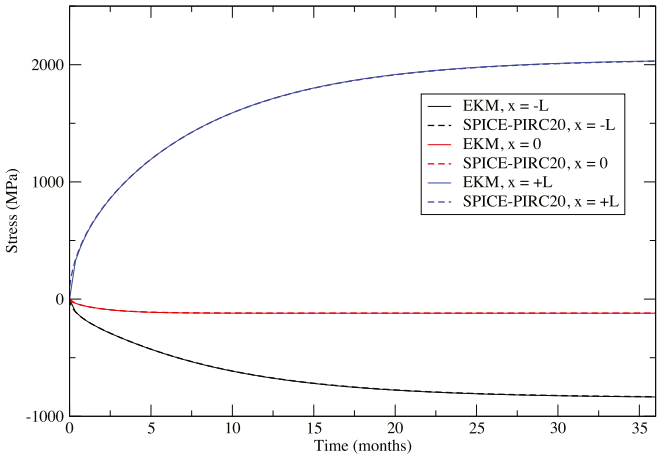

Fig. 26. SPICE v.s. the EKM solution for the dotted-I arrangement, with $w_1 = 2w_2$.

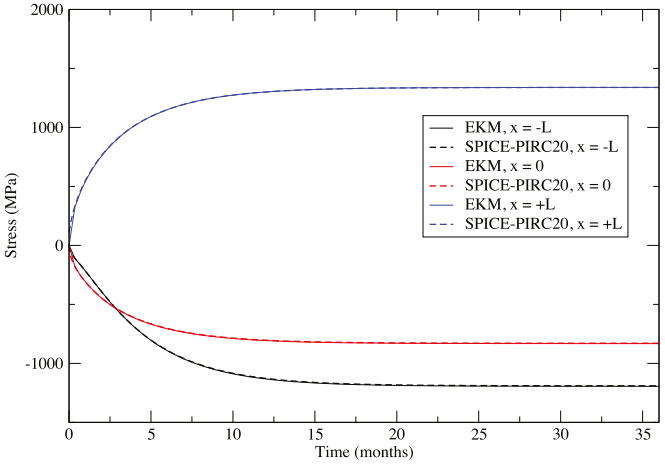

Fig. 27. SPICE v.s. the EKM solution for the dotted-I arrangement, with $w_2 = 2w_1$ and $L_2 = 2L_1$.

```
**********************************************************
* Circuit: Equivalent circuit for a 3-line tree.
************************ Main Circuit Netlist **********
.PARAM TEMP = 400 Kb = 1.380649E-23 BULKMOD = 3.00E+10
+ PSI = 1E-2 XSI = 1E-06 QSTAR = 1.60E-18
+ OMEGA = 1.66E-29 RHO = '3E-8*(1+0.0039*(TEMP-400))'
+ DIFF0 = 5.2E-5 EA = 1.602176634E-19 HEIGHT = 1E-6

.PARAM sigma0 = 0
.include pirc20.sp

X1 N1 N2 PIRC20 Length=100u Width=1u JK= 2E9 DIFF0=DIFF0
X2 N2 N3 PIRC20 Length= 20u Width=2u JK= 1E9 DIFF0=DIFF0
X3 N2 N4 PIRC20 Length=200u Width=3u JK= 3E9 DIFF0=DIFF0

.IC N1=sigma0 N2=sigma0 N3=sigma0 N4=sigma0

.OPTION INGOLD            $ For scientific notation.
.PRINT TRAN V(N1)
.TRAN 86400 315360000     $ Time steps of 1 day.

.END
**********************************************************
```

Fig. 28. A 3-line T-junction test case.

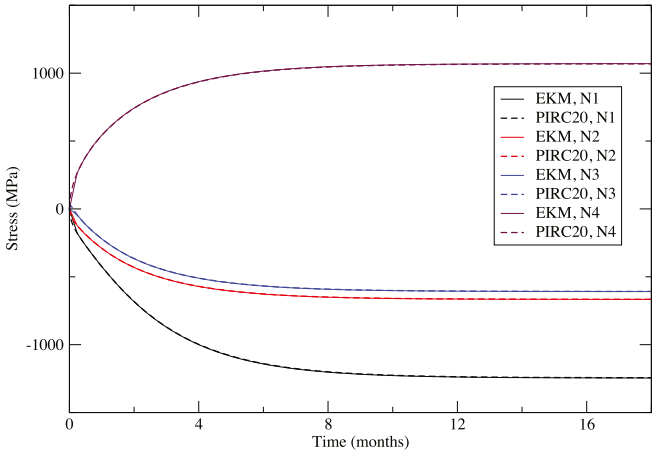

Fig. 29. SPICE v.s. the EKM solution for a 3-line arrangement around a T-junction, using PIRC20.

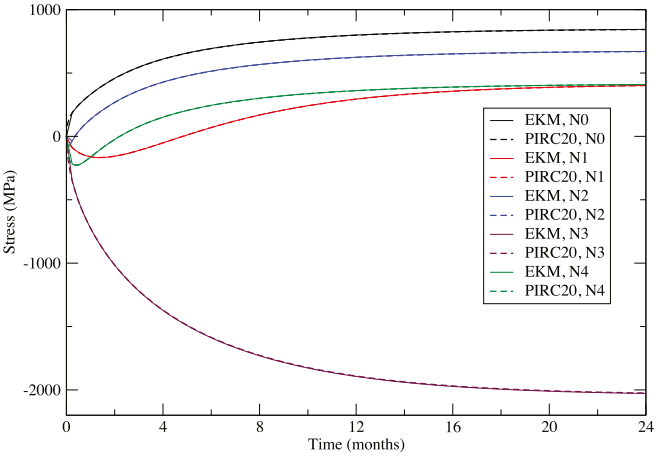

Fig. 30. SPICE v.s. the EKM solution for a 4-line arrangement around a plus-junction, using PIRC20.

```
******************** Start Sub-circuit for PIRC20V0 **********
* NOTE: The way you call this SUBCKT determines the reference
* direction for current density JK. If "X1 N1 N2 PIRC20V0",
* then the reference direction is N1->N2.
*
.SUBCKT PIRC20V0 N00 NNN Length=100u Width=1u JK=1E9 DIFF0=52u

.PARAM NSEG = 20  $There are 20 segments in this sub-circuit.
.PARAM SEGLEN = 'Length/NSEG'
.PARAM DIFF = 'DIFF0*EXP(-EA/(Kb*TEMP))'
.PARAM RK = 'Kb*TEMP*SEGLEN/(DIFF*Width*HEIGHT*PSI)'
.PARAM CK = 'PSI*SEGLEN*Width*HEIGHT/(BULKMOD*OMEGA)'
.PARAM IS = 'XSI*PSI*DIFF*QSTAR*RHO*Width*HEIGHT/
+ (Kb*TEMP*OMEGA)*JK'
.PARAM GS = 'PSI*DIFF*Width*HEIGHT/(Kb*TEMP*DELTA)'
.PARAM CV = 'XSI*PSI*Width*HEIGHT/(OMEGA*ETA)'

************* Start of Junction at 0 ********
CV0 NV0 GND CV
IS0 NV0 GND IS
GS0 N00 NV0 VCCS N00 GND GS
.IC NV0 = 0

************* End of Junction at 0; Start of RC-Chain  *****
XRC01 N00 N01 pirc_seg Rval=RK Cval=CK
XRC02 N01 N02 pirc_seg Rval=RK Cval=CK
XRC03 N02 N03 pirc_seg Rval=RK Cval=CK
XRC04 N03 N04 pirc_seg Rval=RK Cval=CK
XRC05 N04 N05 pirc_seg Rval=RK Cval=CK
XRC06 N05 N06 pirc_seg Rval=RK Cval=CK
XRC07 N06 N07 pirc_seg Rval=RK Cval=CK
XRC08 N07 N08 pirc_seg Rval=RK Cval=CK
XRC09 N08 N09 pirc_seg Rval=RK Cval=CK
XRC10 N09 N10 pirc_seg Rval=RK Cval=CK
XRC11 N10 N11 pirc_seg Rval=RK Cval=CK
XRC12 N11 N12 pirc_seg Rval=RK Cval=CK
XRC13 N12 N13 pirc_seg Rval=RK Cval=CK
XRC14 N13 N14 pirc_seg Rval=RK Cval=CK
XRC15 N14 N15 pirc_seg Rval=RK Cval=CK
XRC16 N15 N16 pirc_seg Rval=RK Cval=CK
XRC17 N16 N17 pirc_seg Rval=RK Cval=CK
XRC18 N17 N18 pirc_seg Rval=RK Cval=CK
XRC19 N18 N19 pirc_seg Rval=RK Cval=CK
XRC20 N19 NNN pirc_seg Rval=RK Cval=CK

************* End of RC-Chain; Start of Junction at N ******
ISN GND NNN IS

.ENDS
****************** End of Sub-circuit for PIRC20V) *********

******************** Start Sub-circuit for RC-segment *****
.SUBCKT pirc_seg N1 N2 Rval=880K Cval=151m
CapN1 N1 GND 'Cval/2'
Resistor  N1 N2  Rval
CapN2 N2 GND 'Cval/2'
.ENDS
******************** End of Sub-circuit for RC-segment *****
```

Fig. 31. A SPICE sub-circuit for a metal line with a void at $x = 0$ using 20 π-RC segments.

```
******************** Start Sub-circuit for PIRC20VN **********
* NOTE: The way you call this SUBCKT determines the reference
* direction for current density JK. If "X1 N1 N2 PIRC20VN",
* then the reference direction is N1->N2.
*
.SUBCKT PIRC20VN N00 NNN Length=100u Width=1u JK=1E9 DIFF0=52u

.PARAM NSEG = 20 $There are 20 segments in this sub-circuit.
.PARAM SEGLEN = 'Length/NSEG'
.PARAM DIFF = 'DIFF0*EXP(-EA/(Kb*TEMP))'
.PARAM RK = 'Kb*TEMP*SEGLEN/(DIFF*Width*HEIGHT*PSI)'
.PARAM CK = 'PSI*SEGLEN*Width*HEIGHT/(BULKMOD*OMEGA)'
.PARAM IS = 'XSI*PSI*DIFF*QSTAR*RHO*Width*HEIGHT/
+ (Kb*TEMP*OMEGA)*JK'
.PARAM GS = 'PSI*DIFF*Width*HEIGHT/(Kb*TEMP*DELTA)'
.PARAM CV = 'XSI*PSI*Width*HEIGHT/(OMEGA*ETA)'

************* Start of Junction at 0 ********
IS0 N00 GND IS

************* End of Junction at 0; Start of RC-Chain  *****
XRC01 N00 N01 pirc_seg Rval=RK Cval=CK
XRC02 N01 N02 pirc_seg Rval=RK Cval=CK
XRC03 N02 N03 pirc_seg Rval=RK Cval=CK
XRC04 N03 N04 pirc_seg Rval=RK Cval=CK
XRC05 N04 N05 pirc_seg Rval=RK Cval=CK
XRC06 N05 N06 pirc_seg Rval=RK Cval=CK
XRC07 N06 N07 pirc_seg Rval=RK Cval=CK
XRC08 N07 N08 pirc_seg Rval=RK Cval=CK
XRC09 N08 N09 pirc_seg Rval=RK Cval=CK
XRC10 N09 N10 pirc_seg Rval=RK Cval=CK
XRC11 N10 N11 pirc_seg Rval=RK Cval=CK
XRC12 N11 N12 pirc_seg Rval=RK Cval=CK
XRC13 N12 N13 pirc_seg Rval=RK Cval=CK
XRC14 N13 N14 pirc_seg Rval=RK Cval=CK
XRC15 N14 N15 pirc_seg Rval=RK Cval=CK
XRC16 N15 N16 pirc_seg Rval=RK Cval=CK
XRC17 N16 N17 pirc_seg Rval=RK Cval=CK
XRC18 N17 N18 pirc_seg Rval=RK Cval=CK
XRC19 N18 N19 pirc_seg Rval=RK Cval=CK
XRC20 N19 NNN pirc_seg Rval=RK Cval=CK

************* End of RC-Chain; Start of Junction at N ******
GSN NNN NVN VCCS NNN GND GS
ISN GND NVN IS
CVN NVN GND CV
.IC NVN = 0

.ENDS
****************** End of Sub-circuit for PIRC20VN *********

******************** Start Sub-circuit for RC-segment *****
.SUBCKT pirc_seg N1 N2 Rval=880K Cval=151m
CapN1 N1 GND 'Cval/2'
Resistor  N1 N2  Rval
CapN2 N2 GND 'Cval/2'
.ENDS
******************** End of Sub-circuit for RC-segment ****
```

Fig. 32. A SPICE sub-circuit for a metal line with a void at $x = l$ using 20 π-RC segments.

where $s_n = (2n + 1)\pi$,

$$r_{x,t}(n) = cos\left(s_n\frac{x}{l}\right)exp\left(-s_n^2\frac{\kappa t}{l^2}\right) \tag{52}$$

and $\kappa = DB\Omega/(k_bT)$, which has units of m^2/s, while l is the line length as usual. This specific form of the solution follows the expression[3] used in [17]. For the case of a Copper line of width 1 μm, height 1 μm and length 250 μm, discretized into 20 segments as in PIRC20, at $T = 400$ K and carrying a current density of 1×10^9 A/m^2, the circuit parameters turn out to be (in round numbers),

$$R_k = 528\,k\Omega, \quad C_k = 251\,mF \quad \text{and} \quad I_S = 69\,\mu A, \tag{53}$$

based on the physical parameters in Table 1. Setting the junction volumes to zero, the comparison of the exact solution at the cathode junction to that from the SPICE solution using PIRC20 is shown in Fig. 22, and the agreement is excellent. This test was repeated for line lengths of 150 μm, 80 μm, 40 μm and 10 μm, and the agreement is excellent in every case, as in the 10 μm case shown in Fig. 23. Throughout the following, all test runs will be based on zero junction volumes.

We also tested the case of an interconnect tree composed of two identical lines in a dotted-I arrangement, against our implementation of the exact solution based on the analysis[4] in [17]. Each line is $L = 250$ μm long and 1 μm wide, with both reference directions to the right, carrying $j_1 = 1 \times 10^9$ A/m^2 in line 1 and $j_2 = 3 \times 10^9$ A/m^2 in line 2, at 400 K. The comparison at the three junctions is shown in Fig. 24, showing excellent

[3] The sign difference (after the σ_0 term) relative to Eq. (3) in [17] is because they've assumed that the reference direction for the current is opposite to that of the x distance variable, as can be seen by comparing their Eq. (1) to our Eq. (12).

[4] Here too, a reversal of the signs of the G_1 and G_2 terms in Eq. (6) of [17] is applied, for a proper comparison.

```
************************************************************
* Equivalent circuit for a 250um line using PIRC20V0.
************************************************************
.PARAM TEMP = 400 Kb = 1.380649E-23 BULKMOD = 3.00E+10
+ PSI = 1E-2 XSI = 1E-06 QSTAR = 1.60E-18
+ OMEGA = 1.66E-29 RHO = '3E-8*(1+0.0039*(TEMP-400))'
+ DIFF0 = 5.2E-5 EA = 1.602176634E-19 HEIGHT = 120E-9
+ DELTA = 1E-9 ETA=1E+9

.PARAM sigma0 = 0
.include pirc20v0.sp

X1 N1 N2 PIRC20V0 Length=250u Width=1u JK=-2E9 DIFF0=DIFF0

.IC N1=sigma0 X1.N01=sigma0 X1.N02=sigma0 X1.N03=sigma0
+ X1.N04=sigma0 X1.N05=sigma0 X1.N06=sigma0 X1.N07=sigma0
+ X1.N08=sigma0 X1.N09=sigma0 X1.N10=sigma0 X1.N11=sigma0
+ X1.N12=sigma0 + X1.N13=sigma0 X1.N14=sigma0
+ X1.N15=sigma0 X1.N16=sigma0 + X1.N17=sigma0
+ X1.N18=sigma0 X1.N19=sigma0 N2=sigma0

.OPTION INGOLD           $ For scientific notation.
.PRINT TRAN V(X1.N01)
.TRAN 86400 189216000    $ Time steps of 1 day.

.END
************************************************************
```

Fig. 33. SPICE description for a single-line circuit with a void at $x = 0$.

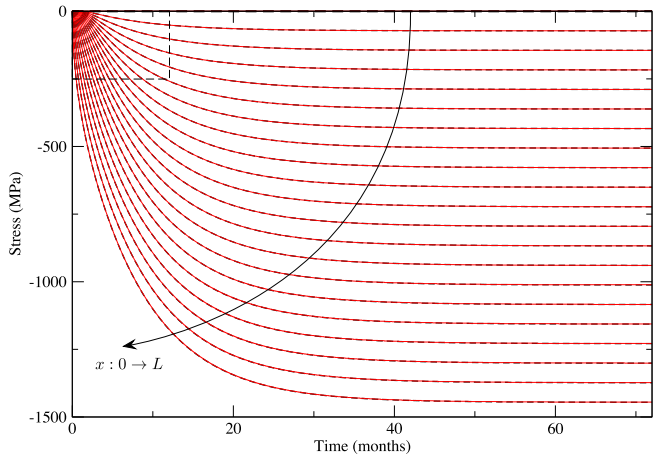

Fig. 34. Stress evolution in a line with a void at $x = 0$, starting with zero stress everywhere. Results from SPICE using PIRC20V0 are compared to the exact solution at multiple points along the $[0, L]$ line span.

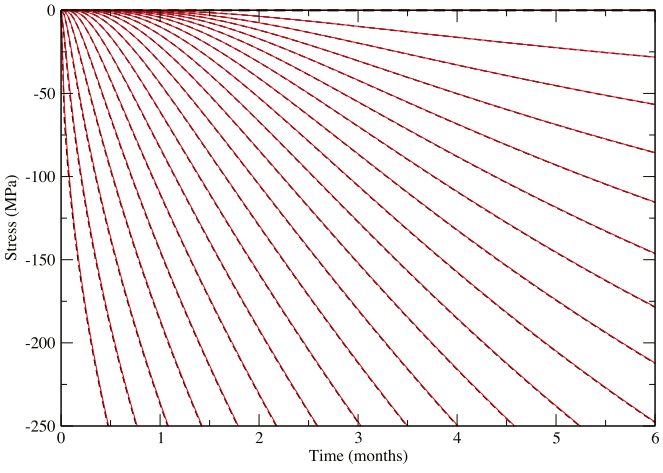

Fig. 35. An expanded view of the rectangular area at the top left of the graph in Fig. 34.

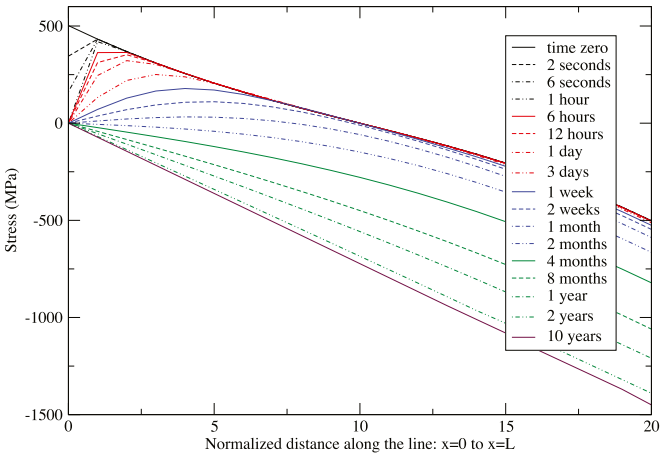

Fig. 36. Stress profile along the length of the line during the void growth phase, for a void at $x = 0$.

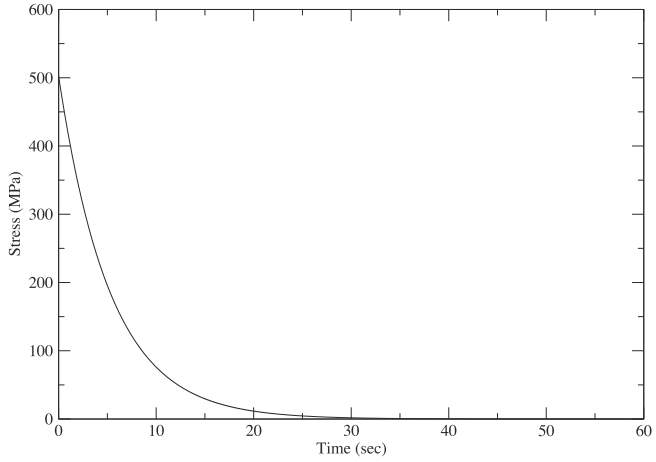

Fig. 37. Fast stress decay at the void at $x = 0$, using SPICE with PIRC20V0.

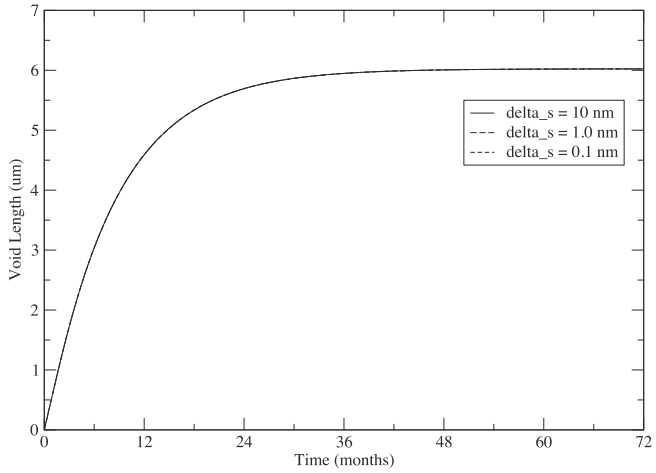

Fig. 38. Sensitivity to the void surface thickness, for a 250 μm long, 1 μm wide line, with $j = 1 \times 10^9 \mathrm{A}/m^2$.

accuracy. We also tested the case of unequal widths, keeping w_1 at 1 μm while setting $w_2 = 2w_1$ and keeping everything else the same. In this case, in the absence of an exact solution, we compared to the EKM implementation [4] and the results are again excellent as shown in

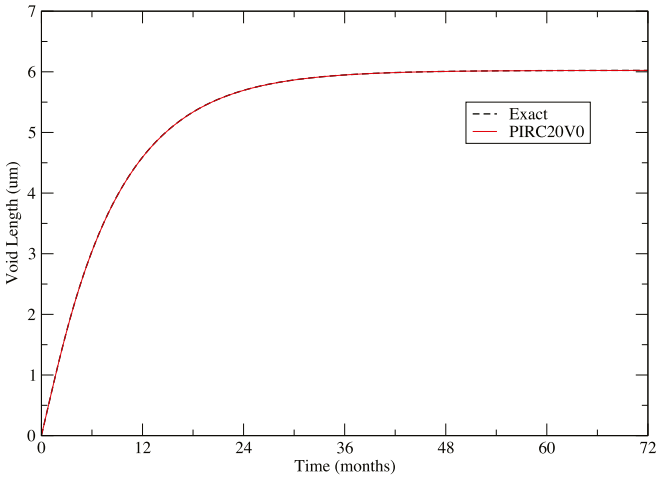

Fig. 39. Void growth for a 250um line.

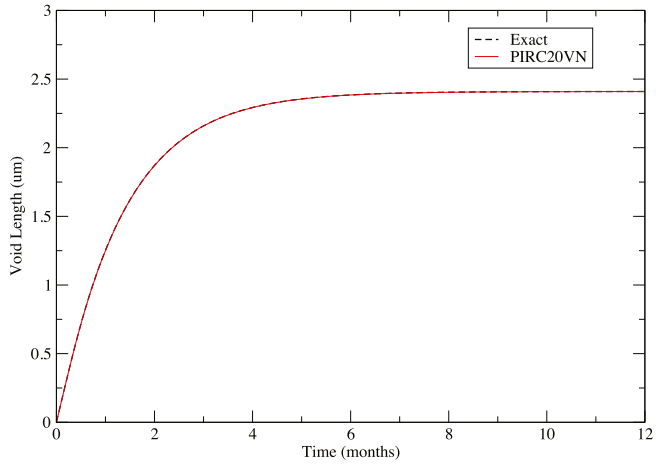

Fig. 40. Void growth for a 100um line.

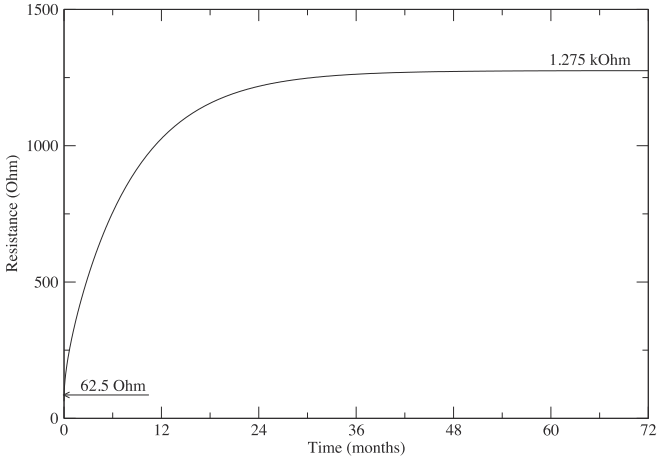

Fig. 41. Resistance increase for a 250um line with a void.

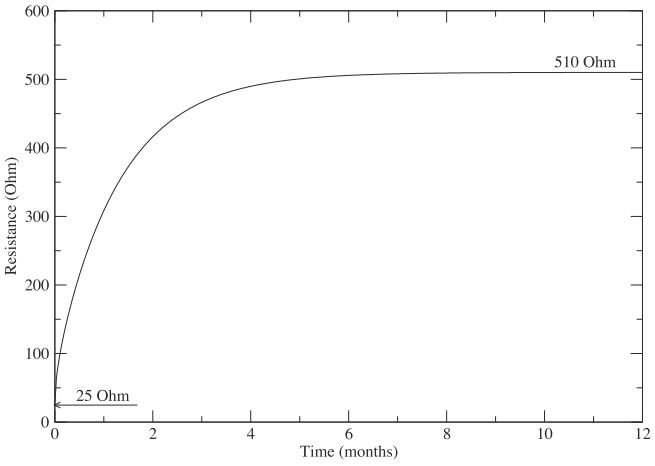

Fig. 42. Resistance increase for a 100um line with a void.

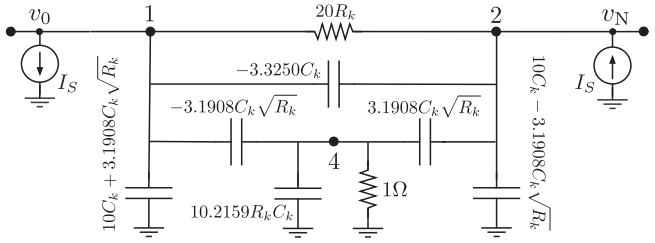

Fig. 43. Contribution of a branch to the tree equivalent circuit using the PACTN4 reduced order model.

```
********************* Start Sub-circuit for PACTN4 *********
* NOTE: The way you call this SUBCKT determines the reference
* direction for the current density JK. If "X1 N1 N2 PACTN4",
* then the reference direction is N1->N2.
*
.SUBCKT PACTN4 N00 NNN Length=100u Width=1u JK=1E9 DIFF0=52u

.PARAM NSEG = 20 $There are 20 segments in this sub-circuit.
.PARAM SEGLEN = 'Length/NSEG'
.PARAM DIFF = 'DIFF0*EXP(-EA/(Kb*TEMP))'
.PARAM RK = 'Kb*TEMP*SEGLEN/(DIFF*Width*HEIGHT*PSI)'
.PARAM CK = 'PSI*SEGLEN*Width*HEIGHT/(BULKMOD*OMEGA)'
.PARAM IS = 'XSI*PSI*DIFF*QSTAR*RHO*Width*HEIGHT/
+ (Kb*TEMP*OMEGA)*JK'

************* Start of Junction at 0 ********
IS0 N00 GND IS

************* End of Junction at 0; Start of RC-Chain  *****
* This PACT-reduced circuit replaces the 20-segment PIRC20.
*
C10 N00 GND '10*CK + 3.1907667152466*CK*SQRT(RK)'
C20 NNN GND '10*CK - 3.1907667152466*CK*SQRT(RK)'
R12 N00 NNN '20*RK'
C12 N00 NNN '-3.3250*CK'
C14 N00 N04 '-3.1907667152466*CK*SQRT(RK)'
C24 NNN N04 ' 3.1907667152466*CK*SQRT(RK)'
C40 N04 GND '10.2158645472653*RK*CK'
R40 N04 GND 1

************* End of RC-Chain; Start of Junction at N ******
ISN GND NNN IS

.ENDS
********************* End of Sub-circuit for PACTN4 *********
```

Fig. 44. A SPICE reduced sub-circuit for a metal line using 20 π-RC segments.

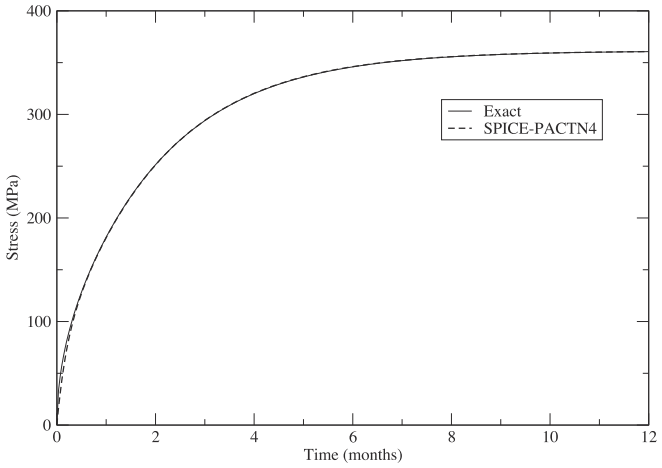

Fig. 45. Stress evolution at the cathode for a *reduced* single isolated metal line.

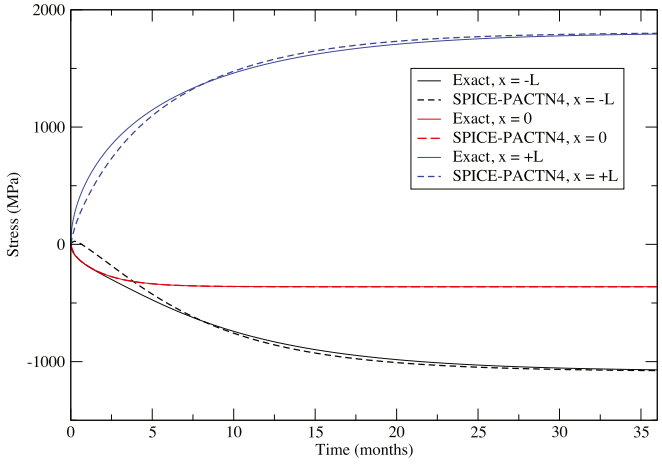

Fig. 46. SPICE v.s. the exact solution for the *reduced* dotted-I arrangement, with equal widths.

Fig. 25. The opposite case comparison, with $w_1 = 2w_2 = 1$ μm is shown in Fig. 26. And, as yet another variation on this circuit, we show the comparison for the case when $w_2 = 2w_1 = 2$ μm with $L_2 = 2L_1 = 250$ μm in Fig. 27.

Another interesting case is the 3-line T-junction arrangement, given in the SPICE description in Fig. 28, for which the comparison to EKM is shown in Fig. 29. Finally, for the plus-junction described in the netlist in Fig. 19 and shown in the layout diagram in Fig. 20, the comparison to EKM is shown in Fig. 30.

6.2. Void growth phase

We will describe the implementation of the above approach and give comparisons to exact solutions from [26]. We have developed a generic SPICE sub-circuit, an example of which is shown in Fig. 31 for a void at $x = 0$ and Fig. 32 for a void at $x = l$. The figures show two sub-circuit types consisting of 20 π-RC segments each, called PIRC20V0 and PIRC20VN, which make use of another sub-circuit for a single π-RC link, called pirc_seg and included in the figures. These sub-circuits capture the contributions of a single (voided) metal line to the equivalent circuit of an interconnect tree, based on the equivalent circuits shown in Figs. 17 and 18. One can construct the equivalent circuit for any given interconnect tree by connecting multiple instances of these PIRC20V0 and PIRC20VN sub-circuits, along with the PIRC20 sub-circuits shown earlier for any un-voided line, in the same way as the metal branches are connected. Additional capacitors to ground may then be added for any junctions whose volumes are deemed to be significant. Circuit simulation can then be applied to the circuit to find all voltages, therefore all stresses and void lengths.

We will explore the transient stress response in the line as well as the void growth evolution over time. When possible, we will compare to exact solutions, which can be found analytically in certain special cases [26]. For the simple case of a single isolated line, and assuming that a void has just nucleated at $x = 0$ at time zero, the condition $\sigma(0,t) = 0, \forall t$ is enforced as a boundary condition in [26]. They also assume that the initial stress throughout the line is negligible, i.e., $\sigma(x,0) = 0, \forall\, x$, an assumption that is presumably made in order to be able to get an analytical solution. With this setup, the exact solution is given by[5]

$$\sigma(x,t) = \frac{q^* \rho j l}{\Omega}\left(\frac{x}{l} + 2\sum_{n=1}^{\infty}\frac{(-1)^n}{c_n^2}\, s_{x,t}(n)\right), \tag{54}$$

where $c_n = (2n-1)\pi/2$,

$$s_{x,t}(n) = sin\left(\frac{c_n x}{l}\right) exp\left(-c_n^2 \frac{\kappa t}{l^2}\right) \tag{55}$$

with $\kappa = DB\Omega/(k_b T)$ as before, while l is the line length. For our test case, we specified a Copper line of width 1 μm and length 250 μm, discretized into 20 segments as in PIRC20V0, at $T = 400$ K and carrying a current density of -2×10^9 A/m^2, as shown in the SPICE circuit description in Fig. 33. Notice that there are additional physical constants (DELTA for δ_s and ETA for η) that have to be specified up-front. Also, a detailed. IC statement is needed to set up the correct initial profile of stress in the line at the time of voiding, which in this case was set to zero so as to allow a fair comparison with [26]. Having set the junction volume (at $x = l$) to zero, we compared the time evolution of $\sigma(x,t)$ for the *SPICE* solution v.s. the exact solution, at every node of the RC chain, i.e., at $x = 0, \delta_k, 2\delta_k, \ldots, l_k$, where $\delta_k = l_k/20$. The comparison is shown in Fig. 34, where the rectangular area in the top-left corner is expanded and shown in Fig. 35. The SPICE solution is shown as the solid red curves while the exact solution is the dashed black curves, and the agreement is clearly excellent. Throughout the following, all test runs will be based on zero junction volumes.

Using our approach, we can handle more realistic cases, such as when the initial stress in the line is non-zero, and where a non-zero residual thermal stress can be included. For example, for the same 250μm line, we first simulated the line before voiding, saved the state at the time of voiding and then applied that state as the initial stress profile during the subsequent simulation of the voided line. The result is shown in Fig. 36, where we have shown the profile of the stress along the length of the line at different points in time. Notice that the stress at $x = 0$ drops very quickly from $\sigma(0,0) = 500$ MPa to a constant $\sigma(0,t) = 0$ over a period of seconds, while the rest of the line (at 5% of the line length away from the void, and beyond) takes months or years to reach its steady state. This fast transient behavior of the stress at $x = 0$ is shown in Fig. 37 and testifies to the very high initial flux at the void surface due to the high initial stress gradient σ_{crit}/δ_s there. Fig. 38 shows the void growth for a single line with δ_s set to 10 nm, 1 nm and 0.1 nm. It is clear that the solution is not sensitive to the choice of δ_s in this range, as one would like to see in fact. We have found that this property of this model [18] remains valid over the wide range of 1pm $\leq \delta_s \leq 1\mu$m.

Looking next at the void length over time, we will compare to the exact solution provided in [26], as

[5] The sign difference (before the first term) relative to Eq. (8) in [26] is because they've assumed that the reference direction for the current is opposite to that of the x distance variable, as can be seen by comparing their Eq. (1) to our Eq. (12).

$$\frac{l_{vd}}{l_{vd,sat}} = 1 + 4\sum_{n=1}^{\infty} \frac{(-1)^n}{c_n^3} exp\left(-c_n^2 \frac{\kappa t}{l^2}\right), \tag{56}$$

where $l_{vd,sat} = q^*\rho|j|l^2/(2B\Omega)$ from [26]. The comparison to SPICE using PIRC20V0 for the same 250 μm line with $j = -$ 2E9A/m^2 is shown in Fig. 39. Another comparison is also shown for a 100μm line carrying $j =$ 5E9A/m^2, with the void at the far end of the line, so we use PIRC20VN, and the results are in Fig. 40. The agreement is excellent in both cases. Finally, the resistance increase over time for these two lines is shown in Figs. 41 and 42, based on Eq. (19).

6.3. Reduced line

Given the PIRC-20 lumped model, we can apply the PACT [27] model-order reduction approach, as described in [28] to get the generic scalable compact model shown in Fig. 43, which we use to replace PIRC20, resulting in what we call the PACTN4 sub-circuit, given in Fig. 44. For the same 250 μm line considered in Fig. 22, the comparison to the PACTN4 reduced line is shown in Fig. 45. Comparisons are also given for the dotted-I arrangement, with equal widths, in Fig. 46, showing some degradation at the fast transients, but otherwise quite acceptable. The major advantage of using the PACT transformation is to reduce the number of nodes in the system, thus allowing one to handle very large interconnect trees. If the interconnect tree has n junctions and m branches (recall that in a tree, $m = n - 1$) then using PIRC20 would generate an equivalent circuit with $(20n - 19)$ nodes while, for PACTN4 the resulting circuit has only $(2n - 1)$ nodes, which is a $\approx 10\times$ reduction. In other words, this reduction allows the analysis of $10\times$ larger interconnect trees. This clearly shows the benefit of using the equivalent circuits approach! It would have been very difficult to imagine, looking only at the stress equations, that this kind of reduction of the problem size is at all possible.

7. Conclusion

We have demonstrated a deep connection between the EM-induced stress-flux dynamics in metal lines and the voltage-current dynamics in RC circuits. Effectively, the atomic transport in an interconnect network behaves in the same way as the electronic current in the metal lines; they obey the same circuit laws. We have done this for both the void nucleation phase and the void growth phase, and provided sample SPICE sub-circuits that can be used to generate a large RC network for any given metal interconnect network. Simulation results demonstrate excellent agreement between the two "worlds" of stress and voltage.

CRediT authorship contribution statement

Sole Author **Farid N. Najm**: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Resources, Data Curation, Writing - Original Draft, Writing - Review & Editing, Visualization, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

The author acknowledges the many useful discussions with Dr. Valeriy Sukharev of *Siemens EDA* (formerly Mentor Graphics) that have helped improve this manuscript.

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