Experimental Validation of a Novel Methodology for Electromigration Assessment in On-Chip Power Grids

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***Abstract*—A recently proposed theoretical methodology for the assessment of the electromigration (EM) induced IR-drop degradation in on-chip power/ground grids has been validated by means of measurements performed on real silicon. A voltage tapping technique was employed for the direct measurement of voltage variations at 162 nodes of the power net, stressed with 10 mA constant source current at an elevated temperature of 350 °C. A voltage drop between cathode and anode pads exceeding a specified threshold was considered as a failure. Times-to-failure (TTF) was measured on 19 packaged test grids and used for computing the mean TTF (MTTF). The EM-induced voltage degradation in this grid was also analyzed with an assessment methodology based on a simulation of stress evolution everywhere in the grid, resulting in a voiding in some of grid branches and corresponding resistance increase. A set of voiding compact models for different grid segments was developed and used in the simulations. The stochastic nature of the EM phenomenon was captured by introducing random distributions of atomic diffusivities and critical stresses across the grid and iterating them with Monte Carlo loops. A good fit between the measured voltage evolution kinetics at different grid nodes and that predicted by simulation, and the good agreement between measured and simulated failure distributions can be considered as the ever first experimental validation of this EM assessment methodology for on-chip power/ground (p/g) grids.**

***Index Terms*—Diffusivity, electromigration (EM), failure, grain boundary (GB), mean-time-to-failure (MTTF), p/g grid, partial differential equation (PDE), stress, test chip, voiding.**

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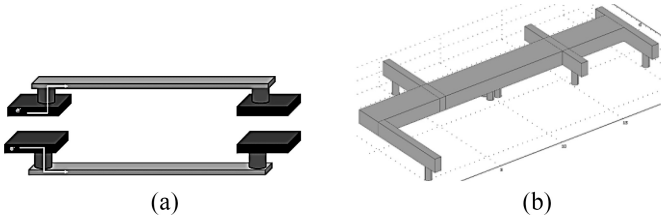
I. Introduction

AN ACCURATE assessment of electromigration (EM)-induced failure is an important step in helping to get a realistic estimation of the lifetime of semiconductor chips. Besides this practical importance, it is also a complex and interesting scientific problem, which combines a wide range of topics, from materials science, solid-state physics, and the theory of electrical circuits to statistics and probability, making it as a truly multidisciplinary subject. The electric current passing through on-chip interconnect metal segments embedded in a surrounding dielectric moves some of lattice atoms by means of momentum exchange with the conduction electrons. Volumetric deformation accompanying the redistribution of atomic density along the metal segment generates elastic stress due to interaction with the rigid confinement. The gradient of this stress forces atoms to migrate in the direction of the electric current, further affecting the atomic redistribution. The growth of mechanical stress caused by a unidirectional current can cause an evolution of a variety of defects that are inevitably present in the metal bulk, and on the interfaces with metal liners and dielectric barriers. Tensile stress, which is generated near the cathode region of a metal line, can cause growth of the defects characterized by the presence of free surfaces, such as micropores and delamination, leading to void formation. Compressive stress, which is generated in the vicinity of the anode, can cause an extrusion of metal into the surrounding dielectric through the defects in the encapsulating liners, and forms the so-called hillocks. Both these developments can affect the electrical properties of the interconnect [1]. Voiding can result an increase of resistances of individual interconnect segments and even cause an open circuit in the extreme cases. Hillocks can be responsible for shorting to a neighboring conductor. However, this simplistic picture of generation of the EM-induced electrical failures is valid only for individual metal segments with diffusion barriers at both ends preventing atomic exchange between neighboring segments, as shown in Fig. 1(a). Note that a via is said to be an upstream (downstream) via if the electronic current is move up (down) through it.

These barriers are thin layers of refractory metals, such as Ta and TaN, or Ti and TiN, characterized by very low diffusivities of copper atoms. Their presence at the line ends explains the depletion and accumulation of atoms and the



(a) (b)

Fig. 1. (a) Single-link test structures with upstream and downstream vias, where arrows indicate the direction of electron flow. (b) Interconnect segment confined by diffusion barriers/liners.

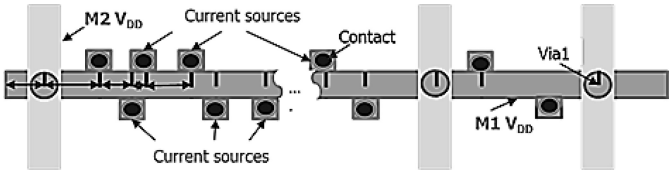


Fig. 2. Schematics of the current source distribution along a power line.

corresponding generation of tensile and compressive stresses at the cathode and anode ends of a line that is loaded by unidirectional current. A very different picture of the redistribution of metal density and stress, caused by electric stressing, can be expected in multibranch interconnect structures formed by connected metal lines within the same metal layer, which are called interconnect trees [2], as in Fig. 1(b). The connection point between metal lines in an interconnect tree is called a junction. The absence of diffusion barriers in tree junctions allows atoms to freely migrate between lines along the trajectories of the current carriers. When a multibranch structure includes metal lines that are connected in parallel, the creation of a void in one of the parallel branches does not necessarily result in a failure, which contrasts with what happens in a single line segment, because current can continue to flow in the unvoided parallel lines [2]. The on-chip power/ground (p/g) grid is an example of such electrically redundant multibranch structures. Indeed, wide p/g rail segments and narrow leads connecting them to the gates are placed in the same level of metallization and continuously connected to each other and to the interlayer power vias, as in Fig. 2. If any of these segments are undercut by a void, the power is still delivered to the underlying gates from the redundant via [3]. Voiding of the metal segments or junctions causes a redistribution of the segment currents and, therefore, a voltage drop variation in the grid nodes. An EM-induced failure of a p/g grid is deemed to occur when the increased resistance of the voided branches makes it impossible to deliver sufficient voltage to the underlying gates. In other words, when the voltage drop at some gate exceeds the specified threshold [4].

In order to estimate the time-to-failure (TTF) caused by such a failure, a linked multiphysics problem should be solved. First, one must compute the initial voltage distribution, which is generated by the underlying gate currents, so called the time-zero voltage drop. Kinetics of the stress evolution in each interconnect tree should then be resolved until the first void is nucleated. Then, the analysis of the void shape and size evolution should be performed in order to trace changes in resistances of individual voided lines and vias, which result in redistribution of currents in the grid. This should continue until the voltage variation at any grid node reaches the threshold. This procedure provides the TTF of the p/g grid characterized by an arbitrary given distribution of atomic diffusivities and critical stresses required for void nucleation in all grid branches. Finally, averaging the set of computed TTFs with the proper distribution functions of random diffusivities and critical stresses provides the mean TTF (MTTF) of the grid.

This methodology of theoretical assessment of the p/g grid MTTF was described recently in a number of publications [5]–[8]. A question that was never addressed is the experimental validation of this methodology with real silicon data. The principal difficulty of this validation is the requirement of simultaneous tracking of the EM induced voltage evolution at all nodes. Another complication is related to the high test temperature of 300 °C–400 °C required for the failure development in reasonable times of several hours in order to be tracked in the experiment. The large device leakage currents that happen at such temperatures make the measurements unreliable and prohibit the use of standard test-chips for this validation. A recently proposed novel experimental procedure has demonstrated the potential for addressing these issues [9]. Based on the voltage tapping technique that was originally developed for analyzing a preferred location of void nucleation inside a single-link interconnect segment [10], the voltage evolution was measured at all nodes of a multisegment power grid driven by DC currents through a number of cathode and anode ports. The measurements clearly demonstrated the key role played by different types of voids, such as voids cutting upstream and downstream vias and intraline voids, in the kinetics of current redistribution and nodal voltage evolution and in the development of the ultimate circuit failure [9].

The aim of this article is to confirm the predictive power of the new physics-based methodology of the assessment of EM-induced voltage drop degradation in power grids by a direct comparison of the simulation and measurement results. This article is organized as follows. Section II describes in detail the methodology of theoretical analysis of the voiding induced degradation of electrical characteristics of the grid and extracting the failure statistics. The following Section III provides an in-depth description of the experimental procedure for tracking the dynamics of the nodal voltage evolution and collecting the TTF distributions. In Section IV, a comparison of the measured and simulated results is provided. A phase field method is employed there for analyzing the effect of evolution of different types of voids on the electrical resistances of individual segments of the grid. The results of this 2-D phase field analysis are used, after a proper reduction, for 1-D analysis of the kinetics of the full grid voltage drop degradation. Finally, Section V provides some conclusions and outlines some directions for future research.

II. Theoretical Methodology for Assessing EM-Induced Voltage Drop Degradation in Power Grids

Capturing the EM-induced evolution of stress over time, which results in voiding in some branches, is a crucial part of the theoretical analysis of voltage-drop degradation in the power grid. In this article, we concentrate on the analysis

of EM-induced voiding as it is the more frequent cause of EM-induced failures in the power grids, in comparison with hillocks.

A. Accurate But Expensive 2-D and 3-D Analysis

Strictly speaking, accurate analysis of the stress evolution in a metal line loaded with an electric current requires solution of a number of coupled partial differential equations (PDEs). The continuity equations, describing the evolution of concentrations of vacancies and plated atoms along the line, are linked with the force balance equation yielding the elastic stress evolution due to the interaction of the metal line volumetric deformation with the rigid confinement. The electric current density distribution is found by solving the corresponding Laplace equation. Accounting for the polycrystalline structure of the metals used as conductors in on-chip interconnects, and proper consideration of a variety of venues for the diffusion of vacancies, such as grain boundaries (GBs) and interfaces with liners and capping layers, requires a comprehensive 2-D or 3-D analysis. One must also consider the dependence of vacancy diffusivity on the crystallographic orientations of GBs and on properties of copper interfaces, as well as the variation of thermal mechanical properties of grains with different crystallographic orientations. Special attention should be paid to the phenomenon of equilibration of the local vacancy concentration with the local stress, which involves atomic exchange between metal bulk and GB, and interfaces and dislocations by means of atom plating or dissolution. Indeed, a basic phenomenon of vacancy formation requires transfer of an atom from the lattice site to another location that can accept extra atoms. It can be interstitial sites or extended defects. Thus, changes in vacancy concentration are accompanied by changes in concentration of paired plated atoms. The calculation of the total volumetric strain should account for the generation/annihilation of vacancy-plated atom pairs. Following void nucleation, which happens when the tensile stress reaches a critical value σ_{crit}, the void shape and size evolutions due to atom redistribution along the void surface caused by electric current and the gradient of the surface chemical potential, and due to atomic exchange between void surface and surrounding metal, are described by a combination of the Cahn–Hilliard and Allen–Kahn equations with the phase field formalism. A detailed description of these coupled PDEs and results of their solution for a number of cases using finite element analysis (FEA) was demonstrated previously [11]–[14].

B. Approximate But Efficient 1-D Analysis

However, this comprehensive analysis cannot be employed for EM assessment of large p/g grids. The number of degrees of freedom (DOF) for a relatively small simulation problem, which describes the EM-induced evolution of vacancies, stress, and voiding in a single-link interconnect segment representing a short metal line terminated by upstream or downstream interlayer vias, as in Fig. 1(a), can easily exceed a million! The 3-D FEA method cannot be extended for simulation of grids of any reasonable size.

As shown in [15], the comprehensive 3-D EM model discussed above can be reduced to a 1-D formulation describing the EM induced evolution of the hydrostatic stress σ and the concentrations of vacancies and plated atoms averaged on the cross section of the polycrystalline metal segment embedded into a rigid confinement by introducing the averaged effective diffusivity D_a^{eff} and the effective generation/annihilation rate of the vacancy plated atom pairs. By adopting Korhonen's assumption of immediate equilibration of the vacancy concentration with stress, the system of PDEs described above can be reduced to 1-D Korhonen's equation [16]

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_a^{\text{eff}} B\Omega}{k_B T}\left(\frac{\partial \sigma}{\partial x} - \frac{eZ\rho j}{\Omega}\right)\right] \tag{1}$$

which describes the stress evolution in a metal line embedded in a rigid confinement under a current density j. Here, B is the effective bulk modulus [2], ρ is the metal resistivity, Ω is the atomic volume, $q* = eZ$ is the effective charge of the migrating atom, e is the elemental charge, Z is the effective valence, k_B is the Boltzmann constant, and T is the absolute temperature. Equation (1) provides different stress evolution kinetics, depending on the boundary conditions (BCs) at both ends of a line segment and the character of the electric current load, which may be time dependent or constant. Different solutions to Korhonen's equation with different BC have been reported in several papers (see, for example, [16]–[20]).

C. Effective Diffusion Coefficient

All these analyses have adopted the condition assumed by Korhonen *et al.* [16] that the effective atomic diffusion coefficient D_a^{eff} does not depend on stress. In the following, we will adopt this approximation for the sake of simplicity. The effective diffusivity includes atomic diffusion in metal bulk, in GBs, and along interfaces (IFs). Since the bulk diffusivity is much smaller than the other two, the effective diffusivity can be expressed as

$$\begin{aligned} D_a^{\text{eff}} &= (1 - f_{cb}) D_a^{\text{IF}} \frac{\delta^{\text{IF}}}{h} + f_{cb}\left(D_a^{\text{IF}} \frac{\delta^{\text{IF}}}{h} + D_a^{\text{GB}} \frac{\delta^{\text{GB}}}{d}\right) \\ &= D_a^{\text{IF}} \frac{\delta^{\text{IF}}}{h} + f_{cb} D_a^{\text{GB}} \frac{\delta^{\text{GB}}}{d} \end{aligned} \tag{2}$$

where $\delta^{\text{IF}}$and δ^{GB} describe correspondingly the thicknesses of the interface and grain boundary, d is the grain size, and h is the line thickness. The parameter f_{cb} is the fraction of the line length occupied by polycrystal clusters, and $(1 - f_{cb})$ is the fraction characterized by the bamboo grain structure. Hence, f_{cb} determines the relative contribution of GB and interface diffusion to overall mass transfer in a Cu interconnect line [21]. Since grain sizes follow the lognormal distribution [22], it is also valid for the distribution of diffusivity. The effective diffusivity is described by a thermal activation mechanism, $D_a^{\text{eff}} = D_0 \exp(-E_a^{\text{eff}}/k_B T)$. It is assumed that D_0 is a constant, and the effective activation energy E_a^{eff} is a random characteristic.

D. Efficient Power/Ground Grid EM Assessment

The flow of the method for p/g grid EM assessment starts with a decomposition of the grid into interconnect trees. For each tree, the set of discretized PDEs (1) is solved for all branches characterized by different current densities, diffusivities, and geometries (length and width). The solutions at the segment junctions are linked through the proper BC given by (3) and (4) reflecting the continuity of stress and atomic flux at every junction between neighboring branches

$$\sigma_n(x,t) = \sigma_{n+1}(x,t), x = x_n,\ t > 0 \tag{3}$$

$$\kappa_n\left(\frac{\partial \sigma_n}{\partial x} + G_n\right)w_n = \kappa_{n+1}\left(\frac{\partial \sigma_{n+1}}{\partial x} + G_{n+1}\right)w_{n+1}, x = x_n,\ t > 0. \tag{4}$$

Here, $\sigma_n(x,t)$ is the time-varying hydrostatic stress at location x in the nth branch of the tree and the standard notations are used as $\kappa_n = D^n_{\text{eff}}B_n\Omega/k_BT_n$, and $G_n = eZ\rho j_n/\Omega$, where D^n_{eff} is the effective atomic diffusivity in the nth branch, B_n is the effective bulk modulus, w_n is the branch width, and j_n is the electric current density in the nth branch. The initial condition for (1) is the stress in interconnect tree at $t = 0$, before the electric stressing is applied. In on-chip interconnects, since the metal lines are embedded in a rigid confinement, the difference in the coefficients of thermal expansion (CTE) of the metal and confinement generates residual stresses $\sigma_n(x,0)$ as the chip cools down after the anneal step. The temperature distribution across the metal layers is taken into account by employing a compact thermal model, similar to [23].

In a typical power grid structure, every metal layer mostly consists of a set of alternating parallel power and ground stripes, which are, respectively, connected to the power and ground stripes of the immediate upper and lower neighboring layers by vias. This gives rise to the mesh structure in modern grids. These metal stripes are the multibranch structures, which represent interconnect trees. Note that the stripes are not necessarily straight lines: they may have orthogonal branches, which can be, for example, the leads connecting p/g rails with the vias of the underlying logics. In the flip-chip technology, the top metal layer is connected to the external package through C4 bumps, while the bottom layer is connected to the underlying logic circuitry.

The only parasitic effect on a p/g grid, which is important in EM analysis, is the resistive one. This is because EM analysis is based on effective DC current densities. A p/g grid is a linear system, with current sources (modeling the effects of the underlying logic circuits) as inputs and node voltage drops as outputs. Since p/g grids carry mostly unidirectional currents, the effective-EM currents are the same as average currents [19]. The mesh model [6] should be used for p/g grid reliability checks, in which user-provided thresholds on average voltage drops are used to determine the grid lifetime. In this framework, it becomes sufficient to perform DC analysis of the power grid, driven by average source currents. Applying Kirchhoff's current law at every node leads to the following nodal analysis formulation:

$$G(t)\upsilon(t) = i_S \tag{5}$$

where $G(t)$ is the time-varying (but piecewise-constant) conductance matrix, $\upsilon(t)$ is the corresponding time-varying (but piece-wise constant) vector of node voltage drops, and i_S is the vector of effective values of the current sources tied to the grid. This system could be used to obtain the evolution of voltage drops directly for an analyzed power grid.

Initial current densities and nodal voltages in all branches can be determined by the appropriate power integrity tools. Based on the set of design specification, such as the layout file, which may be the LEF/DEF database, and cell description with .lib, SDC file for current sources extraction, which contains timing constraints, the employed power integrity tool generates the list of all resistors with resistance values, where each resistor is specified by coordinates of two nodes and metal layer index for each node, length and width of each resistor, mapping of metal layer names and indexes, belonging of each node to a VDD/VSS net; voltage drop for each node; voltage sources: names of nodes that represent VDD/VSS voltage ports; current sources: nodes where cell instances are connected and the corresponding supply currents.

The solution of the above initial value boundary problem (IVBP) (2)–(5) with randomly chosen atomic diffusivities for each branch of the grid and critical stresses σ_{crit} for each discretization node provides the kinetics of stress evolution until σ_{crit} is developed at any node of the p/g grid. It means that a void is nucleated at this location, which can be either a junction between branches representing in majority of cases an interlayer via, or an intrabranch location of the node resulted by the branch discretization [8]. It should be mentioned that by the void nucleation, we mean an activation of a preexisting defect by the EM-induced stress. The inverse dependence of σ_{crit} on the defect size [21], [24], which can be expected in the range of several nm, suggests the several hundreds of MPa as a good estimation for σ_{crit}. The overwhelming presence of small size defects suggests that the asymmetric distribution functions, such as Weibull or Lognormal, should be used for σ_{crit} characterization.

It is known that void nucleation does not lead to immediate change of a line or a via resistance. A noticeable increase of the line resistance will happen when a growing void undercuts a line cross section and forces electric current to pass through high resistive liners. An upstream via resistance will undergo noticeable changes when a void growing in the metal line undercuts a via top, or when this void or voids drifting along the line toward a cathode end will propagate into the via toward its bottom and also force electric current to pass through via liners. A downstream via will experience a resistance increase when void is nucleated exactly below the via bottom, which services as a cathode in the underneath metal line. In Section IV, we will demonstrate a set of compact models developed for capturing effects of different types of voiding on degradation of the grid voltage drop.

Postvoiding stress evolution is described by the same IVBP (2)–(5) with the additional BC at the emerged void surface, which in the 1-D case is reduced to BC at the void ends. The large stress gradient formed in close proximity to a void causes atomic flux to flow from the void surface into the metal bulk, which results in an increase of the void size and reduction

of the tensile stress. Introducing an effective thickness of the void interface δ, which is infinitely small in comparison with all other lengths, allows us to introduce a stress gradient between the zero-stress void surface and the surrounding metal as $\nabla\sigma = \sigma(\delta, t)/\delta$, where $\sigma(\delta, t)$ is the stress in the metal near the void surface. In the case of a single line, an analytical solution of (1) with zero flux BC at the anode end of line $\partial\sigma/\partial x|_A - eZ\rho j/\Omega = 0$ and $\partial\sigma/\partial x|_V - \sigma/\delta = 0$ at the void edge yields the postvoiding stress relaxation kinetics with the final steady-state linear stress distribution characterized by the zero stress at the void edge [20]. The void length in the 1-D case evolves as

$$l_{\text{void}}(t) = -\int_0^L \frac{\sigma(x,t)}{B}dx \tag{6}$$

where L is the line length [21]. In a case of multiple voids nucleated in the same tree, (6) provides the cumulative length of all voids. An individual growth rate of each void can be obtained by calculating an atomic flux $\Gamma(x, t)$ from each void into the metal bulk as

$$v = \Omega\Gamma(x,t) = \frac{D_a^{\text{eff}}\Omega}{k_B T}\left(\frac{\partial\sigma}{\partial x}\bigg|_{\text{void\_edge}} - \frac{eZ\rho j}{\Omega}\right). \tag{7}$$

Simulated void length evolution is used for extracting the time-varying conductance matrix $G(t)$, and calculating the time-varying vector of node voltage drops $\upsilon(t)$. The details of the developed numerical analysis and the EM assessment flow can be found in [6] and [8]. Here, we just want to mention that the maximal grid size that was assessed with the proposed methodology had 1.6×10^7 nodes, 1.25×10^7 branches, and 2.78×10^6 trees. It was found that 10% increase of the voltage drop was developed in about 11 years. The run (CPU) time of 5.5 h was spent for calculating the MTTF of this grid. A major result of this assessment was a demonstration of the effect of the grid redundancy on TTF. It was shown that the formation of the first void alone did not cause a grid failure. A failure criterion of 10% voltage drop increase was met due to the cumulative effect of nucleation of several voids and their growth in the failed branches.

III. Experimental Procedure for Tracking the Dynamics of EM Induced Nodal Voltages in P/G Grids

Resistance shift measured in experiments is typically used as the indicator of EM failure. These studies mainly focus on how EM lifetime of a simple single-link test structure is affected by structure geometries, temperature, current density, current frequency, and duty cycle. In contrast, EM studies in power grid structures have been seldom reported due to the complexity of the measurement. Due to redundant current paths in a power grid, it is imperative to understand how the voltages at different points in a power grid change with EM voiding. This is different from single wire measurements where the time to failure is determined simply based on a fixed shift (e.g., 10%) in the overall resistance. In power grids, the current density profile is much more complex than that of a single wire structure. This difference can result in considerable discrepancy between EM behaviors in single wire and power grids.

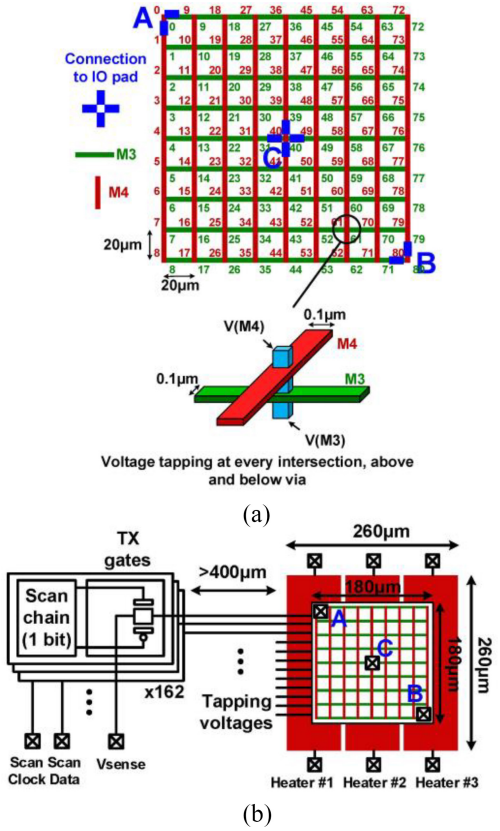


Fig. 3. (a) 9×9 M3–M4 power grid with three voltage connection points. (b) EM test chip with on-chip heaters, power grid, I/O transmission gates, and scan chain [9].

In order to study the EM effects in a power grid, the voltage tapping idea [10] was employed in [9]. As a result, the failure location and failure time of each individual EM event in a power grid with realistic structure were tracked. EM healing phenomena in a power grid under constant voltage and constant current stresses were reported. Several chips under a variety of stress conditions were tested. It was found that the first failure location is always close to the terminal with the lower voltage level (cathode). For accelerated testing, on-chip poly heaters were utilized, raising the local die temperature to 350 °C.

The 9 × 9 test-grid structure is implemented in M3 and M4 metal layers, as shown in Fig. 3(a). Pad connection points A, B, and C with multiple dense vias to prevent failure are located at the two corners and the center of the grid. Each metal segment is 20 μm in length and 0.1 μm in width. A total of 81 intersections are formed on the entire 9 × 9 grid. To collect EM data within an attainable stress time, single minimum size V3 vias are used to connect M4 and M3 layers at each intersection. The resulting 162 nodes are uniformly distributed on the entire grid, with half of the nodes located in M4 and the other half in M3 layers. As shown in Fig. 3, the V4 vias are used to tap the node voltages in M4, and V2 vias to tap the node voltages in M3. This design allows one to directly

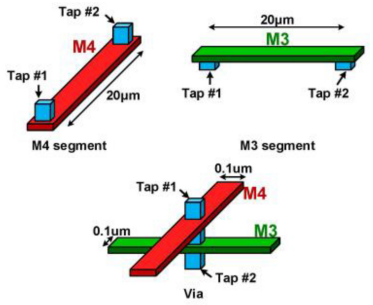


Fig. 4. Voltage drops are calculated at each via, M3 and M4 line segments based on tapped voltages [9].

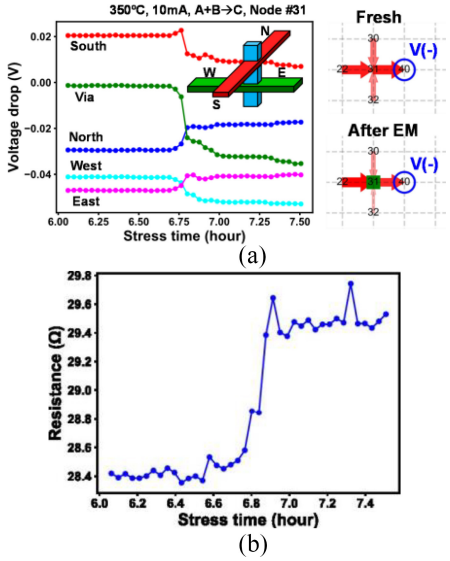


Fig. 5. (a) EM-induced evolution of voltage drops in the via and adjacent metal segments and (b) total resistance jump [9].

measure the voltages in the grid structure without introducing any appreciable electrical or mechanical disturbance to the power grid. M5 and M2 wires are routed to the transmission gate array located at the other side of the chip to protect from the extremely high stress temperatures.

As shown in Fig. 3(b), each power grid voltage is multiplexed out through individual transmission gates connected to a shared analog pad. A scan chain enables one tapping voltage at a time, and I/O devices are used to suppress the leakage current. The active circuits are placed more than 400 μm away from the heating area to further reduce the leakage current. Three on-chip poly resistor heaters are used for efficient local temperature control. The heating area is 260 μm $\times$ 260 μm, with the power grid placed in the middle. The voltage drops across each 20 μm M4 and M3 segment and V3 via were calculated from the measured tapping voltages, as in Fig. 4.

Fig. 5 shows how the voltage drop changes in the north, east, south, and west branches surrounding the location of the first EM failure. The total resistance trace between $A + B$ and C is also plotted for comparison, in Fig. 5(b). In this test, a stress current of 10 mA is sourced from node A and B to C. Only the traces around failure location are plotted. At 6.8 h, the total resistance jumps from 28.4 Ω to 29.5 Ω in a very short time and then stabilizes around 29.5 Ω, indicating that it is an abrupt EM failure rather than a progressive EM failure. There is no direct approach in traditional total resistance tracking test to obtain the failure location during stress. As employed in this experiment, the tapping technique for voltage measurement allows one to detect the failure location. As shown in Fig. 5(a), when a failure occurs, voltage drops in several nearby nodes and branches demonstrate significant changes. Since the change of voltage can be attributed either to the EM induced increase in resistance of the via or wire segment, or to current increase caused by a failure in the nearby location, the magnitudes of all voltage changes should be analyzed. The largest voltage change can indicate the failure location. A detailed analysis of times of voiding and its locations, which was done in this study, has revealed that the failure can happen across the entire power grid with almost no correlation in locations of consecutive in time voids. It was observed that first failures typically happen in the near cathode region of the grid due to large current densities. Different types of voids have been found in this study. The first voiding locations are always at V3 vias, which progress to intraline voiding in M3 and M4 layers.

IV. Validation of the EM Assessment Methodology by Direct Experimental Tracking of the Dynamics of EM-Induced Nodal Voltage Evolution

For validating the methodology of p/g grid EM assessment, we use it to find the EM-induced voltage drop evolution in the same power grid that was described in the previous section and then compare the results with measurements. We use the same grid architecture, layout dimensions, thicknesses, and resistivities of metal wires, vias, and liners. We stress the grid with the same current and keep it at same temperature. To capture the stochastic nature of EM induced failure, we use randomly generated values of diffusivities and critical stresses governed by the Normal distribution for the activation energy of atomic diffusivity, and the Weibull distribution for the critical stress. The parameters of the distributions are optimized based on the best fit between simulated and measured MTTF.

The grid in question, shown in Fig. 3(a), consists of a total of 18 interconnect trees, nine trees in each M3 and M4 layers. Each tree is a rail consisting of eight equal length branches connected to each other by dotted-I junctions [6] (junctions where two lines are incident at a via), which represent triple points where vias V3 are connected to the rail. Each interconnect tree has nine dotted-I junctions, which, due to the diffusion barrier under every via, form a barrier to atomic flux. Depending on the node voltages, these junctions can be either a cathode, injecting the electronic current into a line, or an anode, the sink of electronic current. Three I/O pads A, B, and C, which are connected by multivia arrays to the M3 and M4 branches of the grid, are used as the cathode (for the whole grid) located in the grid center at pad C, and the two anodes (for the whole grid) at pads A and B, located at the two opposite diagonal corners of the grid, as in Fig. 3. An in-house

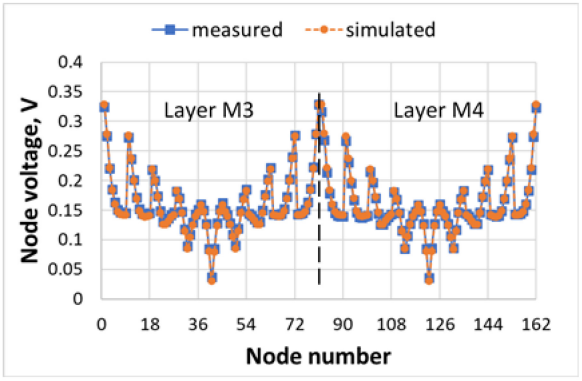


Fig. 6. Fit between simulated and measured initial distributions of nodal voltages in M3 and M4 layers.

power integrity tool mPower was used to extract resistances of all grid branches and vias, which are used to construct the conductance matrix $G(t)$ [25], which is then used to solve (5) with two current sources, each carrying $i_S = 5$ mA, sourced from nodes A and B to node C. Simulation of the nodal voltage distribution across the fresh grid stressed by this source current demonstrates a good fit with measured voltages, as shown in Fig. 6.

The time dependence of the conductance matrix and consequent nodal voltage evolution is governed by EM induced voiding kinetics, which depends on locations and sequence of void nucleation, and void growth and migration. The simulation flow that tracks the evolution of the stresses and voids in every interconnect tree is described in detail in [8]. The trees can be treated independently, because they are isolated from each other by diffusion barriers preventing atomic exchange. However, when voiding is initiated in any of the trees, which may change the resistance of some branches, the electrical coupling of the trees may cause a change in the node voltages and branch currents across the grid.

The numerical integration of Korhonen's equation (1) is performed using the finite difference method [6]. Each branch of length L is uniformly discretized into N equal segments, and the spatial partial derivatives are approximated using the central difference formula. Because the current density j is a constant over time in each branch, Korhonen's equation then provides, for line internal nodes

$$\frac{d\sigma(t)}{dt} = \kappa \frac{\sigma(x+\Delta x,t) + \sigma(x-\Delta x,t) - 2\sigma(x,t)}{(\Delta x)^2} \tag{8}$$

where $\Delta x = L/N$. BC (3) and (4) are used to get the full expression for the right-hand side of (8) at junction nodes, as described in detail in [6]. The adaptive step backward differentiation formula (BDF) is then used to discretize the time derivative and allow one to find the time-domain solution. A spatial discretization number $N = 16$ is used for each branch, as it was found to be optimal [6]. A time increment Δt varies from milliseconds to tens of seconds. For a tree with N_B branches, this results in a set of $(N \times N_B + 1)$ linear equations, which must be solved at every time point.

In this methodology, voids can nucleate at any node of the (discretized) grid, if/when its EM-induced hydrostatic stress exceeds the critical stress. If a void is nucleated, then the increment in its length during each time step is defined by (7), i.e., $\Delta l_v = v\Delta t$. In the finite-difference approach, the stress gradient near the void surface is computed using an extrapolation formula that involves the stress value near the surface σ_0, and the stresses at two neighboring grid points σ_1 and σ_2

$$\Delta l_v = \frac{D_a^{\text{eff}}\Omega}{k_B T}\left(\frac{-3\sigma_0 + 4\sigma_1 - \sigma_2}{2\Delta x} - \frac{eZ\rho j}{\Omega}\right)\Delta t. \tag{9}$$

A check of the resistance growth of voided branches for all trees and calculation of consequent increase in voltage drop in grid nodes are performed periodically with a time step $T_{\text{step}} > \Delta t$. Since the electric current in voided branches flows through the liners, the resistance change depends on liner resistivity ρ_{liner} and its cross sectional area S_{liner}

$$\Delta R(t) = \left(\frac{\rho_{\text{liner}}}{S_{\text{liner}}} - \frac{\rho_{Cu}}{S_{Cu}}\right) l_v.(t). \tag{10}$$

Depending on the particular realizations of D_a^{eff} and σ_{crit} in grid branches and junctions, this voiding kinetics becomes random. In order to predict voltage and current evolutions, a set of physics-based simulation models describing the evolution of different types of voids should be available.

A detailed description of the developed numerical procedure, which involves a steady-state filtering of the immortal trees and parallel calculation of stress evolution in the remaining trees, can be found in [8]. All simulation results demonstrated below are obtained with the following basic parameters of the grid: width and thickness of lines are 100 and 200 nm correspondingly, TiN liner thickness is 4 nm, via radius is 50 nm; liner resistivity $\rho_{\text{liner}} = 2 \cdot 10^{-6}$ Ωm; and via and branch resistances are $R_0^{\text{via}} = 3.5\Omega$ and $R_0^{\text{branch}} = 38\Omega$ correspondingly. Typical values of current densities in M3 and M4 branches are of order of $(2 \div 5) \cdot 10^{10}$ A/m^2.

A. Physics-Based Simulation Models for Conductance Matrix Evolution Caused by Voiding

While the physics governing the void shape and size changes, which is a redistribution of metal atoms along the void surface and atomic exchange between void surface and surrounding metal, is the same for different types of voids, differences in metal segment architectures/geometries and electric current distributions in the case of voids located in M3 underneath downstream vias, in M4 above upstream vias, and inside M3 or M4 branches, result different models. The employment of full EM simulation methodology for describing the void evolution, explained in Section II, helps to generate these models. Some examples of simulated void evolution in different cases are shown in Fig. 7.

Voiding evolution shown in Fig. 7(a) happens in the case of upstream via, where electron flow is directed from M3 wire to M4. A void precursor either could be located at the interface between M4 metal and dielectric cap layer just above the via, where the high hydrostatic stress is developing, e.g., Fig. 8, or the small voids could drift from the nucleation sites located in the wire somewhere downstream the electron flow. Electric current induced atomic migration along the void surface and

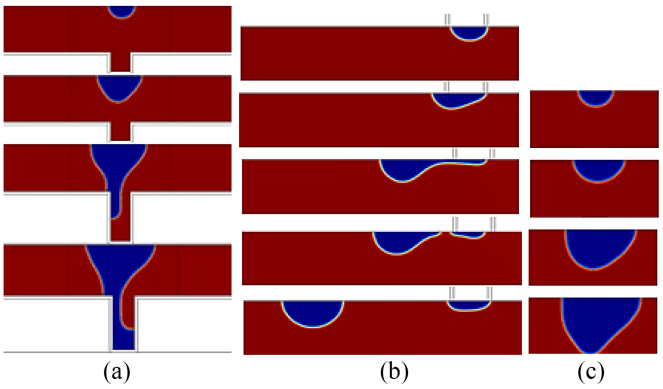


Fig. 7. Voiding evolutions at upstream (a) and downstream (b) vias, and in line (c).

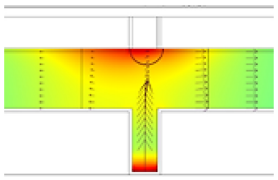


Fig. 8. Hydrostatic stress distribution in the dotted-I junction between upstream via and M4 metal line.

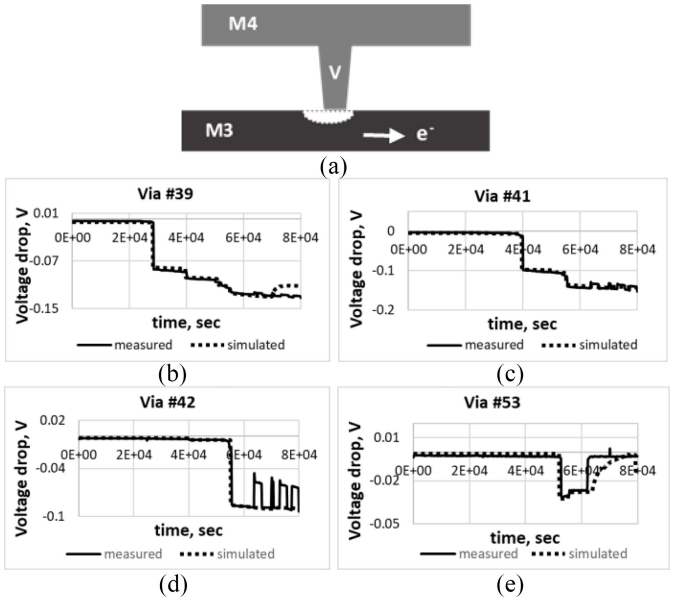


Fig. 9. Voiding below the downstream via (a), and voltage drop evolutions caused by voiding in some downstream vias (b)–(e).

atoms exchange with metal cause the void growth toward the via and partial propagation to the via bottom. Such phenomenon was experimentally observed in [26] and simulated in [14] and [27]. Fig. 7(b) demonstrates a case where a void nucleated in M3 underneath the downstream via undercuts it electrically from M3 wire and migrates along M3 wire in the direction opposite to the electron flow. As a result, it partially reopens the via, and then splits on two parts, with one drifting away, and another continuing the growth until, finally, undercuts the via again. A void evolution shown in Fig. 7(c) can happen when a precursor located at the metal-cap interface in the wire somewhere between junctions is growing until it undercuts the entire wire cross section. This behavior is possible if pinning of a void by a GB prevents its migration, and atom exchange between void surface and surrounding metal is fast enough.

These simulation results have inspired us to develop a number of compact models describing the void evolution in a variety of grid segments. Calibration of model parameters has resulted a good fit between the kinetics of simulated and measured nodal voltage evolutions.

In the following sections, we will demonstrate different 1-D compact models that were developed for description of voiding dynamics in three major locations: 1) metal line below a downstream via; 2) metal line above an upstream via; and 3) intraline location.

1) Voiding Beneath Downstream Vias: If a void is nucleated at a dotted-I junction under a downstream via, we assume that it immediately undercuts the via. The void shape is assumed to be semispherical with its initial radius given by $r_{\text{void}} = r_{\text{via}}$. An electric current in an M3 wire, recomputed after cutting off the via, can move the void along the current direction. For the void drift velocity, we have the equation [26]

$$\vartheta_V = \frac{D_S \delta_S e Z \rho j}{k_B T r_{\text{void}}} \tag{11}$$

where D_S is the atomic diffusivity along the void surface and $\delta_S = N_S \Omega$ is the effective thickness of the surface diffusion layer, which we use as a tuning parameter, with N_S as the concentration of void surface atoms participating in surface diffusion. Along with the drift, we also compute and track the void growth. A grid node below a via is a junction between two branches. It is assumed that the nucleated void grows into both branches. Void lengths l_{v1} and l_{v2} in each branch and corresponding branch resistance increases are calculated with (9) and (10). In order to simultaneously capture the void drift and growth, we assume that the semispherical formalism (11) can be used in 1-D approximation for the description of displacements of both void edges caused by void drift.

A good fit between simulated and measured nodal voltage kinetics in case of a downstream via can be achieved with a slightly modified model of void length evolution, in order to describe a partial via reopening happening during void evolution. Indeed, a small void shift to the left, as in Fig. 9(a), which can be caused by a redistribution of the void surface atoms, results in a partial restoration of the via conductivity. Resumed electron flow through the reopened part of the via bottom (from M4 wire to M3) moves copper atoms away and generates additional tensile stress under the via. It accelerates a dissolution of the void surface atoms into the metal, which results in a drift of the void edge to the right with a possibility to cut off the via one more time. This process can repeat itself many times, which can explain the nodal voltage oscillations observed at node #42 in the experiment, as shown in Fig. 9(d).

In order to represent this behavior with a 1-D approximation, the following simplified models were developed. Void drift during the time increment Δt results in its shift to the

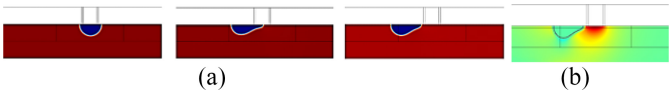


Fig. 10. (a) Voiding evolution under the bottom of downstream via caused by large current in M3 line. (b) Hydrostatic stress distribution around the bottom of downstream via with restored electrical connectivity by moving void.

left and partial opening of the via bottom, which is

$$\Delta l_{\text{left}}(t) = \frac{D_S \delta_S e Z \rho j(t)}{k_B T r_{\text{via}}} \Delta t. \tag{12}$$

Via conductance is determined by the length of the bottom opening, which as a simple approximation can be computed as $G_{\text{via}}(t) = G_0 |2r_{\text{via}} - \Delta l_{\text{open}}(t)| / 2r_{\text{via}}$. One can then easily recompute the currents and voltages with this new via conductance, which provides the stress under the open via bottom. The shift of the void edge to the right, due to atomic transfer between the void surface and the metal, is

$$\Delta l_{\text{right}}(t) = \frac{D_a^{\text{eff}} \Omega}{k_B T} \frac{\partial \sigma(t)}{\partial x}\bigg|_{\text{void\_edge}} \Delta t. \tag{13}$$

Thus, the new length of the open part of the via bottom is

$$\Delta l_{\text{open}}(t) = \frac{D_S \delta_S e Z \rho j(t)}{k_B T r_{\text{via}}} \left| 1 - \frac{D_a^{\text{eff}}}{D_S \delta_S} \frac{\Omega r_{\text{via}}}{e Z \rho j(t)} \frac{\partial \sigma(t)}{\partial x}\bigg|_{\text{void\_edge}} \right| \Delta t. \tag{14}$$

Equation (14) shows that a large stress developed under the reopened portion of the via bottom can generate an oscillation of via conductivity. Depending on the ratio of atomic diffusivity in the wire and at the void surface, D_a^{eff} / D_S, and on δ_S, the stress needed to initiate the voltage oscillation can be of the order of tens of MPa. It can also be seen from (14) that when a large current passes through the M3 wire, this effect of the via conductance oscillation is small, which corresponds to a result obtained with the phase field method, as in Fig. 10. It should be mentioned that due to the nature of the parameter δ_S, which was introduced to fix the physical dimension (see, for example, [13], [27]), only a product $\delta_S D_S$ is used in the analysis. Best fit with measurement results was obtained with $\delta_S D_S = 4 \cdot 10^{-9} D_a^{\text{Eff}}$.

By tuning the model parameters, the voltage drop kinetics are found to agree with the measured ones in the vias at nodes 39, 41, 42, and 53, as shown in Fig. 9(b)–(e). It can be seen that when the electric current in M3 wire is small, as in the case of node #42 where $j_{\#42-\#51} = 3 \cdot 10^{10}$ A/m^2, the under-via voiding generates via voltage oscillations, as in Fig. 9(d). A different situation was observed in the case of node #53, where the large current density of $j_{\#42-\#53} = -7.5 \cdot 10^{10}$ A/m^2 in the M3 wires causes fast void drift along the current direction and full restoration of via connectivity in accordance with (14), as in Fig. 9(e). Simulation shows that when a void moves away from the via, large tensile stress is developed under the via, as in Fig. 10(d), which can be sufficient for a new void generation. But in this case, measurements did not show any voltage oscillation at this node, as in Fig. 9(e). This can be explained if we assume that the original void precursor was eliminated during the first void evolution. Simulated voiding

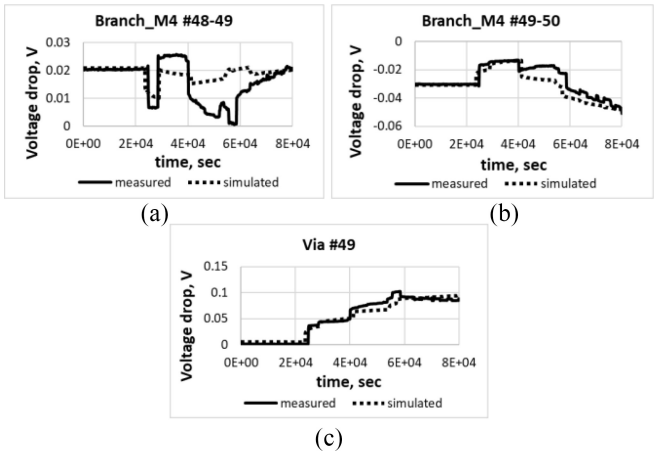


Fig. 11. Kinetics of voltage drop evolutions caused by voiding in upstream vias, simulations versus measurements. Voltage drop along the branches (a) and (b), and inside via (c).

times of 28 110, 39 500, 52 000, and 55 000 s were obtained with σ_{crit} of 339, 457, 144, and 325 MPa for nodes 39, 41, 53, and 42 correspondingly. These times match the measured times of sharp voltage changes observed in these nodes.

2) Voiding Above Upstream Vias: A large hydrostatic stress generated by EM above a V3 via in the M4 metal line, as shown in Fig. 8, suggests a high probability of void nucleation there since the growth of precursors with different sizes can be activated. Like the case of a downstream via, we assume that a grid node above a via is a junction between two branches. It is also assumed that the nucleated void grows into both branches. Void lengths l_{v1} and l_{v2} in each branch and the corresponding branch resistance changes are computed using (9) and (10). As shown in Fig. 7(a), a part of the above-via void can propagate into the via and partly occupy it. This happens in the case of large currents passing through the via. When currents are small, voids are formed only in the two M4 branches. In the former case, electric current will be forced to pass through the via liners and liners of the portion of M4 branches undercut by voids. Via resistance is estimated as $R^{\text{via}}(t) \approx R_0^{\text{via}} + \theta(l_{v1}(t) + l_{v2}(t))$, where θ is a parameter that depends on the via radius r_{via}, liner resistivity and a fraction of the void propagated into the via, which is used as a tuning parameter for getting the best fit with measurements. As an example, Fig. 11 shows the fit between simulated and measured kinetics of voltage drop evolution between nodes n48–n49 and n49–n50 in an M4 line, as well as between the top and bottom of via 49, which were obtained with $\theta = 5.1 \cdot 10^8$ Ω/m.

For the demonstrated failed node n49, the $\sigma_{\text{crit}} = 309$ MPa provides a voiding time of $t_{\text{nuc}} = 24800$ s, which matches the measured event time.

3) Intraline Voiding: An EM-induced failure that is the result of void nucleation internal to a metal line, somewhere between two junctions or vias, can be caused by two different mechanisms. The first is when the line resistance increases when the line is cut due to a growing void, as in Fig. 7(c), and the second is due to a drift of the void toward an underlying via in the direction of electric current, followed by a via failure, as in Fig. 7(a). Which of these mechanisms prevails,

depends on a number of parameters, such as current density, critical stress, atomic diffusivity, and others. In the simulation, a void can appear at any discretization point in the line where and when the hydrostatic stress developed during EM stressing exceeds σ_{crit}, which is randomly generated and assigned to that point. Atomic diffusivity assigned to this line governs the kinetics of stress evolution. Usually, voids are nucleated at triple points formed by GBs of neighboring grains or by GB crossing the interface with cap layer or liner. Thus, a void is initially pinned to a GB and needs to grow to a so-called critical size in order to detach [28]. Based on the consideration of the energy that is required for restoration of the portion of the GB area, which was eliminated by the void, the critical size required for detachment was estimated in [28] as

$$R_{\text{DT}} = \sqrt{\frac{6\gamma_{\text{gb}}\Omega}{11eZ\rho j}} \tag{15}$$

where γ_{gb} is the surface energy of the GB. For typical parameter values, $\gamma_{\text{GB}} = 1\ \text{J/m}^2$, $\Omega = 1.66 \cdot 10^{-29}\ \text{m}^3$, $e = 1.6 \cdot 10^{-19} q$, and $Z = 10$, $\rho = 3 \cdot 10^{-8}$ Ohm $\cdot$ m, we have $R_{\text{DT}} = 1.4 \cdot 10^{-2} \big/ \sqrt{j}, m$. Thus, for current densities exceeding $j > 1.9 \cdot 10^{10}\ \text{A/m}^2$, the void detachment radius is smaller 100 nm. The void detachment size will be smaller if we account for current crowding caused by a growing void. In any case, to be in agreement with the experiment, demonstrating that many small voids drift along the line, it would be reasonable for the sake of predictability improvement to introduce a coefficient $\chi < 1$ in (15) which could be calibrated so as to tune the model. In the current study, the value of $\chi = 1$ was used.

In the case when R_{DT} is larger than a biggest linear size of the line cross section, the growing void undercuts the line before it will detach from GB. The time instant when this happens determines the initial moment t_{R0} when the line resistance starts to increase. If the void detachment size is smaller than the line thickness or width, the void will detach from GB at t_{DT} and start drifting toward the line nearest cathode where it can participate in via resistance increase. In order to calculate these time instants, the rate of void growth should be available. A growth rate of the semispherical precursor located at the copper-cap interface was derived in [29], which for long enough times can be written as

$$r_{\text{void}}(t) \approx \sqrt{2D_V\sigma_{\text{crit}}\frac{\Omega}{k_BT}e^{-\frac{E_V}{k_BT}}t} \tag{16}$$

where E_V and D_V are the activation energy of vacancy formation and the vacancy effective diffusivity, which can be substituted by an atomic diffusivity based on the standard relation $D_a = D_V \exp\{-E_V \big/ k_BT\}$ describing the equality of atomic and vacancy fluxes. Hence, based on (15) and (16), we can express t_{DT} and t_{R0} as

$$t_{\text{DT}} = \frac{k_BTR_{\text{DT}}^2}{2D_V\sigma_{\text{crit}}\Omega}e^{\frac{E_V}{k_BT}} = \frac{3k_BT\gamma_{\text{gb}}}{11D_V\sigma_{\text{crit}}eZ\rho j}e^{\frac{E_V}{k_BT}} \tag{17}$$

$$t_{R0} = \frac{k_BT(\max(W,H))^2}{2D_V\sigma_{\text{crit}}\Omega}e^{\frac{E_V}{k_BT}}. \tag{18}$$

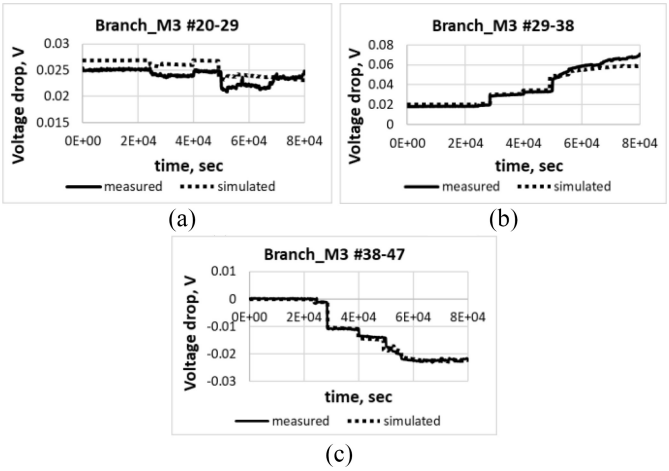


Fig. 12. Kinetics of voltage drop evolutions caused by intraline voiding in (b), voided M3 branch (n29–n38) and electrically connected neighboring (a) and (c) M3 branches (n20–n29 and n38–n47), simulations versus measurements.

Thus, for EM induced failure caused by the intraline void, we are interested in t_{R0}, a moment of time when a line resistance growth is started, which is different for different branches of the grid. Indeed, it depends on random factors, such as atomic diffusivity and precursor size, which provides σ_{crit}. To generate these initiation times, we perform the following simulation steps: 1) by solving Korhonen's equation, we generate the kinetics of stress evolution in every branch of the grid, which depends on the branch current density, temperature, and random atomic diffusivity and 2) for each discretization node of all grid branches, characterized by different random diffusivity, we exercise the MC run to generate the random σ_{crit}. This allows us to extract locations and instances in time where and when void growth is activated. If the void undercuts the line, then t_{R0} is calculated by (18). Further void growth can then be computed with the standard void growth technique (9).

As an example, Fig. 12 shows the fit between simulated and measured kinetics of the voltage drop evolution in the neighboring M3 branches caused by intraline void formed between nodes n29 and n38. For the failure in the branch n29–n38 of M3 line, the used $\sigma_{\text{crit}} = 270$ MPa and constant $D_a^{\text{eff}} = 1.7895 \cdot 10^{-17}\text{m}^2/\text{s}$ provides a voiding time of $t_{\text{nuc}} = 48600$ s, which matches the measured event time.

B. EM-Induced Failure Statistics: Simulation Versus Measurements

Comparison of the computed and measured voltage evolution at a number of grid nodes confirms the validity of the developed compact models. Ten simulated voiding events, shown in the order of appearance in Fig. 13(a), have confirmed that the range of σ_{crit} between 144 and 457 MPa is sufficient to match all the simulated nucleation times. It should be noted that all the voltage evolution kinetics shown above were simulated without Monte-Carlo randomization: constant atomic diffusivity $D_a^{\text{eff}} = 1.7895 \cdot 10^{-17}\ \text{m}^2/\text{s}$ was assigned to all grid branches, and critical stress values were tuned manually

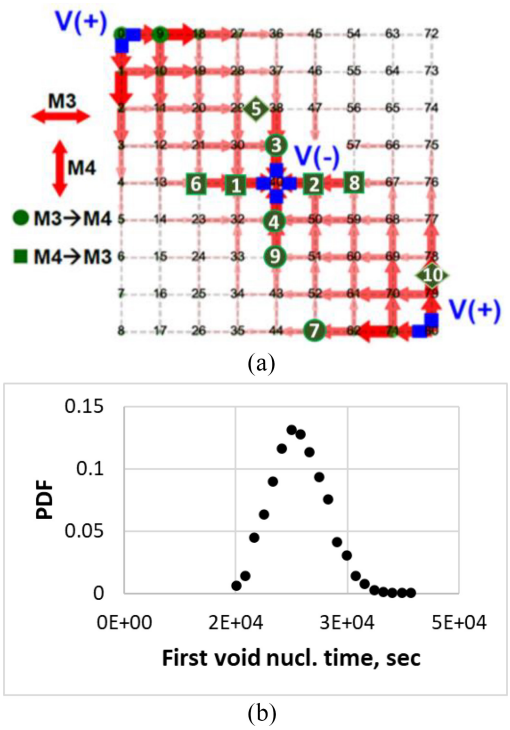


Fig. 13. (a) First ten failures of one of the tested chips in order of generation. (b) PDF of the first void nucleation time.

in order to match the simulated voiding times to the measurements. This has to be done this way for demonstrating that the model is calibratable and for a fair comparison, because there is no way to find out, for a given chip instance, what diffusivities and critical stress happen to be; that is why model tuning is needed. Instead, we are after the MTTF, and we will see below that the fit to the MTTF and the distribution of failure times is very good. Fig. 13(b) shows the simulated probability distribution of the first void nucleation time in grids characterized by different realizations of diffusivities and critical stresses.

The above voiding models have been used for simulating the failure of the grid for different realizations of diffusivities and critical stresses across the grid branches and discretization points. First, we should define the meaning of the EM induced failure of the considered test grid, and then to compute the corresponding TTF. For the standard on-chip p/g grid, TTF is determined as the instant in time when voltage variation at any gate exceeds an established threshold. But this approach is not applicable to the analyzed grid, due to the highly nonuniform original voltage distribution. A more relevant choice would be tracking the variation of the total voltage drop between the cathode (C) and anode (A and B) pads. Different sequences of voiding events and different pictures of current redistribution through redundant pathways in the analyzed test-grid samples provide a clear picture of the statistical nature of EM induced failure.

In this study, the electrical degradation of 20 identical test-grid samples stressed with the total source current of 10 mA at $T = 350$ °C was measured. Hundreds of same test grids were used for collecting the failure statistics by simulations. As it was mentioned above, the effective diffusivity is characterized

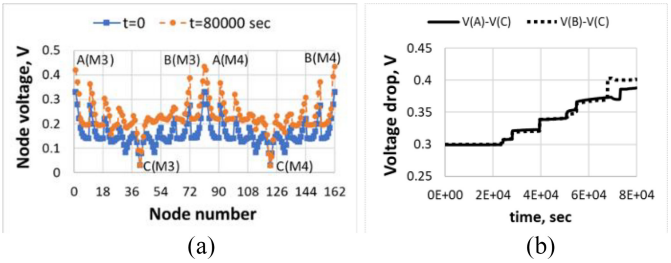


Fig. 14. (a) Voltage drop distribution across the fresh grid and after approximately 20 h of stressing by 10-mA source current. (b) Kinetics of the anode–cathode voltage drop during the stressing.

by the lognormal distribution, which is resulted by the traditional normal distribution of the activation energy of atomic diffusion with the probability density function (PDF) of

$$f(E_a) = \frac{1}{\bar{\sigma}\sqrt{2\pi}} \exp\left(-\frac{1}{2}\left(\frac{E_a - \bar{E}_a}{\bar{\sigma}}\right)^2\right). \tag{19}$$

In the simulation, the mean activation energy $\bar{E}_a = 1.38 \cdot 10^{-19}$ J and the standard deviation $\bar{\sigma} = 8 \cdot 10^{-22} J$ were used. The preexponential factor for the effective atomic diffusivity was kept constant as $D_0 = 5 \cdot 10^{-11}$ m^2/s. The simulation results have demonstrated that only a narrow enough distribution of atomic diffusivity can generate the voiding events across the grid similar to the picture observed in the experiment. A wide distribution generates an unrealistically large number of voids in junctions between branches where the noticeable differences between atomic diffusivities are responsible for flux divergence.

The critical stress is randomly spread across the grid discretization nodes in accordance with the Weibull distribution, which was used to emphasize a low probability of the existence of large size precursors, which are characterized by small σ_{crit} for void generation. The PDF is

$$f(\sigma_{\text{cr}}) = \frac{\beta}{\eta}\left(\frac{\sigma_{\text{crit}} - \mu}{\eta}\right)^{\beta-1} \exp\left(-\left(\frac{\sigma_{\text{crit}} - \mu}{\eta}\right)^{\beta}\right) \tag{20}$$

where, the location parameter $\mu = 200$ MPa, scale parameter $\eta = 110$ MPa, and shape parameter $\beta = 2.2$ were used in simulations in order to have the mean $\bar{\sigma}_{\text{crit}} = 300$ MPa and the standard deviation of 50 MPa.

The statistical EM analysis was performed by means of MC random sampling of values for σ_{crit} and D_a, from the underlying distributions (19) and (20). An increase of anode voltage above 0.4 V was taken as a grid failure criterion. Fig. 14(a) shows an example of the nodal voltage distributions in the fresh grid and in the same grid at instance in time of 80000 s for one of the MC samples. Kinetics of the simulated voltages increase at the anode tabs A and B is shown in Fig. 14(b). It can be seen that cumulative effect of about six to ten voiding events was responsible for achieving the grid failure criterion of 0.4-V voltage drop between anode and catode. This fact confirms that a realistic grid lifetime can be three to four times longer than predicted with the weakest link approximation. Failure PDF and cummulative distribution function (CDF)

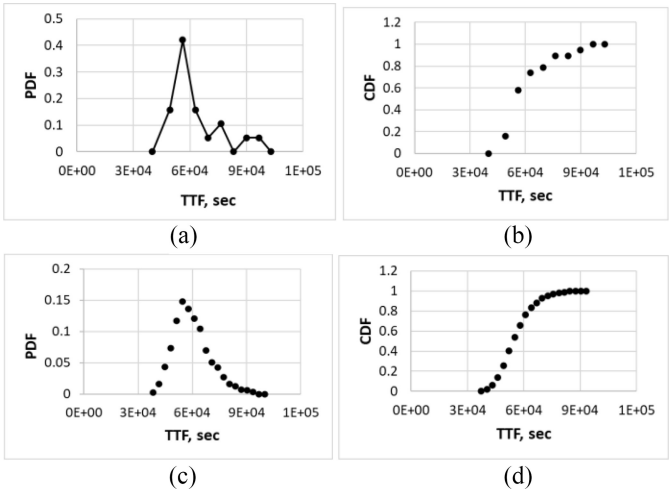


Fig. 15. Failure PDFs and cumulative probability functions extracted from measurements (a) and (b) and from simulations (c) and (d).

extracted from the sets of measured and simulated TTF are shown in Fig. 15.

The resulting $\text{MTTF}_{\text{EXP}} = 62305$ s and standard deviation $\Delta_{\text{EXP}} = 14012$ s computed from experimental data fit well the distribution parameters resulting from the simulation: $\text{MTTF}_{\text{SIM}} = 60344$ s and $\Delta_{\text{SIM}} = 12613$ s. This good fit between failure statistics derived from measurements and simulation was achieved by employing the previously tuned model parameters, such as $\delta_S D_S$, χ, and θ, providing a good correspondence between simulated and measured nodal voltage evolution kinetics, and tuning the characteristics of the probability distribution functions for atomic diffusivities and critical stresses until a good fit between measured and simulated MTTFs and failure distribution widths was achieved. A comparison of the simulated grid failure PDF with the first void nucleation time PDF shown in Fig. 13(b) demonstrates the stronger grid resilience toward EM induced failure than predicted with the series model and the weakest link approximation.

V. Conclusion

A wide range of solid results found in this study validates the robust capability of the described simulation methodology for predicting the on-chip power grid EM lifetime. The consideration of EM induced failure of the grid as the IR-drop degradation is opposite to the widely accepted industry approach where EM-induced failure rates of individual segments are considered as a measure of EM induced reliability and, in the extreme end, the MTTF of the weakest segment is accepted as a measure for the chip lifetime. This approach, when applied to the on-chip power grid, is highly inaccurate [4]–[6]. The direct comparison of the simulated lifetime with the measured on real silicon grid is the only ultimate way to prove validity of either approach.

In this study, the character of EM-induced voltage evolution simulated for the individual grid nodes has demonstrated a qualitative agreement with measurement. Due to the stochastic nature of the EM phenomenon, the quantitative fit cannot be expected for every sample. A random realization of physical parameters across the grid does not allow to predict exactly same kinetics of voltage evolution at different nodes as it was observed in the measurements in Figs. 9, 11, and 12. But, direct comparison of the simulated and measured statistical distributions of EM lifetimes on the same test grid has demonstrated the excellent fit. EM-induced MTTF extracted by both simulation and measurements is very close to each other and several times longer than predicted with the series model and the weakest link approximation.

Further improvement of TTF predictability for the realistic p/g grids can be achieved by accounting for the grid-wide distributions of temperature, residual stress, and the presence of preexisting voids. A capability for accurate estimation of the full-chip power map, current densities, and temperature, which is required for accurate EM assessment, was implemented in the code by a coupling to power integrity and thermal simulation tools. The residual stress developed across the whole interconnect structure immediately after packaging can be assessed by using the methodology described in [30]. Stress relaxation occurring during the chip shelf live can result in a stress distribution that is uniform within every interconnect tree but varies from tree to tree [14].

Despite the need for additional improvements, the presented physics-based EM verification and checking methodology and the numerical technique have demonstrated a capability of realistic assessment of grid's EM lifetime. This article provides a solid validation of this statement.

This physics-based EM assessment approach provides the MTTF for any given power grid, which can be a DC, RC, or RLC netlist, and user-specified current sources and voltages. This approach can effectively relax the very conservative current density design rules, which can allow many improvements in power, time-to-market, and design cost.

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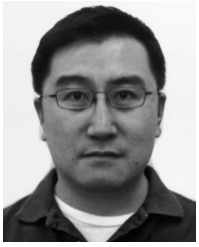

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