Electromigration Check: Where the Design and Reliability Methodologies Meet

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***Abstract*—Due to technology scaling, electromigration (EM) signoff has become increasingly difficult, mainly due to the use of inaccurate methods for EM assessment, such as the empirical Black's model. Results of recent measurements performed on power grid-like structures isolated in the power grid environment have demonstrated that the weak link approach cannot accurately predict lifetime of the power grids. It calls for significant over-design, while, today, there is very little margin left for EM. Numerous observations clearly indicate that there is a need for a new EM checking approach that accurately models EM degradation using physics-based models, combined with a mesh model to account for redundancy, while being fast enough to be practically useful. In this paper, we present a novel approach for power grid EM checking using physics-based models that can account for process, voltage and temperature variations across the die. Existing physical models for EM in metal branches were extended to track EM degradation in multi-branch interconnect trees. Our results, for a number of IBM power grid benchmarks, confirm that Black's model is overly inaccurate. The lifetimes found using our physics-based approach are on average 2.75x longer than those based on a Black's model, as extended to handle mesh power grids. With a maximum runtime of 2.3 h among all the IBM benchmarks, our method appears to be suitable for large VLSI circuits.**

***Index Terms*—Electromigration, hydrostatic stress, power grid, reliability, verification.**

I. Introduction

AS A RESULT of continuing scaling of integrated circuits (IC) technology, electromigration has become a major reliability concern for design of on-die power grids in large integrated circuits [1]. The ongoing IC component miniaturization results in a reduction of the metal line cross-sections and, hence, an increase of the current densities, consistent with the unified theory of constant electric field scaling. It is well known that an EM-induced voiding is responsible for the interconnect line resistance increase, while a hillock formation can generate the electrical short induced failure. This paper concentrates on void-induced degradation because voids occur much more frequently than hillocks in practice. There are two major functions of the on-chip interconnect: (i) as signal lines, providing intra- and inter-cell connectivity for proper signal propagation and (ii) as power (and ground) lines, delivering a well-regulated supply voltage to every cell. While the resistance degradation of individual metal line segments can destroy both these functions, the time-scales of EM induced degradation in the power supply versus the signal lines are quite different. It can be explained by the physical nature of EM-induced voiding, which is the activation of growth of preexisting microscopic defects by generation of high tensile stress at specific regions of a conductor where divergence of atomic flux takes place. The atomic flux is the result of interaction between metal atoms and the applied electric field as well as the conduction electrons due to a momentum exchange. The difference in the pace of EM induced degradation between the power and the signal circuits is in the types of electric currents employed in these two cases. Indeed, the majority of signal lines carry bidirectional currents that lead to a repetitive increase and decrease of the mechanical stress at the wire diffusion blocking ends, which results in very long times to the EM-induced failure. In contrast, power lines carrying mostly unidirectional currents and so can fail in much shorter times due to the absence of, or negligible, stress relaxation. Thus, we can conclude that, in the majority of cases, EM induced chip failure is due to the failure of the power network to deliver needed voltages to some cell of the circuitry, [2]. Hence the focus of this paper is on EM in power grids.

Today, it is becoming harder to sign off on chip designs using traditional EM checking tools, as there is very little margin left between the predicted electric currents and that allowed by EM design rules [3]. This loss of safety margin can be traced back to the inaccurate and oversimplified EM assessment methodology used by existing tools. This methodology is based on an extension of the traditional single link test-structure EM assessment to the domain of the power grid.

A standard single-link test-structure EM test is typically performed on a set of Cu lines, as in Fig. 1a, in which the electric current flows from the wide metal supply lines through the vias, into the narrower test lines. Changes in voltage and resistance over time are measured and recorded. An increase of resistance of individual lines above some threshold value is considered to be a failure. Details describing this methodology characterized by a variety of measurement techniques can be found elsewhere; see [4]. Here, we will only give a brief summary of the approach.

Manuscript received August 22, 2018; revised September 27, 2018; accepted October 1, 2018. Date of publication October 5, 2018; date of current version December 5, 2018. This work was supported by the Semiconductor Research Corporation. *(Corresponding author: Valeriy Sukharev.)*

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Digital Object Identifier 10.1109/TDMR.2018.2874244

The time-to-failure (TTF) of each metal line, stressed by direct current (DC) of density j at the temperature T, is recorded for hundreds of identical lines that may be in the test structures.

The mean-time-to-failure (MTTF) is extracted from the measured TTF ensembles, and it is known to follows the Black's dependency [5]

$$MTTF = \frac{A}{j^n}\exp\left\{\frac{E_A}{kT}\right\} \tag{1}$$

where, k is the Boltzmann constant and A is a proportionality coefficient, which depends on line geometry, residual stress, and temperature. Two critical parameters, the current density exponent n and activation energy E_A are extracted by regression from the measured TTFs. In order for the failure to happen in reasonable time-intervals of several hours, these measurements are carried out at so-called stressed conditions, characterized by elevated temperatures of $200 - 400°C$ and high current densities of $3 \times 10^9 - 5 \times 10^{10}$ A/m^2. Failure times are customarily fitted to a lognormal distribution

$$F(t) = \int_0^t \frac{1}{\sqrt{2\pi}\sigma u}\exp\left\{\frac{\left[\log(u) - \log(MTTF)\right]^2}{2\sigma^2}\right\}du \tag{2}$$

or a Weibull distribution

$$F(t) = 1 - \exp\left\{-0.693\frac{t^\beta}{MTTF}\right\} \tag{3}$$

Here, $F(t)$ is the cumulative percent failures at time t and σ is the standard deviation. Both MTTF and σ are found by plotting the experimental TTF data on a lognormal plot; the coefficient β is extracted from a Weibull plot. All these parameters are extracted from measurements that are done on a variety of test structures designed for different metal layers and different current directions (upstream and downstream tests, as in Fig. 1b).

Translation of the MTTF obtained at the stress conditions to the operating conditions, characterized by lower temperatures and current densities, is performed based on the equation

$$MTTF_{OPER} = MTTF_{STRESS}\left(\frac{j_{STRESS}}{j_{OPER}}\right)^n \times \exp\left\{\frac{E_A}{k}\left(\frac{1}{T_{OPER}} - \frac{1}{T_{STRESS}}\right)\right\} \tag{4}$$

It is assumed that knowing the MTTF and the failure probabilities for each type of interconnect segment and for all metal layers allows one to calculate the failure times for every segment with different geometries using the independent element model, Fig. 2. When the failure probability of the i-th element, $F_i(t)$, is known, the chip level failure probability, $F_{Chip}(t)$, is calculated based on the weakest link statistics

$$F_{Chip}(t) = 1 - \prod_{i=1}^{m}(1 - F_i(t)) \tag{5}$$

where m is the total number of elements with EM concerns in the chip. Thus, EM-induced failure rates of individual segments are considered as a measure of EM induced reliability and, in the extreme end, the MTTF of the weakest segment is accepted as a measure for the chip life-time.

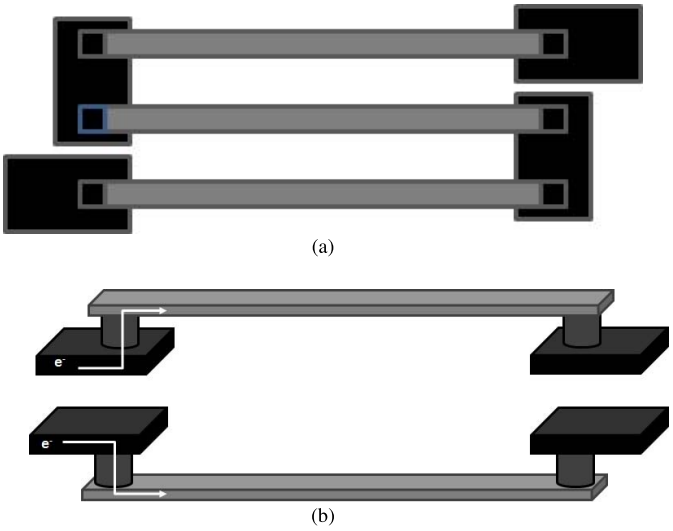

Fig. 1. Multi-link test structure (a), upstream and downstream EM test-structures (b). Black arrows are the electron flow directions.

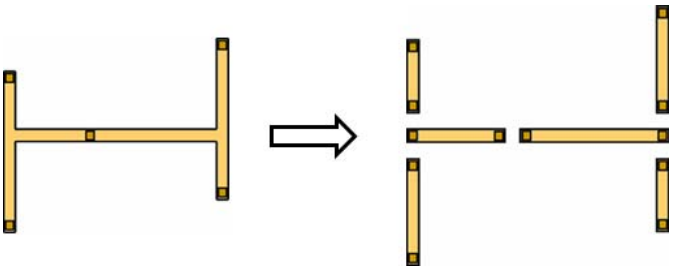

Fig. 2. An interconnect tree broken into segments. In conventional reliability assessment approaches the reliability of the segments are independently estimated, [6].

The scaling equation (4) is used also for generating a set of so-called EM design rules, which provide maximum allowed current densities for all interconnect segments characterized by different geometries, current directions, and temperatures. Indeed, accepting the requirement that each segment should survive not less than a required period of tme $MTTF_{SPEC}$, which can be any specified amount of years, the equation (4) provides the maximum current density sitisfying that requirement

$$j_{MAX} = j_{STRESS}\left(\frac{MTTF_{STRESS}}{MTTF_{SPEC}}\right)^{\frac{1}{n}} \times exp\left\{\frac{E_A}{nk}\left(\frac{1}{T_{OPER}} - \frac{1}{T_{STRESS}}\right)\right\} \tag{6}$$

In accordance with this methodology, the standard practice employed in industry is to break up a grid into isolated metal branches, assess the reliability of each branch separately using Black's model [5] and then use the series model (earliest branch failure time) to determine the failure time for the whole grid, Fig. 2. This approach, when applied to the on-chip power grid, is highly inaccurate, for at least three reasons. First, the fitting parameters obtained for Black's model under accelerated testing conditions are not necessarily valid at actual operating conditions, and this can lead to significant errors in lifetime extrapolation [4], [7], [9].

Second, Black's model ignores the material flow between branches. In today's mesh structured power grids, many branches within the same metal layer are connected (there are no diffusion barriers between them), forming an interconnect tree, and atomic flux can flow freely between them, [6]. As a result, the physical analysis of the failure of a single line segment with diffusion barriers at both ends, which is based on the accumulation of stresses at these ends, is not applicable. This is confirmed by results of the analytical solution of the EM-induced stress evolution in multi-segment interconnect trees, which was done first by Chen *et al.* [10]. As an example, Figs. 3a and 3b demonstrate the EM-induced stress evolution along segments in the 3-terminal interconnect tree shown in Fig. 3d. These time-dependent stress distributions cannot be obtained for the same segments after decomposition of the tree on individual segments, Fig. 2. Stress evolution in each of them separately (assuming diffusion barriers at both ends) provides the set of well-known symmetrical curves, shown in Fig. 3c. Hence, direct use of Black's model providing the MTTF for each segment based on extracted current densities and geometries cannot be justified for multi-line interconnect trees, [6]. For example, in the case where individual branches happen to be short, so that they are deemed immortal due to the Blech effect, [11], then the interconnect would appear to be immortal, which is highly optimistic and can be entirely misleading for design.

Finally, the third problem lies with the series model assumption. A series model is the case where a power grid is deemed to have failed as soon as the first of its branches has failed, typically due to an open circuit. However, modern power grids use a mesh structure, [12]–[15]. As such, there are many paths for the current to flow from the flip-chip bumps to the underlying logic, a characteristic we are referred to as a redundancy, Fig. 4. Mesh power grids are in fact closer to some extent to a parallel system. As such, it is highly pessimistic to assume that a single branch failure will always cause the whole grid to fail.

The later was demonstrated by Ouattara *et al.* [14] by direct measurement of the evolution of resistance in two structures shown in Fig. 5, which were composed at the silicon level of a long wire (250 μm) with a width of 0.2 μm in the metal 2 layer (M2) and supply wires in M3.

Finally, a wire in M1 was tapped in the middle of the structure to represent a standard cell connection. The line under test was connected by via matrices (multiple-vias) to the supply layers. In the reference structure shown in Fig. 5a, the current density j_1 was established between supply vias V_A and V_B, while the layer M1 was not used. In the redundant structure, shown in Fig. 5b, an electric current of twice higher density was injected from the M1 pad into the M2 wire. Due to the equidistant location of the vias V_A and V_B from the M1 pad, the same current densities j_1 were expected in the left and right legs of the M2 wire. It was shown that the redundant structure is characterized by two abrupt jumps of resistance, while the reference structure demonstrated just one coincident with the first jump in redundant. But after the first critical void was generated in the redundant structure, the current continued to flow through the redundant path. Only after

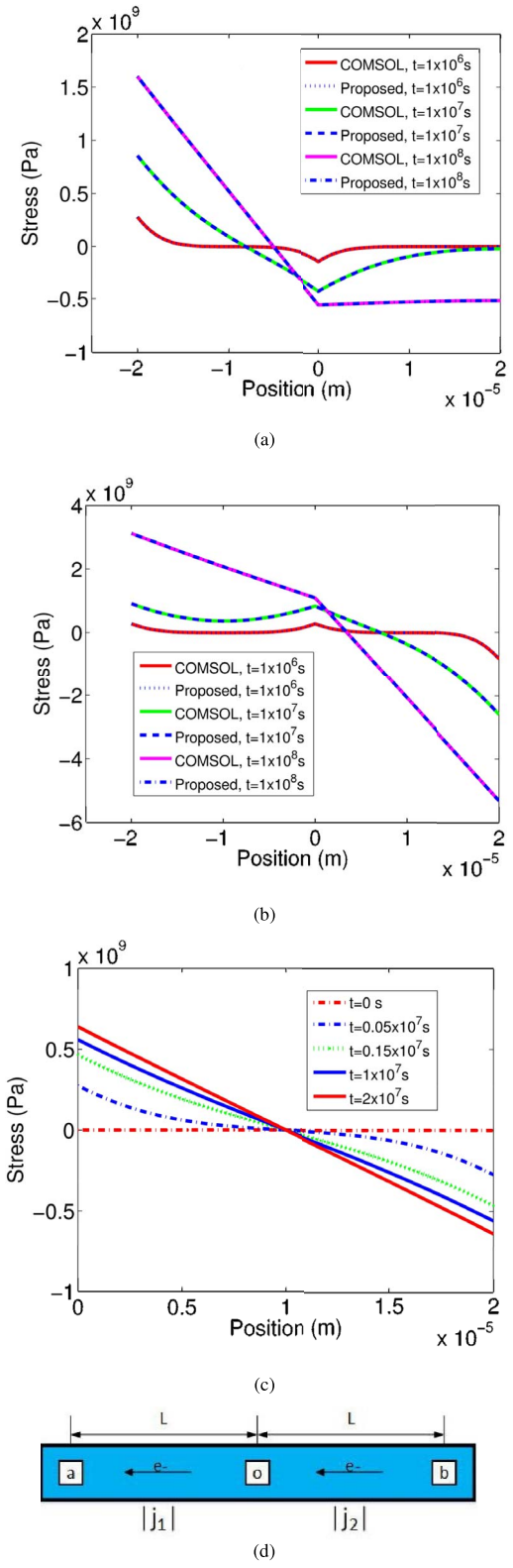

Fig. 3. EM-induced stress development along the lines 1 and 2 in the 3-terminal interconnect tree: (a) $j_1 = 2 \times 10^{10} A/m2$, $j_2 = 0 A/m2$; (b) $j_1 = 2 \times 10^{10} A/m2$, $j_2 = 6 \times 10^{10} A/m2$; (c) single segment with diffusion blocking ends; (d) the straight-line 3-terminal interconnect tree, [10].

generation of the second critical void in the redundant path this structure was failed. Derived cumulative failure distributions versus TTF for both structures have demonstrated the

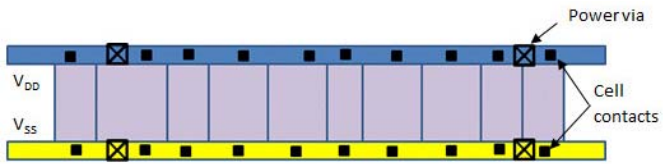

Fig. 4. Example of a power grid. The standard cells, which are the grey rectangles separated by vertical lines, can be supplied by two paths, from either the left or the right power vias.

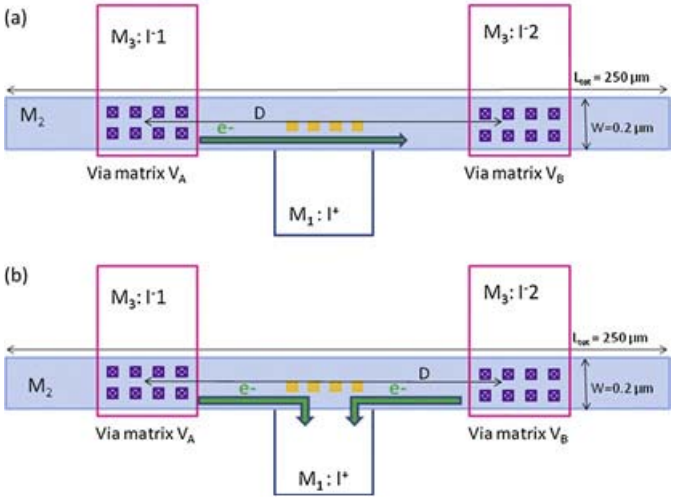

Fig. 5. Test structures: (a) reference, (b) redundant, [14].

same MTTF for both structures, although the total gate current in the redundant structure was two times higher. Note, that the currently accepted EM assessment methodology would consider the later redundant test-structure as failed immediately after the first critical void was formed. Thus, the weak link approximation isn't applicable for power grid EM assessment.

Another experimental demonstration of the importance of redundancy in EM induced power grid reliability was demonstrated recently by Li *et al.* [15]. They analyzed the resistance degradation in small interconnect power grid-like structures isolated inside the power grid environment. Two different 3-leg power grid-like structures have been used for measurements, Fig. 6. The connection between all three parallel M2 legs of 50 µm length provides an isolated structure with almost equal initial resistances of all legs (Type I, Fig. 6a), and, given the parallel connection of legs and the very short length of the M5 connectors (~0.7 µm), leads to almost equal initial currents in the three lines. Another structure (Type II) was designed in a way that the center leg has lower resistance that the other two legs, so that the initial current density in the center leg was higher than in the other two, Fig. 6b. To compare the EM behavior of power grid-like structures with that of the traditional single-link EM structure, a V2/M2 EM test-structure, Fig. 1b, was used as a reference.

Measured distributions of the time to resistance jump for both types of power grid-like structures and the single-link V2/M2 EM structure have shown that both power grid-like

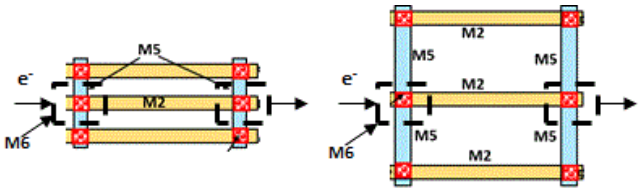

Fig. 6. Schematics of two EM power grid-like structures isolated in the power grid design, [15].

structures demonstrate much longer time to the first jump in resistance than the traditional single link test-structure. The reason is the current redistribution that takes place in power grid-like structures due to the grid redundancy. Redundancy doesn't only provide the alternative current paths, but also allows the electric current to redistribute when the EM induced void causes a local resistance increase. The differences in the times to the first resistance drop observed for different types of power grid-like structures is explained by the larger initial current flowing through the central leg and slower current redistribution caused by the growing void in the Type II structure in comparison with Type I.

Thus, on-chip power/ground interconnect grids have distinct EM characteristics due to the parallel network configuration where the standard weakest link approximation used to evaluate EM lifetime is not applicable for evaluating the EM performance and would have been too pessimistic to project the EM lifetime and current density capability. In addition, Black's model, which is currently employed for calculating the MTTF of individual links, ignores the material flow between branches. In today's mesh structured power grids, many branches within the same metal layer are penetrable by atom diffusion since there are no diffusion barriers between them. In this way, the branches form an interconnect tree where atomic flux can flow freely between them. As a result, the physical analysis of the failure of a single line segment with diffusion barriers at both ends, which is based on the accumulation of stresses at these ends, is not applicable. Hence, direct use of Black's model providing the MTTF for each segment based on extracted current densities and geometries cannot be justified for multi-line interconnect trees. The above observations clearly indicate that there is a need for a new EM checking approach that accurately models EM degradation using physics-based models, combined with a mesh model for the grid to account for redundancy, while being fast enough to be practically useful.

II. EM Assessment of Power Grids Based on Physical Modeling

One such new approach to EM assessment was recently proposed based on the notion that EM induced chip failure is deemed to happen only when the grid interconnect cannot deliver the needed voltage to some part of the underlying circuitry. If the power supply for a circuit is not within the user-defined specification, the result can be a timing violation or a reduction of the noise margin. In other words, the loss

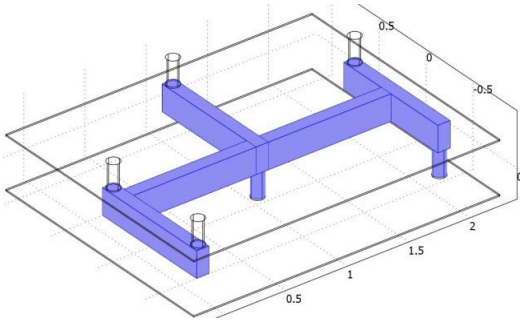

Fig. 7. Interconnect segment confined by diffusion barriers/liners.

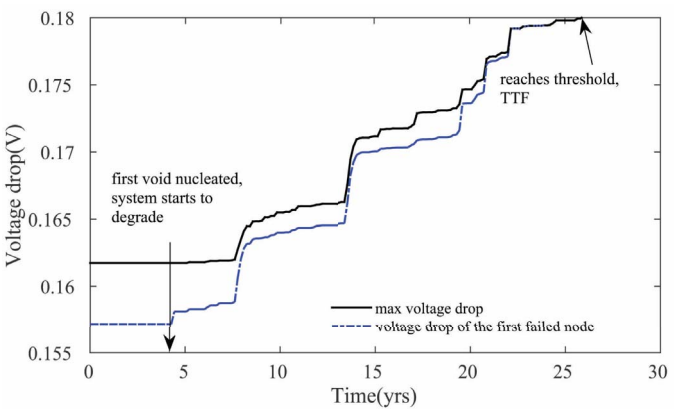

Fig. 8. Voltage drop of the first failed node and the maximum voltage drop in IBMPGNEW1, showing the evolution over time, [17].

of performance, which is a *parametric* failure, should be considered as the more realistic and practical failure criterion for EM-induced power grid failures.

This novel approach has been developed recently, [12], [13], [16]–[19]. Chatterjee *et al.* [12] proposed the mesh model as an alternative to the series model. In the mesh model, a grid is deemed to have failed, not when the first line fails, but when enough lines have failed so that the voltage drop at some grid node has exceeded some pre-defined threshold (which would cause errors in the underlying logic). However, [12] still made use of Black's model to compute the reliability of individual branches, which as we saw above is inaccurate. Huang *et al.* [13], [17] proposed an adaptation of Korhonen's physical EM model [20] for interconnect trees. Hau-Riege and Thompson [6] and, later Alam *et al.* [19] used Korhonen's model to develop a closed-form solution for stress evolution at a junction (a point where multiple branches meet) by replacing connected branches with semi-infinite limbs, which was later used by Li *et al.* [21] in their EM verification tool. The works [13], [16], [17], [21] were later extended to account for temperature variation, [18], [22]–[24].

In [13] and [17] Korhonen's physical EM model was adapted to interconnect trees, representing continuously connected, highly conductive metal lines terminated by diffusion barriers within one layer of metallization [6], Fig. 7. For transient current sources, the effective DC currents and current sources have been calculated in a way as proposed in [13], [16], and [25]. The EM-induced kinetics of the evolution of power grid network resistances were considered. Due to EM degradation, the resistance value of a metal wire starts to increase once a void has nucleated. As a result, this approach ends up with a system of equations for the power grid that is a linear, time-varying and driven by the DC effective currents. To denote the fact that the branch conductances and corresponding voltages can change upon successive void nucleations, the grid model was expressed as

$$G(t) \times \upsilon(t) = I_S \tag{7}$$

where $G(t)$ is a $n \times n$ time-varying conductance matrix, $v(t)$ is the corresponding time-varying vector of node voltage drops, and I_s is the vector of effective values of the current sources tied to the grid. In this problem, the time scale is the EM time scale, which can be months or years. Instead of direct solution of the system of the Korhonen's equations linked by junction stress/flux continuity boundary conditions, Huang *et al.* [13], [17] have developed a compact model that provides the void nucleation times for the cathodes (electron flow inlet ports), which are characterized by the steady state stresses exceeding the critical stress. Resistance increase of individual branches was calculated with the void growth formalism, which was described in [26]. Because all trees are electrically connected, a void-induced resistance change in one tree can change the currents in all neighboring trees, which can change the volumes of already formed saturated voids, and hence the resistances of the corresponding branches. That triggers a new calculation iteration. This iterative process continues until the voltage drop at some node of the power/ground network reaches a user-specified threshold value, or the total physical time exceeds the required life-time, Fig. 8. The proposed EM assessment method was tested on the IBM power grid benchmark circuits [27], on a 2.3 GHz Linux server with 132 GB memory.

Huang *et al.* [13] have demonstrated for the first time that the Black's equation-based assessment performed on either series or mesh models leads to more pessimistic results when compared with the proposed method, Table I. In Black's equation-based analysis the equation (4) was used to estimate MTTF of single metal line, where $T_{\text{stress}} = 600$ K, $j_{\text{stress}} = 3 \times 10^{10}$ A/m2, $E_a = 0.86$ eV, and MTTFstress was obtained from t_{nuc} calculated under these stressed conditions [17] with the critical stress of 500 MPa. The use/operating conditions were characterized by the constant temperature of 373 K and the branch current densities distributed between 3.4×10^3 and 4.7×10^{10} A/m^2, which were extracted with SPICE simulations.

However, the approach developed in [13] and [17] was very slow, requiring up to 17 hours to estimate the failure time of a 700K node grid. In [21], since the connected branches were replaced by semi-infinite limbs, the atomic flow across the whole tree was not accounted for. Thus, there was a need for a new EM checking approach that accurately models EM degradation using physics-based models, combined with a mesh model to account for redundancy, while being fast enough to be practically useful.

TABLE I
COMPARISON OF POWER GRID MTTF OBTAINED USING BLACK'S MODEL AND PROPOSED MODEL

Power Grid		Time-To-Failure (years)				
		Black's Equation		Proposed Model		
Name	Nodes	Series	Mesh	No saturat.	With saturat.	Run Time
IBMPG2	61797	6.17	12.83	16.85	18.78	6.36 min
IBMPG3	407279	12.79	17.90	23.56	31.97	5.83 hour
IBMPG	474836	13.23	22.27	26.97	33.41	14.71 hour
IBMPG	497658	4.41	12.34	19.13	25.16	40.64 min
IBMPG	807825	8.44	10.89	14.62	19.85	1.75 hour
IBMPG NEW1	715022	12.85	13.96	18.84	25.97	16.78 hour
IBMPG NEW2	715022	12.73	13.84	15.60	21.79	15.32 hour

III. EXTENDED KORHONEN'S MODEL IS AN ACCURATE AND PRACTICAL METHODOLOGY FOR POWER GRID EM ASSESSMENT

This novel approach has been developed recently by Chatterjee *et al.* [16], [18], [28]. While it implements similar physical models as was used by Huang *et al.* [13], [17], the advanced numerical technique developed by Chatterjee *et al.* appears to be a promising approach for EM assessment of power grids in large VLSI circuits. The method consists of decomposing the power grid into a number of interconnect trees, solving the set of discretized PDEs (8) for all branches of each tree characterized by different current densities and geometries (length and width), and linking the solutions at the segment junctions to each other through the proper boundary conditions (BC) given in (9) and (10).

$$\frac{\partial \sigma_n}{\partial t} = \frac{\partial}{\partial x}\left[\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G_n\right)\right] \tag{8}$$

Here, $\sigma_n(x,t)$ is the time-varying hydrostatic stress at location x in the n-th branch of the tree. We use the standard notations: $\kappa_n^2 = D_{eff}^n B_n \Omega / k_B T_n$, and $G_n = eZ\rho j_n / \Omega$, where D_{eff}^n is the effective atomic diffusivity in the n-th branch, B_n is the effective bulk modulus, Ω is the atomic volume, k_B is the Boltzmann's constant, T_n is the absolute temperature, eZ is the effective charge of migrating atoms, ρ is the metal resistivity, and j_n is the electric current density in the n-th branch. The boundary conditions (BC) reflecting the continuity of stress and atomic flux at every junction between neighboring branches take the form:

$$\sigma_n(x,t) = \sigma_{n+1}(x,t), \text{ at } x = x_n,\ t > 0 \tag{9}$$

$$\kappa_n^2\left(\frac{\partial \sigma_n}{\partial x} + G_n\right) = \kappa_{n+1}^2\left(\frac{\partial \sigma_{n+1}}{\partial x} + G_{n+1}\right), \text{ at } x = x_n,\ t > 0. \tag{10}$$

Initial conditions for the equation (8) determine the stress in interconnect trees at t = 0, before the electric stressing was applied. In on-chip interconnects, the metal lines are embedded in a rigid confinement. Because of the difference in the coefficients of thermal expansion (CTE) of the metal (Cu) α_m and confinement (Silicon) α_{conf}, stress is generated as the chip cools down after anneal. This so-called thermal stress can be expressed as:

$$\sigma_n^{T_n}(t) = B_n\big(\alpha_m - \alpha_{conf}\big)(T_{ZS} - T_n(t)) \tag{11}$$

where $\sigma_n^{T_n}(t)$ is the thermal stress, $T_n(t)$ is the temperature of branch b_n and T_{ZS} is the stress-free annealing temperature. In our work, we assume that the initial stress $\sigma_n(0,t)$ in branch b_k is equal to its thermal stress at $t = 0$, so that:

$$\sigma_n(0,t) = \sigma_n^{T_n}(0) \tag{12}$$

Accounting for the temperature distribution across the metal layers is done by employing a compact thermal model that represents a die as array of cuboidal thermal cells with effective local thermal properties. Specifically, each thermal block is represented as a thermal node connected to 6 resistors, a current source and a capacitor. Thermal resistors represent heat propagation in the lateral and vertical directions, a thermal capacitor can be included for transient thermal analysis. The methodology includes three steps: (i) extract effective thermal properties of each thermal cell, (ii) generate thermal netlist of the whole chip, and (iii) calculate temperature at each thermal node by a circuit solver, similarly to what was done in [29].

The effective thermal conductivities are calculated as functions of metal density and routing direction of wires in each metal layer based on the theory of effective thermal properties of anisotropic composite materials [30]. Based on the standard procedure [29], with the extracted thermal resistances, estimated power sources, as well as the thermal boundary conditions, the chip can be represented as a thermal netlist, in which the nodal temperatures correspond to the nodal voltages and the powers corresponds to the current sources. The total power dissipated in a thermal block can be represented as a sum of the average power dissipated by joule heating of the metal branches within the thermal block and the average heating dissipated by the underlying logic due to active switching and leakage currents [22], [23]. The electric circuit solver can then obtain temperature for each thermal node. We generate the thermal grid at t = 0 and calculate the branch diffusivities and thermal stress in all branches at initial temperature. After a void nucleates, the branch currents change. Hence, we update the average powers dissipated by joule heating for all thermal nodes, find the new temperature distribution and update the branch diffusivities and thermal stresses. As an example, we have analyzed the effect of temperature on the lifetimes estimated using the extended Korhonen's model. For this comparison, we used the interconnect tree taken from ibmpg2 grid with 192 branches and high current density profile, with maximum branch current density being 5.31×10^9 A/m^2 [18]. We first estimated the MTTF using the actual temperature distribution, which has varied between 318K and 333K. For this case, the first failure happens around 13.2 yrs. Then, we artificially assumed a constant temperature of 325K throughout the tree. Note that 325K is the average of the actual branch temperatures. In this case, the first failure happens around 20.26 yrs. A higher nominal temperature would result in a lower failure time and vice versa. Hence, temperature distribution plays

a very important role and should be taken into account while doing EM analysis.

It should be mentioned that initial variation in thermal stress, before the electric stressing is applied, can be explained by dependency of the effective bulk modulus B on the line geometry, particularly on its width and aspect ratio, and the grain morphology [31]. Additional residual stress developed across the whole interconnect structure immediately after packaging can be assessed by using the methodology described in [32] and [33]. Stress relaxation, caused mainly by stress-gradient induced atomic diffusion (stress migration - SM), occurring during chip shelf-live can result in a uniform stress distribution within every interconnect tree, [34]. Follow He *et al.* [35], we can assume that those trees that are characterized by residual stresses exceeding the critical stress, can end up with the presence of saturated voids (stress induced voiding - SIV), whose sizes can be estimated from the consumed initial strain, and zero stress everywhere else in the line. Also, the possibility of multi-void generation in interconnect trees should be accounted for. An actual distribution of stress, which is used as an initial stress in the EM analysis, depends on the duration of the chip shelf-live that introduces another uncertainty factor. However, the stress evolution caused by EM in two cases of initially void less line and line with the saturated void is characterized by different kinetics just in the beginning, which disappears at long times, resulting the same steady state stress distributions [36]. Hence, in order to be in a more pessimistic side regarding the EM induced MTTF prediction, we should use as an initial condition the SM induced steady state stress distribution in all analyzed interconnect trees with saturated voids located in trees with residual stresses exceeding the critical one. The BC at the void edge, which is used for calculating the postvoiding stress evolution, takes the form [36]

$$\frac{\partial \sigma\left(x_{edge}, t\right)}{\partial x} = \frac{\sigma\left(x_{edge}, t\right)}{\delta} \tag{13}$$

Here, δ is the thickness of the void interface, $\sigma(x_{edge}, t)$ is the stress near the void edge, which equals to the critical stress at the time of void nucleation. Resolved postvoiding stress evolution kinetics allows us to calculate the void volume evolution from the volume of atoms drifted into the line, $V_{void}(t) = A\int_0^L (\sigma(x,t)/B)dx$, where A is the cross-sectional area and L is the length of the segment. Void evolution kinetics implemented in the resistance evolution computation has replaced the approximation currently employed in [16], [18], and [28] of very fast void growth, which provides very short times (relative to nucleation phase durations) needed to reach void saturation volumes. The latter can generate some noticeable conservatism in the computed grid TTF.

Additional variations of the residual stress can be expected in the junctions between line segments characterized by polygranular and near bamboo structures [31] and in the vicinity (above and below) of interlayer vias [37]. All these variations can be addressed by introducing a lookup table, which provides different values of the effective bulk modulus B corresponding different layout segment configurations.

The discussed above physics provides accurate calculation of the stress evolution inside multi-segment tree. Fig. 9 shows

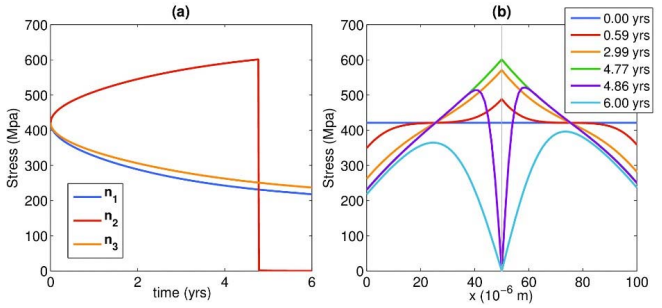

Fig. 9. Evolution of stress at junctions with time, (a) and stress profile evolution with time, (b). Here $L_1 = L_2 = 50$um, and $j_1 = -j_2 = 6e9$ A/m^2, [16].

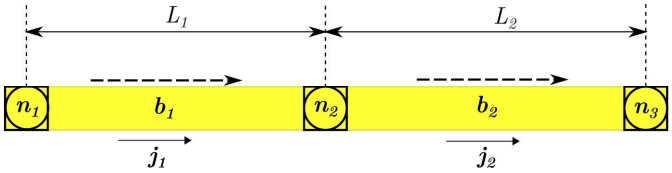

Fig. 10. A simple 3-terminal tree.

the kinetics of stress evolution at all tree junctions and the evolution of the stress distribution across the 3-terminal tree shown in Fig. 10.

The extended Korhonen's model starts out as a system of PDE coupled by the boundary laws (9)–(10), which are then scaled and discretized to reduce the model to a system of ordinary differential equations (ODE), which is shown to be a linear time-invariant (LTI) system. The method then moves on to numerically solve the ODE system at successive time-points to track the stress evolution and find the corresponding time of void nucleation(s).

To account for the random nature of EM degradation, Monte Carlo random sampling is performed to estimate the MTTF. In each Monte Carlo iteration, new randomly generated diffusivities are assigned to all the branches in the grid. This effectively produces a new instance of the whole power grid, which is referred to as a sample grid. Then, the TTF values are generated based on the mesh model, and another based on the series model for comparison purposes. With enough samples, two averages are formed as the estimates of the series MTTF and the mesh MTTF.

Computation speed is enhanced by using a filtering scheme that estimates upfront the set of trees that are most likely to impact the MTTF of the grid, with minimal impact on accuracy. The process also includes a predictive scheme that allows for faster MTTF estimation by extrapolating the solution (stress curve) obtained from a few initial time-points. This has also been shown to have minimal impact on accuracy.

The resulting approach was tested on the same set of IBM power grid benchmarks, [27], on a quad-core 3.4GHz Linux machine with 32GB of RAM. The MTTFs estimated using the physics-based approach were on average 3x longer than those based on a Black's model, supporting the claim that Black's model is not accurate enough for modern power grids and confirming the need for physical models. Having achieved

TABLE II
COMPARISON OF POWER GRID MTTF AS ESTIMATED USING BLACK'S MODEL AND EXTENDED KORHONEN'S MODEL

Power Grid				Black's Model			Extended Korhonen's Model							
							Filtering			Filtering + Predictor				
Grid Name	# nodes	#bra-nches	#trees	μ_s^{blk} (yrs)	μ_m^{blk} (yrs)	t_{blk} (hrs)[a]	μ_s^{act} (yrs)	μ_m^{act} (yrs)	t_{act} (hrs)[a]	μ_s^{pre} (yrs)	μ_m^{pre} (yrs)	t_{pre} (hrs)[a]	$\frac{\mu_m^{\text{act}}}{\mu_m^{\text{blk}}}$	$\frac{t_{\text{act}}}{t_{\text{pre}}}$
ibmpg1	6K	11K	709	5.39	9.13	0.001	4.52	10.69	0.11	4.19	10.90	0.003	1.17	33.59x
ibmpg2	62K	61K	462	2.96	6.33	0.03	6.50	9.72	0.39	6.53	10.11	0.04	1.54	9.86x
ibmpg3	410K	401K	8.1K	2.92	6.62	0.26	4.11	10.04	10.79	4.12	9.95	0.41	1.52	26.61x
ibmpg4	475K	465K	9.6K	1.38	2.97	0.53	4.95	9.45	9.25	4.96	11.95	2.31	3.18	4.01x
ibmpg5	249K	496K	2K	2.26	3.61	0.02	4.56	6.18	0.26	4.50	6.63	0.06	1.71	4.21x
ibmpg6	404K	798K	10.2K	1.20	1.32	0.02	4.79	10.11	4.40	4.84	11.96	0.79	7.67	5.59x
ibmpgnew1	316K	698K	19.5K	1.18	2.64	0.14	2.39	10.36	1.72	2.32	11.64	1.24	3.92	1.39x
ibmpgnew2	718K	698K	19.5K	1.62	4.82	0.68	3.44	6.18	1.22	3.48	6.72	0.43	1.28	2.87x

[a] t_{blk}, t_{act} and t_{pre} denote the run-time(s) for Black's model, Filtering and predictor based approaches, respectively.

a run-time of less than three hours for the largest grid (700K nodes), this approach has been demonstrated as suitable for large VLSI circuits, Table II, [18]. The stress conditions that were used for calculating MTTF were similar to what was mentioned for the table I excepting the critical stress, which was taken as 600 MPa, and the use temperature of 300 K.

In order to show the inaccuracy in Black's model, two scenarios, based on two interconnect trees T_1 and T_2 taken from ibmpg2, have been presented. Both trees are straight metal stripes with 192 branches each. T_1 has a high current density profile, with maximum branch current density being 5.31×10^9 A/m^2 (Fig. 11). In this case, Black's model predicts the first failure time of about 6.2 years, whereas the actual failure time found using the Extended Korhonen's model is about 13.2 years, which is $\sim$ 2x longer. T_2 has a low current density profile, with maximum branch current density being 1.44×10^9 A/m^2 (Fig. 12). Here, due to the Blech effect, Black's model predicts that no failure would occur. However, benefiting from a physical model that accounts for material flow between the branches, it was found that the first failure would occur at about 2.44 years. Thus, Black's model was pessimistic in the first scenario and highly optimistic in the second one. This shows that lifetime estimates using the Black's model can be highly inaccurate.

Developed 1D model has a built-in capability to account an early failure, which happens if a large enough void forms below a via [18]. Removal of a via, as it happens during the early failures, has a significant impact on grid reliability. In our model, once we have determined the void volume, we check for the following two conditions: *i)* is the void located below a via (this is determined based on the geometry of the grid) and *ii)* is the void large enough to disconnect the via. If both conditions are met, this void leads to an early failure, so that we remove the via from the power grid and update the voltage drops and current density values. Impact of the early failure was analyzed using the ibmpg2 grid. It was found that turning off early failures gives an optimistic MTTF estimate, which is 34% longer than the actual MTTF. Details of this case study can be found in [18].

In order to improve model predictability and, as a result, the accuracy of MTTF predictions a number of model enhancements should be done. For example, the methodology

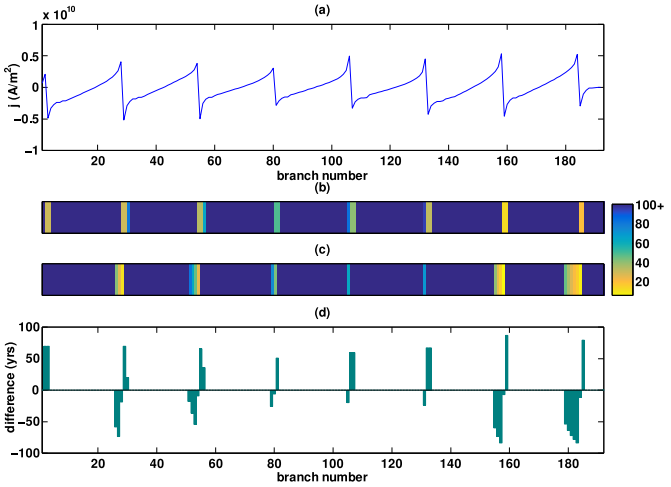

Fig. 11. (a) Current density profile for T_1 and MTTFs estimated using (b) Extended Korhonen's model (MTTF_{ekm}), (c) Black's model (MTTF_{blk}) and (d) $\text{MTTF}_{\text{blk}} - \text{MTTF}_{\text{ekm}}$, [18].

for finding the saturated void volume V_{SV} in interconnect trees should be improved. The currently employed formalism describes V_{SV} for the case of a single line, [13], [16]; it should be extended to the case of a multi-segment interconnect tree, and the effect of the already nucleated voids on new void nucleation and growth should be accounted for. Effect of microstructure on EM-induced stress evolution and voiding should be implemented in a way similar to that discussed by Korhonen *et al.* [38]. Discussed in [39] and [40] effect of the EM induced plasticity, which creates new interfaces for atomic diffusion in later stages of the electromigration process in the form of dislocations and subgrain boundaries parallel to the direction of the current, can be addressed in the discussed 1D modeling by adjusting the atomic diffusivity at the calibration stage. Finally, different types of void growth kinetics should be implemented in the case of initially void-less trees versus trees with preexisting saturated voids, similar to what was proposed in [35].

These model enhancements will require additional spatial discretization of the tree segments and solution of even larger systems of ODEs, which in turn will demand further improvement of the numerical techniques providing a faster

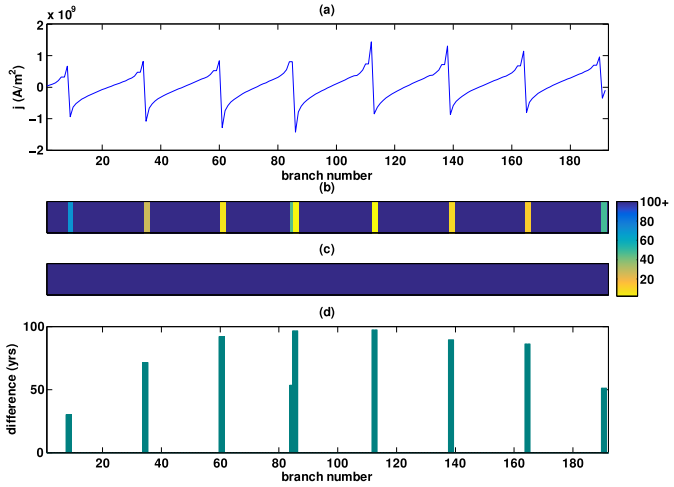

Fig. 12. (a) Current density profile for T_2 and MTTFs estimated using (b) Extended Korhonen's model ($MTTF_{ekm}$), (c) Black's model ($MTTF_{blk}$) and (d) $MTTF_{blk}$ - $MTTF_{ekm}$, [18].

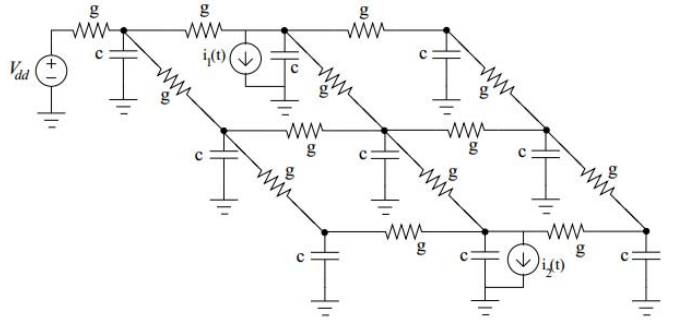

Fig. 13. Power grid schematics with user-provided current sources and voltages.

computation speed. Thus, we can conclude that the critically needed analysis of EM-induced voltage-drop degradation in on-chip power/ground grids is a justification and a strong drive for further development of accurate 1-D EM models and fast simulation techniques, [16].

IV. Conclusion

Despite the need for various additional improvements, the physics-based EM verification and checking methodology that is already available, and the numerical capabilities recently developed, have demonstrated that the industry-accepted Black's model-based EM assessment approach cannot accurately predict life-time of modern power grids. The Black's model based methodology calls for significant over-design, while, today, there is very little margin left for electromigration. It has been demonstrated that the pessimism, which is natural for this methodology, is very high: grids that must survive 10 years, are being designed to survive 40 years or more. One might think that such pessimism is not a bad strategy in VLSI. However, too much pessimism in the power grid can be a big problem. It leads to overuse of metal area, leaving little room for signal routing, which makes EM signoff extremely difficult in modern designs, thus increasing design complexity and design time. In contrast, the newly developed physics-based EM assessment approach provides the MTTF for any given power grid, which can be a DC, RC, or RLC netlist, and user-specified current sources and voltages, Fig. 13. If adopted, this approach can effectively relax the very conservative current density design rules, which can allow many improvements in power, time-to-market and design cost.

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