

RÉSUMÉ

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EDUCATION :

1986-1989: University of Illinois at Urbana-Champaign Urbana, Illinois, USA

Ph.D. degree, Electrical Engineering. Thesis topic: "Probabilistic Simulation for Reliability Analysis of VLSI Circuits," worked with Prof. Ibrahim N. Hajj and Dr. Ping Yang, of Texas Instruments Inc. Research conducted in-part at Texas Instruments in Dallas, Texas.

1985-1986: University of Illinois at Urbana-Champaign Urbana, Illinois, USA

M.S. degree, Electrical Engineering. Thesis topic: "Switch-Level Test Generation for MOS VLSI Circuits," worked with Prof. Ibrahim N. Hajj.

1979-1983: American University of Beirut Beirut, Lebanon

B.E. degree (with distinction), Electrical Engineering. Employed as a part-time teaching assistant in the Electrical Engineering Department.

WORK EXPERIENCE :

Since 1999 : University of Toronto Toronto, Ontario, Canada

Associate Professor (1999-2001), then Professor since 2001 (and Vice-Chair 2004-2007) with the Electrical and Computer Engineering (ECE) Department. Research interests include Computer-Aided Design (CAD) techniques for Integrated Circuits, with the goal of contributing to design methodologies with features that include design for low-power and reliability, early design planning, and physical design verification.

1992-1999 : University of Illinois at Urbana-Champaign Urbana, Illinois, USA

Assistant Professor 1992-1997, then Tenured Associate Professor 1997-1999, with the Electrical & Computer Engineering (ECE) Department and the Coordinated Science Laboratory. Conducted research on power estimation and modeling for VLSI circuits, synthesis and optimization for low-power, ultra low-power circuits, and integrated circuit reliability analysis.

1987-1992 : Texas Instruments Inc. Dallas, Texas, USA

Member of Technical Staff with the Semiconductor Process and Design Center (SPDC) at Texas Instruments. Worked with Dr. J.-H. Chern and Dr. Ping Yang, in the general areas of Technology-CAD, Design for Manufacturing, Design-in Reliability, and Reliability Analysis of VLSI.

PERSONAL BACKGROUND :

Dual US & Canadian Citizen, born in Lebanon, 1960. Speaks fluent English, Arabic, & fair French.

AWARDS :

9. American University of Beirut (AUB), Faculty of Engineering and Architecture (FEA), **The FEA Distinguished Alumnus Award**, *in recognition of groundbreaking contributions to computer-aided design techniques for power management in integrated circuits*, May 2007.
8. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2005, for a patent submission on a low-leakage FPGA routing switch, with Navid Azizi.
7. **Fellow of the IEEE**, *for contributions to estimation and modeling of power dissipation in integrated circuits*, January 2003.
6. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2003, for a patent submission on a low-leakage asymmetric-cell SRAM, with Navid Azizi and Andreas Moshovos.
5. **Infrastructure Award**, Canada Foundation for Innovation (CFI) and Ontario Innovation Trust (OIT), 2001, award of CN\$96,000 for purchase of equipment in support of research.
4. University of Illinois ECE Faculty **Outstanding Teaching Award**, 1999. Also, named, in 1997, to the “Incomplete list of teachers ranked excellent by their students.”
3. National Science Foundation (NSF) **Faculty Early Career Development Award (CAREER)**. Award of US\$200,000, in 1996, to fund work on reliability engineering for integrated circuits.
2. National Science Foundation (NSF) **Research Initiation Award (RIA)**. Award of US\$100,000, in 1993, to fund work on synthesis of reliable and low power VLSI circuits.
1. IEEE Transactions on CAD **Best Paper Award**, in 1992, for the paper “Probabilistic Simulation for Reliability Analysis of CMOS VLSI Circuits,” published in the April 1990 issue.

PATENTS :

Issued:

2. F. N. Najm, A. Moshovos, and N. Azizi, “Low Leakage Asymmetric SRAM Cell Devices,” *US Patent No. 7,307,905*, supported by the Semiconductor Research Corporation (SRC), December 11, 2007.
1. J. H. Anderson and F. N. Najm, “Leakage Power Optimization for Integrated Circuits,” *US Patent No. 6,993,737 B1*, supported by Xilinx Corp., January 31, 2006.

Filed:

4. G. Nabaa, N. Azizi, and F. N. Najm, “A Novel FPGA Architecture with Threshold Voltage Compensation and Reduced Leakage,” *US Patent Application*, supported by Actel Corp., **filed** August 29, 2007.
3. F. N. Najm, “A Novel Second-Order Implicit Numerical Integration Formula which is A-Stable and which Allows One to Use a Fixed Circuit Matrix as Time-Step is Changed in the Simulation of Linear Systems,” *US Patent Application*, supported by Nascentric Corp., **filed** January 3, 2006.
2. N. Azizi, M. M. Khellah, V. De, and F. N. Najm, “Method for Temperature-Dependent Deactivation of Parallel Low-Voltage Circuits,” *US Patent Application*, supported by Intel Corp., **filed** November 2004.
1. F. N. Najm and R. J. Shank, “Apparatus and Methods for Characterizing Electronic Circuits having Multiple Power Supplies,” *US Patent Application No. 09/933,532*, supported by Silicon Metrics Corp., **filed** August 20, 2001.

Other Disclosures:

3. F. N. Najm and S. Onaissi, “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners,” *Invention Disclosure*, University of Toronto, April 2006.

2. N. Azizi, K. Pagiamtzis, and F. N. Najm, "A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting Match Scheme," *Invention Disclosure*, University of Toronto, October 2005.
1. F. N. Najm, "A Logic Design Technique for Ultra Low-Power Logic Circuits based on Dynamic Control of the Standby Leakage Current," *Invention Disclosure*, University of Illinois at Urbana-Champaign, June 1996.

INVITED TALKS :

12. F. N. Najm, "Power Management for VLSI: The History and the Outlook," plenary talk, *IEEE 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14–17, 2008.
11. F. N. Najm, "Power Management for VLSI Circuits and the Need for High-Level Power Modeling and Design Exploration," plenary talk, *IEEE/FMCAAD Formal Methods in Computer Aided Design*, Austin, TX, Nov. 11-14, 2007.
10. F. N. Najm, "Power Management for VLSI Circuits," *6th Faculty of Engineering and Architecture (FEA) Student Conference*, American University of Beirut, May 23–24, 2007.
9. F. N. Najm, "On the Need for Statistical Timing Analysis," panel discussion, *ACM/IEEE Design Automation Conference*, Anaheim, CA, June 13–17, 2005.
8. F. N. Najm, "Power Estimation and Modeling for VLSI Circuits," *Distinguished Lecture Colloquium*, Dept. of Electrical and Computer Engineering, University of Toronto, Feb. 2, 1999.
7. F. N. Najm, "High-Level Power Estimation and Modeling," Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, April 23, 1998.
6. F. N. Najm, "High-Level Power Estimation and Modeling," *Dept. of Electrical Engineering/Systems*, University of Southern California, March 1998.
5. F. N. Najm, "Low-Power Design Methodology: Power Estimation and Optimization," *Great Lakes Symposium on VLSI*, March 1997.
4. F. N. Najm, "Power Estimation Techniques for Integrated Circuits," *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 5–9, 1995.
3. F. N. Najm, "Power Estimation Techniques for VLSI Circuits," *ECE Dept. Distinguished Lecture Series*, Carnegie Mellon University, October 1995.
2. F. N. Najm, "Feedback, correlation, and delay concerns in the power estimation of VLSI circuits," *Design Automation Conference*, San Francisco, CA, June 12–16, 1995.
1. F. N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits," *ECE Dept. Graduate Seminar*, University of Iowa, Feb. 1995.

SERVICE IN PROFESSIONAL SOCIETIES :

1. **Associate Editor**, IEEE Transactions on Computer-Aided Design, since 2001.
2. **Associate Editor**, IEEE Transactions on VLSI, 1997–2002.
3. **Editor**, Simulation and Modeling Column, IEEE Circuits and Devices Magazine, 1995–1997.
4. **Guest Editor**, VLSI Design journal, 1995.
5. **Guest Editor**, High Speed Electronics and Systems journal, 1995.
6. **General Chairman**, International Symposium on Low-Power Electronics and Design, 1999.
7. **Technical Program Co-Chairman**, International Symposium on Low-Power Electronics and Design, 1998.

8. **Technical Program Chairman**, Great Lakes Symposium on VLSI, University of Illinois, 1997.
9. **Fellow** of the IEEE since Jan. 2003, member of the Circuits and Systems Society.
10. **Technical Committee Member** of:
 - Design Automation Conference (DAC 1998-99, 2006-08)
 - International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (the TAU Workshop) (TAU 2007-08)
 - International Conference on Computer-Aided Design (ICCAD 1995-97, 2001-2003)
 - International Symposium on Low-Power Electronics and Design (ISLPED 1995-2000)
 - International Symposium on Quality Electronic Design (ISQED 2001-2004)
 - Custom Integrated Circuits Conference (CICC 1994)
 - International Conference on Computer Design (ICCD 1999)
 - International Symposium on VLSI Technology, Systems, & Applications, Taiwan (VLSITSA 93)
 - International Workshop on Low Power Design (IWLDP 1994)
11. **Executive Committee Member**, International Symposium on Low-Power Electronics and Design, since 1999.
12. **Workshop Co-chairman**, Illinois Computer Affiliates Program (ICAP) workshop, University of Illinois at Urbana-Champaign, 1993.
13. **Session Chairman**, on numerous occasions for ICCAD, VLSITSA, DAC, IWLDP, and ISLPED.

SERVICE IN THE UNIVERSITY :

At the University of Toronto

17. Member, Examination Committee, Faculty of Applied Science and Engineering, 2008-2009
16. Chair, ECE Promotions Committee, 2006-2007
15. Member, Faculty Vice-Dean Search Committee, 2006-2007
14. Member, ECE PTR Committee, 2004-2007
13. Chair, ECE Computer Systems User Advisory Committee, 2005-2007
12. Chair, ECE Awards Committee, 2004-2007
11. Member, ECE Chair's Advisory Committee, 2004-2007
10. Member, ECE Department Executive Committee, 2004-2007
9. Vice-Chair, ECE Department, 2004-2007
8. Member, Faculty Senior Promotions Committee, 2003-2007
7. Chair, ECE Department Governance Committee, 2003-2004
6. Served on the Strategic Planning Organizing Committee, 2003-2004
5. Chairman of the Computer and Communications Faculty Search Committee, 2002-2003
4. Chairman of the Computer Faculty Search Committee, 2001-2002
3. Chairman of the Computer Engineering Group, 2000-2003
2. Served on the Group Review Committee, 1999-2000
1. Served on the Computer Engineering Group Search Committee, 1999-2000

At the University of Illinois

6. ECE Department Computer Resources and Education Committee, 1999
5. Circuits and Signal Processing Area Committee Chair, 1997-1998
4. ECE Department Curriculum Committee, 1996-1999
3. Served on the ECE Department ABET Accreditation Committee, 1994-1995

2. Served on the ECE Department Graduate Committee, 1994–1995
1. Chairman, CSL Black/Whiteboard Committee, 1992–1993

CONSULTING ACTIVITIES :

19. Member, External Advisory Board for the Department of Electrical and Computer Engineering at the American University of Beirut, Dec. 2008 – Dec. 2010.
18. Nascentric Inc., Austin, TX, 2008.
17. Nascentric Inc., Austin, TX, 2007.
16. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2007.
15. Synopsys Inc., Mountain View, CA, 2006.
14. Nascentric Inc., Austin, TX, 2005.
13. Nascentric Inc., Austin, TX, 2004.
12. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2003.
11. Silicon Metrics Corporation, Austin, TX, 1999–2003.
10. ATI Technologies Inc., Unionville, ON, 2000.
9. Actel Corp., Sunnyvale, CA, 2000.
8. Taveren Technology, Austin, TX, 1998.
7. Synopsys Corporation, Mountain View, CA, 1997.
6. International Business Machines (IBM) Corporation, Fishkill, NY, 1996, 1997.
5. Synopsys Corporation, Mountain View, CA, 1996.
4. Intel Corp., (Visiting Faculty/Consultant) Folsom, CA, 1996.
3. Texas Instruments Incorporated, Dallas, TX, 1995.
2. Intel Corp., (Visiting Faculty/Consultant) Santa Clara, CA, 1994.
1. Dimensions in Quick Design Turnaround (DQDT), Carlsbad, CA, 1994.

TUTORIALS AND TECHNOLOGY TRANSFER :

5. Full-day tutorial, with B. Krauter (IBM), R. Panda (Freescale), and E. Chiprout (Intel), on “Design and Analysis of High-Performance Package and Die Power Delivery Networks,” *ACM/IEEE 44th Design Automation Conference (DAC-07)*, San Diego, CA, June 9, 2007.
4. Full-day tutorial, with A. Devgan (IBM), S. Narendra (Intel), and D. Blaauw (Michigan), on “Leakage Issues in IC Design,” *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 9–13, 2003.
3. Full-day tutorial, with A. Chandrakasan (MIT) and R. Panda (Freescale), on “Low Voltage/Low Power Design Methodologies and CAD,” *IEEE International Conference on Computer-Aided Design*, November 1999.
2. Technology Transfer Course, “Power Estimation Tools for VLSI Circuits,” for the Semiconductor Research Corporation (SRC), University of Illinois, Urbana, IL, June 1996.
1. Short course, “Dynamics of Physical Systems Under Noise,” for Texas Instruments Inc., Dallas, TX, March 1994.

UNIVERSITY COURSES TAUGHT :

At the University of Illinois

1. ECE-325, Introduction to VLSI Systems Design. This is a 4th year course, but was also taken by some graduate students. In my first semester on campus, I did a major overhaul of this course, by updating the material and bringing in the latest material from my industrial practice.

2. ECE-342, Microelectronics. This is a 3rd year course taken by about 100 students. I was course director for this course; I was also responsible for selection of a new text and for restructuring the course material.
3. ECE-484, Reliability Engineering for Integrated Circuits. This is a graduate course which I created. Few universities teach courses on this topic which is becoming increasingly important for today's advanced technology. Thus, this course is a valuable addition to the curriculum. The course attracted 25 students in the first semester that it was offered. My course notes have been incorporated into a textbook on this material, in collaboration with a colleague from Texas Instruments, published by John Wiley and Sons.

At the University of Toronto

4. ECE-451, VLSI Systems. This is a 4th year course. In my first offering of the course, I completely redid the lecture part, using my previous VLSI course at Illinois as a basis. In the 2nd offering of this, I upgraded the labs, so that the students are now using custom IC design software, such as MicroMagic, Cadence, and Synopsys tools, instead of FPGAs.
5. ECE-1768, Reliability of Integrated Circuits. This is a new graduate course which I created, along the lines of my reliability course at Illinois.

GRADUATE STUDENT SUPERVISION :

	Graduated	Current
PhD	13	3
MASc	25	3
MEng	0	0

CURRENTLY SUPERVISED :

1. Meric Aydonat, 2008–now. Working on **MASc**.
2. Mehmet Avci, 2008–now. Working on **MASc**.
3. Ankit Goyal, 2008–now. Working on **MASc**.
4. Khaled R. Heloue, 2003–now, **MASc June 2005** on “Statistical Timing Analysis under Process Variations.” Working on **PhD** with me since July 2005.
5. Sari Onaissi, 2005–now, **MASc June 2007** on “A Linear-Time Approach for Static Timing Analysis Covering All Process Corners.” Working on **PhD** with me since July 2007.
6. Nahi Abdul Ghani, 2005–now, **MASc June 2007** on “Handling Inductance in Early Power Grid Verification.” Working on **PhD** with me since July 2007.

PREVIOUSLY SUPERVISED :

At the University of Toronto

12. Imad Ferzli, 2001–2009, **MASc Dec. 2003** on “Power Grid Statistical Analysis and Verification in Presence of Leakage Current Variations,” **PhD Feb. 2009** on “Verification and Planning of the Power Delivery Network in Integrated Circuits Under Design Uncertainties.” Now at CPPIB in Toronto.
11. Navid Azizi, 2001–2007, **MASc Dec. 2002** on “Low-Leakage Asymmetric-Cell SRAM”, **PhD May 2007** on “Challenges in Nanometre Digital Integrated Circuit Design.” Now at Altera Corp. in Toronto.

10. Bin Wu, 2001-2006, **PhD June 2006** on “Dynamic Range Estimation and Bitwidth Determination.” Now at Freescale Corp. in Phoenix, Arizona.
9. Denis Kouroussis, 2000-2006, **PhD January 2006** on “Power Grid Verification.” Now at ATI Technologies, Unionville, Ontario, Canada.
8. Kay Chan, 2003-2005, **MASc August 2005** on “Exploring Spatial Locality in VLSI On-Chip Power Grid.” Now at Intellon Corp. in Toronto.
7. Georges Nabaa, 2003-2005, **MASc July 2005** on “Minimization of Threshold-Voltage Variations and Their Impact in Circuits and FPGAs.” Now at Actel Corp. in San Jose, California.
6. David Ng, 2003-2005, **MASc July 2005** on “Modeling Circuit-Level Leakage Current Using Algebraic Decision Diagrams.” Went on to study law at the University of Toronto.
5. Jason Anderson, 2001-2005, **PhD June 2005** on “Power Optimization and Prediction Techniques for FPGAs.” Now at Xilinx Corp. in Toronto.
4. Maha Nizam, 2003-2005, **MASc June 2005** on “Power Grid Voltage Integrity Verification.” Graduated and left the country.
3. Rubil Ahmadi, 2001-2003, **MASc 2003** on “Timing Analysis in Presence of Power Supply and Ground Voltage Variations.” Now at ATI Technologies in Unionville, Ontario, Canada.
2. Roman Kordasiewicz, 2000-2002, **MASc 2002** on “Timing Verification of PD-SOI Circuits”. Went on to do a PhD at McMaster University in Hamilton, Ontario.
1. Mehrdad Shahriari, 2000-2001, **MASc 2001** on “A Gate-Level Timing Model for SOI Circuits”. Now at Genum Corp. in Oakville, Ontario, Canada.

At the University of Illinois

15. Kavel Buyuksahin, 1998-2003, **MS 1999** on “High-Level Interconnect Capacitance Estimation”, **PhD 2003** on “Early Power Estimation for VLSI Circuits”. At Intel Corp., in Portland, OR, USA.
14. Srinivas Bodapati, 1998-2003, **MS 1999** on “Pre-Layout Estimation of Individual Wire Lengths”, **PhD 2003** on “Bottom-up High-Level Current Macro-models for Logic Blocks”. At Intel Corp., in Santa Clara, CA, USA.
13. Joseph Kozhaya, 1996-2001, **MS 1997** on “Power Estimation for Sequential Circuits”, **PhD 2001** on “Analysis and Design of Power and Ground Networks for VLSI Circuits”. At IBM Corp., in Burlington, Vermont, USA.
12. Subodh Gupta, 1995-2000, **MS 1997** on “Power Macromodeling for High Level Power Estimation”, **PhD 2000** on “Bottom-up High-Level Power Modeling and Estimation”. At Cadence Design Systems, Inc., in California, USA.
11. Rouwaida Kanj, 1998-2000, **MS 2000** on “High Level Design Exploration and Optimization”. Went on to do a PhD with another Professor at Illinois, then took a position with IBM Austin Research Labs, in Austin, TX.
10. Xiaochun Tan (co-advised with E. Rosenbaum), 1998-2000, **MS 2000** on “Silicon-on-Insulator MOSFET Body Voltage Model for Application in a Timing Simulator”. At Freescale Corp. in Illinois.
9. Gilbert Yoh, 1997-1999, **MS 1999** on “A Statistical Model for Electromigration Failures”. At Agilent Technologies Inc., in Colorado, USA.
8. Mahadevamurthy Nemani, 1995-1998, **PhD 1998** on “High-Level Power Estimation”. At Intel Corp. in California, USA.
7. Luis Amaya (co-advised with P. Krein), 1995-1998, **PhD 1998** on “Simulation and Design of DC to DC Power Converters”.

6. Rajendran Panda, 1993–1996, **PhD 1996** on “Synthesis Techniques for VLSI Low-Power Circuits”. At Freescale Corp. in Austin, Texas, USA.
5. Jonathan Halter, 1995–1997, **MS 1997** on “A Gate-Level Leakage Power Reduction Method”. At Freescale Corp. in Austin, Texas, USA.
4. Vikram Saxena (co-advised with I. Hajj), 1995–1996, **MS 1996** on “Power Estimation for Sequential Circuits”. At Synopsys, Inc., in California, USA.
3. Michael Xakellis, 1993–1994, **MS 1994** on “Estimating Node Transition Densities with Statistical Simulation Techniques”. At Mercury Interactive Corp. in California, USA.
2. Yimin Zhang, 1993–1994, **MS 1994** on “Estimation of Node Maximum Transition Density”. At Intel Corp. in California, USA.
1. Harish Kriplani (co-advised with I. Hajj), 1991–1993, **PhD 1993** on “Worst Case Voltage Drops in Power and Ground Buses of CMOS VLSI Circuits”. At Cadence Design Systems, Inc., in California, USA.

PUBLICATIONS :

Books

- [1] G. K. Yeap and F. N. Najm, Editors, *Low Power VLSI Design and Technology*. Singapore: World Scientific Publishing Co., 1996 (ISBN: 9-810-22518-0).
- [2] E. A. Amerasekera and F. N. Najm, *Failure Mechanisms in Semiconductor Devices*, 2nd Ed.. Chichester: John Wiley & Sons, 1997 (ISBN: 0-471-95482-9).
- [3] F. N. Najm, “Power Estimation and Optimization,” in *Encyclopedia of Electrical and Electronics Engineering*. New York, NY: John Wiley & Sons, February 1999.

Journal Papers

- [1] R. Burch, J. Hall, F. Najm, D. Hocevar, P. Yang, and M. McGraw, “A CAD system for modeling voltage drop and electromigration in VLSI metallization patterns,” *Texas Instruments Technical Journal*, vol. 5, no. 3, pp. 74–84, May-June 1988.
- [2] F. Najm, R. Burch, P. Yang, and I. Hajj, “Probabilistic simulation for reliability analysis of CMOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 4, pp. 439–450, April 1990 (Errata in July 1990). (**Best Paper Award**)
- [3] F. Najm and I. Hajj, “The complexity of fault detection in MOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 8, pp. 995–1001, September 1990.
- [4] F. Najm, I. Hajj, and P. Yang, “An extension of probabilistic simulation for reliability analysis of CMOS VLSI circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 10, no. 11, pp. 1372–1381, November 1991.
- [5] F. Najm, “Transition density: a new measure of activity in digital circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 12, no. 2, pp. 310–323, February 1993.
- [6] R. Burch, F. Najm, P. Yang, and T. Trick, “A Monte Carlo approach for power estimation,” *IEEE Transactions on VLSI Systems*, vol. 1, no. 1, pp. 63–71, March 1993.
- [7] F. Najm, “Low-pass filter for computing the transition density in digital circuits,” *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, pp. 1123–1131, September 1994.
- [8] F. Najm, “A survey of power estimation techniques in VLSI circuits,” *IEEE Transactions on VLSI Systems*, vol. 2, no. 4, pp. 446–455, Dec. 1994. (**Invited Paper**).

- [9] H. Kriplani, F. N. Najm, and I. Hajj, "Pattern independent maximum current estimation in power and ground buses of CMOS VLSI circuits: algorithms, signal correlations, and their resolution," *IEEE Transactions on Computer-Aided Design*, vol. 14, no. 8, pp. 998–1012, August 1995.
- [10] M. Nemani and F. N. Najm, "Towards a high-level power estimation capability," *IEEE Transactions on Computer-Aided Design*, vol. 15, no. 6, pp. 588–598, June 1996.
- [11] F. N. Najm and M. G. Xakellis, "Statistical estimation of the switching activity in VLSI circuits," *VLSI Design*, vol. 7, no. 3, pp. 243–254, 1998.
- [12] R. Panda and F. N. Najm, "Post-mapping transformations for low-power synthesis," *VLSI Design*, vol. 7, no. 3, pp. 289–301, 1998.
- [13] M. Nemani and F. N. Najm, "High-level area and power estimation for VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 18, no. 6, pp. 697–713, June 1999.
- [14] S. Gupta and F. N. Najm, "Power modeling for high level power estimation," *IEEE Transactions on VLSI Systems*, vol. 8, no. 1, pp. 18–29, February 2000.
- [15] S. Gupta and F. N. Najm, "Analytical models for RTL power estimation of combinational and sequential circuits," *IEEE Transactions on Computer-Aided Design*, vol. 19, no. 7, pp. 808–814, July 2000.
- [16] J. N. Kozhaya and F. N. Najm, "Power estimation for large sequential circuits," *IEEE Transactions on VLSI Systems*, vol. 9, no. 2, pp. 400–407, April 2001.
- [17] S. Bodapati and F. N. Najm, "Pre-layout estimation of individual wire lengths," *IEEE Transactions on VLSI Systems*, vol. 9, no. 6, pp. 943–958, December 2001.
- [18] V. Saxena, F. N. Najm, and I. N. Hajj, "Estimation of state line statistics in sequential circuits," *ACM Transactions on the Design Automation of Electronic Systems*, vol. 7, no. 3, pp. 455–473, July 2002.
- [19] S. Ramprasad, I. N. Hajj, and F. N. Najm, "A technique for improving dual-output domino logic," *IEEE Transactions on VLSI Systems*, vol. 10, no. 4, pp. 508–511, August 2002.
- [20] J. N. Kozhaya, S. R. Nassif, and F. N. Najm, "A multigrid-like technique for power grid analysis," *IEEE Transactions on Computer-Aided Design*, vol. 21, no. 10, pp. 1148–1160, October 2002.
- [21] S. Gupta and F. N. Najm, "Energy and peak-current per-cycle estimation at RTL," *IEEE Transactions on VLSI Systems*, vol. 11, no. 4, pp. 525–537, August 2003.
- [22] N. Azizi, F. N. Najm, and A. Moshovos, "Low-leakage asymmetric-cell SRAM," *IEEE Transactions on VLSI Systems*, vol. 11, no. 4, pp. 701–715, August 2003.
- [23] J. H. Anderson and F. N. Najm, "Power estimation techniques for FPGAs," *IEEE Transactions on VLSI Systems*, vol. 12, no. 10, pp. 1015–1027, October 2004.
- [24] A. Moshovos, B. Falsafi, F. N. Najm, and N. Azizi, "A case for asymmetric-cell cache memories," *IEEE Transactions on VLSI Systems*, vol. 13, no. 7, pp. 877–881, July 2005.
- [25] K. M. Buyuksahin and F. N. Najm, "Early power estimation for VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 24, no. 7, pp. 1076–1088, July 2005.
- [26] I. A. Ferzli and F. N. Najm, "Analysis and verification of power grids considering process-induced leakage current variations," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 1, pp. 126–143, January 2006.
- [27] J. H. Anderson and F. N. Najm, "Active leakage power optimization for FPGAs," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 3, pp. 423–437, March 2006.
- [28] S. Bodapati and F. N. Najm, "High-level current macro-model for logic blocks," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 5, pp. 837–855, May 2006.

- [29] B. Wu, J. Zhu, and F. N. Najm, "Dynamic range estimation," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 9, pp. 1618–1636, September 2006.
- [30] D. Kouroussis, R. Ahmadi, and F. N. Najm, "Voltage-aware static timing analysis," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 10, pp. 2156–2169, October 2006.
- [31] F. N. Najm, N. Menezes, and I. A. Ferzli, "A yield model for integrated circuits and its application to statistical timing Analysis," *IEEE Transactions on Computer-Aided Design*, vol. 26, no. 3, pp. 574–591, March 2007.
- [32] N. Azizi, M. M. Khellah, V. De, and F. N. Najm, "Variations-aware low-power design and block clustering with voltage scaling," *IEEE Transactions on VLSI Systems*, vol. 15, no. 7, pp. 746–757, July 2007.
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Table 2. Summary of funding (grants and contracts) (1k=1,000, U\$=US Dollars, C\$=Canadian Dollars).
In case of joint projects, the average per PI is shown.

Year	Total	U of IL	NSF	Altera	Intel	DEC	Rockwell	SRC	UofT	AMD	Altera	CRD	NIT	NSERC	CFI	Micronet
1992	C\$115k	U\$95k														
1993	C\$75k		U\$25k		U\$33k											
1994	C\$164k		U\$25k		U\$68k	U\$10k		U\$17k								
1995	C\$206k		U\$25k		U\$78k	U\$10k	U\$20k	U\$17k								
1996	C\$214k		U\$65k		U\$45k	U\$10k	U\$20k	U\$17k								
1997	C\$208k		U\$80k				U\$20k	U\$50k								
1998	C\$193k		U\$80k					U\$50k								
1999	C\$594k		U\$152k		U\$17k			U\$140k	C\$110k				C\$25k			
2000	C\$336k		U\$80k					U\$75k					C\$25k	C\$37k	C\$24k	C\$20k
2001	C\$423k							U\$156k						C\$37k	C\$24k	C\$120k
2002	C\$332k							U\$109k						C\$37k	C\$24k	C\$100k
2003	C\$305k							U\$146k							C\$24k	C\$76k
2004	C\$240k							U\$86k						C\$37k		C\$91k
2005	C\$299k				U\$80k			U\$86k			C\$30k	C\$26k		C\$42k		
2006	C\$267k			U\$25k	U\$55k			U\$69k			C\$30k	C\$26k		C\$42k		
2007	C\$202k				U\$80k			U\$69k						C\$42k		
2008	C\$238k				U\$25k			U\$159k						C\$42k		
2009	C\$212k							U\$90k		C\$30k		C\$50k		C\$42k		
2010	C\$170k							U\$90k		C\$30k		C\$50k				
2011	C\$80k									C\$30k		C\$50k				
Total	C\$4,872k	U\$95k	U\$532k	U\$25k	U\$481k	U\$30k	U\$60k	U\$1,426k	C\$110k	C\$90k	C\$30k	C\$202k	C\$50k	C\$358k	C\$96k	C\$407k

GRANTS AND CONTRACTS :

Title: Power Grid Verification
Principal Investigators: F. N. Najm
Sponsor: Natural Sciences and Engineering Research Council (NSERC) CRD Grant
Program: Collaborative Research and Development
Period: 3 years 2009-2012
Amount: CN\$50k/year

Title: Power Grid Verification
Principal Investigators: F. N. Najm
Sponsor: Advanced Micro Devices (AMD), Inc.
Program: Base Funding
Period: 3 years 2009-2012
Amount: CN\$30k/year

Title: Algorithms for Block-Based Parameterized Timing
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Base Funding
Period: 1 year 2008-2009
Amount: US\$25k/year

Title: Vectorless/Early Power Grid Verification
Principal Investigators: F. N. Najm
Sponsor: Semiconductor Research Corporation
Program: Base Funding
Period: 3 years 2008-2011
Amount: US\$90k/year

Title: Parameterized Timing
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Base Funding
Period: 1 year 2007-2008
Amount: US\$25k/year

Title: Vectorless Power Grid Verification and Optimization
Principal Investigators: F. N. Najm
Sponsor: Semiconductor Research Corporation
Program: Base Funding
Period: 3 years 2006-2009
Amount: US\$69k/year

Title: Vectorless Power Grid Verification and Optimization
Principal Investigators: F. N. Najm
Sponsor: Altera Corporation
Program: Base Funding
Period: 1 year 2006-2007
Amount: US\$25k/year

Title: Power Delivery Verification and & Optimization
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Base Funding
Period: 3 years 2005-2008
Amount: US\$55k/year

Title: Statistical Timing Analysis & Optimization
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Base Funding
Period: 1 year 2005-2006
Amount: US\$25k/year

Title: Statistical Timing Analysis for FPGAs
Principal Investigators: F. N. Najm
Sponsor: Altera Corporation
Program: Base Funding and Matching Funds
Period: 1 year 2005-2006
Amount: CN\$30k/year

Title: Statistical Timing Analysis for FPGAs
Principal Investigators: F. N. Najm
Sponsor: Natural Sciences and Engineering Research Council (NSERC) CRD Grant
Program: Collaborative Research and Development
Period: 2 years 2005-2007
Amount: CN\$26K/year

Title: Enabling the Design of High-Performance VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Micronet
Program: Base Funding and Matching Funds
Period: 1 year 2004-2005
Amount: CN\$91k/year

Title: Computer-Aided Design for High-Performance Nanoelectronic Integrated Circuits
Principal Investigators: F. N. Najm
Sponsor: Natural Sciences and Engineering Research Council (NSERC)
Program: Research Grants
Period: 5 years 2005-2009
Amount: CN\$42k/year

Title: Enabling the Design of High-Performance Low-Voltage VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Micronet
Program: Base Funding and Matching Funds
Period: 1 year 2003-2004
Amount: CN\$76k/year

Title: Timing Verification and Optimization Considering Supply and Process Variations
Principal Investigators: F. N. Najm
Sponsor: Semiconductor Research Corporation
Program: Computer-Aided Design and Test Sciences
Period: 3 year 2003-2006
Amount: US\$86k/year

Title: Enabling the Design of High-Performance Low-Voltage VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: Micronet

Program: Base Funding and Matching Funds

Period: 1 year 2002-2003

Amount: CN\$100k/year

Title: Power-Aware Cache Coherence & Hierarchies for High-Performance SMP Servers

Principal Investigators: A. Moshovos, B. Falsafi, and F. N. Najm

Sponsor: Semiconductor Research Corporation

Program: Integrated Circuits and Systems Research

Period: 3 year 2001-2004

Amount: US\$174k/year

Title: Enabling the Design of Low-Power and Reliable VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: Micronet

Program: Base Funding and Matching Funds

Period: 1 year 2001-2002

Amount: CN\$120k/year

Title: High-Performance Systems-on-Chip: Design, IP Reuse, and CAD

Principal Investigators: F. N. Najm, D. Kundur, K. Phang, A. Sheikholeslami, A. Veneris, J. Zhu

Sponsor: Canada Foundation for Innovation

Program: New Opportunities (Equipment Proposal - Infrastructure)

Period: 4 years 2000-2004

Amount: CN\$142k/year

Title: Enabling the Design of Low-Power VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: Micronet

Program: Base Funding

Period: 1 year 2000-2001

Amount: CN\$20k/year

Title: Computer-Aided Design for Low Power and Reliable VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: Natural Sciences and Engineering Research Council (NSERC)

Program: Research Grants

Period: 4 years 2000-2004

Amount: CN\$37k/year

Title: SOI-Specific Design Tools and Methodology

Principal Investigators: F. N. Najm

Sponsor: Semiconductor Research Corporation

Program: Computer-Aided Design and Test Sciences

Period: 2.5 years 2000-2002 (continued from UIUC below)

Amount: US\$48.5k/year

Title: Development of Computer Aided Design Tools and Methodologies for Low Power, Reliable, and High Performance VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: University of Toronto

Program: Nortel Institute

Period: 2 years 1999–2000

Amount: CN\$25k/year

Title: CAD for Low-Power and Reliability

Principal Investigators: F. N. Najm

Sponsor: Connaught Fund at University of Toronto

Program: Start-up Funds

Period: 1999

Amount: CN\$10k

Title: CAD for Low-Power and Reliability

Principal Investigators: F. N. Najm

Sponsor: University of Toronto

Program: Start-up Funds

Period: 1999

Amount: CN\$100k

Title: SOI-Specific Physical Design Flow

Principal Investigators: F. N. Najm and E. Rosenbaum

Sponsor: Semiconductor Research Corporation

Program: Computer-Aided Design and Test Sciences

Period: 0.5 years 1999 (1/2 transferred to Toronto)

Amount: US\$97k/year

Title: Equipment Acquisition in Support of Research into the Design of Next-Generation High-Speed System-on-a-Chip Designs

Principal Investigators: F. N. Najm, with I. N. Hajj, S.-M. Kang, E. Rosenbaum, and N. Shanbhag

Sponsor: National Science Foundation

Program: MRI

Period: 1999

Amount: US\$360k

Title: CAD for Low-Power and Reliability

Principal Investigators: F. N. Najm

Sponsor: Intel Corporation

Program: Equipment Donation

Period: 1999

Amount: US\$17k

Title: High-Level Delay Estimation for VLSI Circuits

Principal Investigators: F. N. Najm

Sponsor: Semiconductor Research Corporation

Program: One time seed money - gift

Period: 1999

Amount: US\$15k

Title: High-Level Power Estimation for VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Semiconductor Research Corporation
Program: IBM customization funds
Period: 3 years 1999–2001
Amount: US\$50k/year

Title: High-Level Power Estimation for VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Semiconductor Research Corporation
Program: TI customization funds
Period: 3 years 1997–1999
Amount: US\$50k/year

Title: An Integrated Design Methodology for Low-Power DSP and Communications Systems
Principal Investigators: F. N. Najm, with I. N. Hajj and N. Shanbhag
Sponsor: National Science Foundation
Program: CISE
Period: 4 years 1997–2000
Amount: US\$470k total

Title: Reliability Engineering for Integrated Circuits
Principal Investigators: F. N. Najm
Sponsor: National Science Foundation
Program: CAREER Award
Period: 5 years 1996–2000
Amount: US\$200k total

Title: Acquisition of Research Equipment for High-Speed Computing and Networking Initiative
Principal Investigators: R. Iyer, with F. N. Najm, B. Hajek, W. Sanders, and W. K. Jenkins
Sponsor: National Science Foundation
Program: Advanced Research Infrastructure
Period: 1996
Amount: US\$725k

Title: Power Estimation
Principal Investigators: F. N. Najm, with I. N. Hajj, S.-M. Kang, and E. Rosenbaum
Sponsor: Semiconductor Research Corporation
Program: Illinois SRC project
Period: 3 years 1994–1996
Amount: US\$200k/year

Title: Low-Power Design Tools and Methodology
Principal Investigators: F. N. Najm
Sponsor: Rockwell Corporation
Program: Rockwell Foundation
Period: 3 years 1995–1997
Amount: US\$60k total

Title: Power Estimation
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Equipment Donation
Period: 1995
Amount: US\$15k

Title: Power Estimation
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Visiting Faculty Award
Period: 1994
Amount: US\$5k

Title: High-Level Power Estimation in VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Intel Corporation
Program: Corporate Research
Period: 3 years 1994–1996
Amount: US\$30k, US\$30k, US\$45k

Title: Power Estimation for VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: Digital Equipment Corporation
Period: 3 years 1994–1996
Amount: US\$30k total

Title: Power Estimation in VLSI Circuits
Principal Investigators: F. N. Najm and I. N. Hajj
Sponsor: Intel Corporation
Program: Corporate Research
Period: 3 years 1993–1995
Amount: US\$33k/year

Title: Synthesis of Reliable and Low-Power VLSI Circuits
Principal Investigators: F. N. Najm
Sponsor: National Science Foundation
Program: RIA Award
Period: 4 years 1993–1996
Amount: US\$100k total

Title: Timing Analysis of Digital Circuits in the Presence of Process Variations
Principal Investigators: F. N. Najm
Sponsor: University of Illinois
Program: Research Board
Period: 1992
Amount: US\$25k

Title: CAD for Low-Power and Reliability
Principal Investigators: F. N. Najm
Sponsor: University of Illinois
Program: Start-up Funds
Period: 1992
Amount: US\$70k

REFERENCES :

Available upon request.
