

A Low-Voltage Current-Controlled Oscillator with Low Supply Dependency

Amir M. Sodagar¹, S. M. Fakhraie², K. C. Smith³

1. *Electrical Eng. Dept., S. Rajaei Univ., Lavizan, Tehran 16788, IRAN, also with: Electrical Eng. Dept., Iran Univ. of Science & Tech., Narmak, Tehran, IRAN.*
2. *Electrical Eng. Dept., Tehran Univ., North Kargar Ave., Tehran 14399, IRAN.*
3. *Electrical & Computer Eng. Dept., Univ. of Toronto, Toronto, Ontario, Canada.*

ABSTRACT A new current-controlled oscillator (CCO) is presented which is suitable for use in low-voltage and low-power designs. These features, and the low supply dependence of this CCO all stem from using a regenerative mechanism in its primitive delay cells. The circuit is designed and simulated in a 0.8 μ m BiCMOS technology.

I. INTRODUCTION

Controllable oscillators of use in digital PLLs, are commonly designed using a ring oscillator structure. One of the most important causes of jitter in controllable ring oscillators is power-supply noise introduced on their frequency control-signal, or directly affecting the delay behavior of their primitive cells.

There are several techniques which reduce jitter in controllable ring oscillators:

- Using current signals and direct digital control as the frequency-control signal, have led to CCOs (Current-Controlled Oscillators)[1-3] and DCOs (Digitally Controlled Oscillators)[4], respectively.
- Using fully-differential circuits to implement the oscillator[5-8], can suppress many common-mode sources of

noise, such as thermal effects and power-supply variations.

- Applying negative feedback around the oscillator can utilize the noise-reduction property of feedback[5].

A survey of the architecture of delay cells shows a forward operation that the cell output voltage is normally produced directly from its input. This paper describes a novel CCO whose primitive delay cells use internal positive feedback. This new design will be shown to reduce considerably the power-supply sensitivity, and consequently the jitter of the proposed CCO. Using positive feedback also leads to some other features such as: suitability for low-voltage and low-power applications, as discussed in section III of this paper.

II. CIRCUIT DESCRIPTION

Circuit schematic of the proposed CCO, which uses three RS-latches as primitive delay cells, is shown in Fig.1. In order to control RS-latch behavior, and consequently the frequency of the CCO, RS-latches are designed by using pseudo-NMOS NOR gates.

The PMOS transistor in each NOR gate operates as the control current-source,

in addition to having the usual active-load role.

As the name 'CCO' for the proposed controlled oscillator indicates, the first jitter-reduction approach in its design is to control its frequency using a current signal. As was pointed out above, changing the state of each delay cell is performed by means of a regenerative mechanism. This will imply two important properties: First, power-supply sensitivity of the oscillator frequency will be lowered, and second, adequate noise margins between LOW and HIGH signal levels (V_{OL} & V_{IH}) are ensured. The last feature is guaranteed by the fact that the delay cells are bistable circuits and HIGH and LOW logical levels are stable states at the full limits of the power-supply voltage. This property will increase the robustness of the output voltage levels when the control current is reduced, or the power-supply voltage is lowered to values less than two threshold voltages of MOS devices. For these reasons this CCO is very appropriate for low-power and low-voltage applications. In addition, another important reason for the favorable operation of the proposed CCO at low voltages is that only two transistors are stacked between V_{DD} and ground in this configuration. This is in sharp contrast to most of the existing published designs, and is a great advantage of this circuit.

III. SIMULATION RESULTS

The operation of the new CCO was evaluated by PSpice simulation using level_3 parameters in a typical 0.8 μm BiCMOS process. Input-output characteristic of the new CCO are shown in Fig.2.

Perhaps the best way of observing the effect of positive feedback on the operation of the proposed CCO, is to consider

eliminating it from the circuit. The resulting circuit, which is the same as that reported in [8], is shown in Fig.3. In order to facilitate for comparison between these two circuits (with and without positive feedback), they are simulated using similar transistors, model parameters, and dimensions.

To compare power-supply sensitivity of the above-mentioned circuits, their input-output characteristics were obtained both with $V_{DD}=5\text{V}$ and with $V_{DD}=4.5\text{V}$. The percentage of CCO frequency change due to the 10% V_{DD} variation (5V to 4.5V) is indicated in Fig.4, which shows a much better supply-independency for the proposed CCO.

Controllability of the proposed CCO by smaller control currents, in comparison to the CCO of Fig.3, is shown in Fig.5. It should be noted that HIGH and LOW in Fig.5 refers to ON and OFF half-cycle voltage levels, respectively.

On the other hand, the proposed CCO can operate with low-enough supply voltages. Its minimum supply requirement is 1.6V while another 2-transistor CCO [8] and one common 4-transistor one [1] require a minimum supply voltage of 2.1V and 3.6V, respectively.

IV. CONCLUSION

A new current-controlled oscillator (CCO) has been presented which is suitable for use in low-voltage and low-power designs. These features, also low supply dependence of this CCO all come from using a regenerative mechanism in its primitive delay cells. Comparison with other published works demonstrate the higher performance of our proposed circuit in terms of low voltage and low power operation.

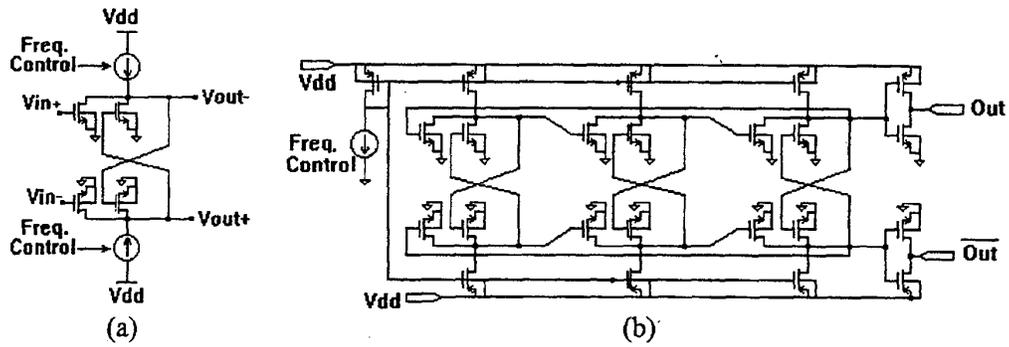


Fig.1 Proposed CCO, (a) Primitive delay cell, (b) Overall schematic diagram

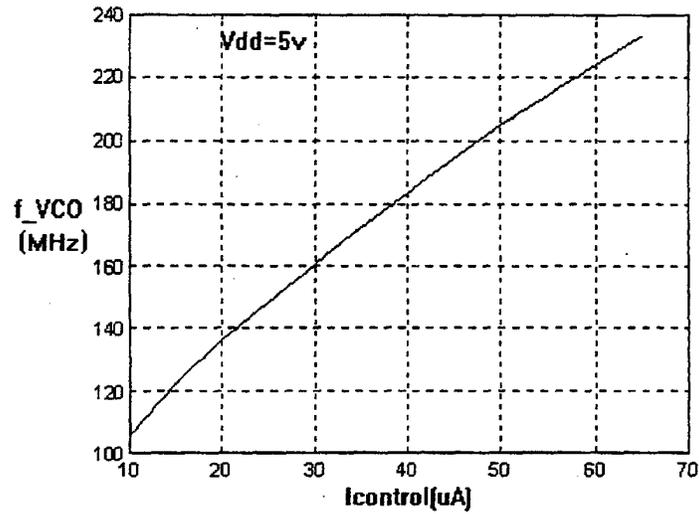


Fig.2 Input-output characteristics of the new CCO

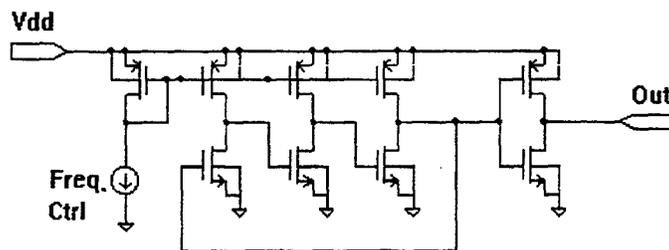


Fig.3 CCO reported in [8]

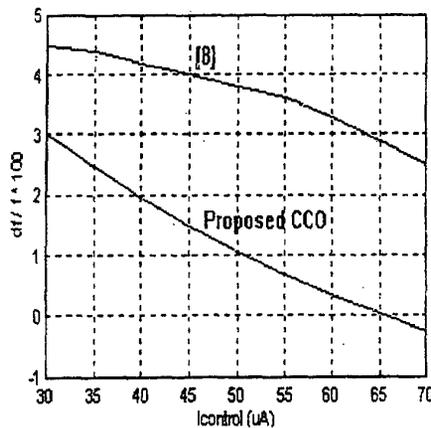


Fig. 4 Percentage of CCO frequency change due to a 10% V_{dd} variation

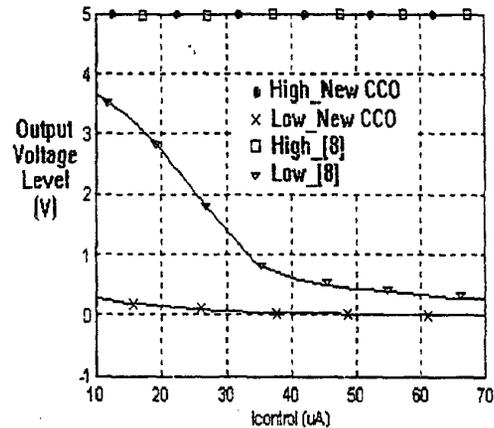


Fig. 5 High & Low output voltage levels as a function of control current

V. REFERENCES

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