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NOVEL APPLICATIONS OF A VARIABLE-THRESHOLD TRANSISTOR

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Introduction

A variable-threshold transistor (VTT) with inherent memory, now available off-the-shelf, can be utilized in a variety of digital and analog circuits using this information storage capability. Current industrial development is directed towards digital applications such as non-volatile, read-mostly semidonductor memories and programmable logic circuits. [1-3]. Applications introduced here are analog in nature, taking full advantage of the basic analog properties of the device. Such applications include a practical implementation of adaptive threshold logic compatable with integrated circuit technology, electronically programmable analog patchboards for use in hybrid computers and economic, long-term analog memories.

Structure of V.T.T.

The basic structure of the V.T.T. is that of an MIS transister with the gate formed by a sandwich of Silicon Dioxide (SiO_2) and Silicon Nitride (Si_3N_4) as shown in Fig.1.

This MNOS transistor structure normally operates as a conventional P-channel enhancement-mode MOSFET with the added advantage of a stabilized threshold voltage due to elimination of contaminating ions from the SiO_2 by the nitride layer. [4] However if a critical gate-to-source (substrate shorted to source) voltage is exceeded, a charge transfer to the SiO_2 - Si_3N_4 interface occurs. This charge is subsequently trapped upon the removal of the bias voltage, thus producing a shift in the threshold voltageof the device.

The charge transfer and accumulation can be explained by the difference in conductivities of the two insulating layers. The non-volatile memory characteristics can be attributed to the nonlinear nature of the conductivities of the insulators. [5] For the structure shown in Fig.1, the SiO_2 layer is more conductive than the Si_3N_4 layer. The nature of this conduction process in SiO_2 is not as yet determined but may be attributed to a tunnelling-injection mechanism.

V.T.T. Characteristics

The P-channel device discussed here exhibits a positive shift in threshold voltage for a positive gate-to-source bias and a negative shift for a negative bias. A typical threshold voltage hysteresis loop of the device used in the applications to be described is shown in Fig.2. The transfer characteristic shown in Fig.3 illustrates the range of threshold voltage attainable.

The critical gate-to-source voltage (Vc) is determined by device design and fabrication technique. Vc's in the order of 25-50 volts can be obtained, eliminating the high voltage circuitry required for the device used here. Once the threshold voltage is established, normal FET operation is resumed as long as the gate-to-source voltage is kept below Vc.

A voltage-time relationship exists between the bias voltage and the threshold characteristic. Figures 4.1 and 4.2 indicate a high voltage requirement for high speed shifting of the threshold. This is consistent with the theory of operation proposed earlier. The upper voltage and speed boundary is determined by the breakdown voltage of the gate. Long term relaxation effects will determine the volatility of the threshold voltage. Volatility can be traded off with speed and operating voltage, allowing memory times ranging from minutes to years.

Applications

We note in Fig.3 that the P-channel device can be made to operate either in the enhancement or depletion mode. It is this characteristic which lends the device to NDRM memories which are non-volatile. This characteristic, along with device symmetry, can be exploited in floating analog switches which can be electronically opened or closed but do not require permanent bias supplies.

The prime application presented here is the use of V.T.T.'s to implement a variable-weight, variable-threshold, threshold logic element. Such an element is extremely versatile from a logic viewpoint in that one circuit can be used to implement many different and complex logic functions.

The block diagram of such an adaptive threshold logic scheme is shown in Fig. 5. The circuit functions required in the logic element are implementable with V.T.T.'s,and thus ensure ease of integration by minimizing the constraints on circuit design and fabrication. That is, circuit tolerances can be cancelled and logical functions can be changed externally by momentary application of the proper voltage to suitable terminals.

The circuit built and tested using discrete devices is capable of 25 distinct thresholds. A typical number of inputs would be 10 to 15 with weights running from 1 to 26.

A third application is that of an economic, non-volatile analog memory. A proposed memory cell and setting circuitry is shown in Fig. 6. This application has not as yet been investigated thoroughly. In order to proceed in this direction one must have a firmer grasp of the technology of device fabrication than is currently available.

References

[1] C.J. Varker, B.V. Keshavan, and H.C. Lin, "MNOS Structure as Active, Passive and Storage Elements in Non-Volatile Memory Applications", IEEE Northeast Electronics Research and Engineering Meeting, Nov.1968

[2] F.W. Flad, C.J. Varker and H.C. Lin, "The Application of MNOS Transistors in a Preset Counter with Non-volatile Memory",

I International Solid-State Circuits Conference, Feb., 1969.

[3] H.G. Dill, R.W. Bower, K.G. Aubuchon and T.N. Toombs., "Anomalous Behaviour in Stacked-Gate MOS Tetrodes", International Solid-State Circuits Conference, Feb., 1969.

[4] "Catch the Wandering Threshold Voltage", Motorola Monitor, Vol.6, No.2, pp.18-20, July, 1968.

[5] F.A. Sewell, Jr., H.A.R. Wegener and E.T. Lewis, "The Variable Threshold FET: Theory and Experiment", International Solid-State Circuits Conference, Feb.1969.

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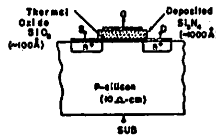

Figure 1: p-channel VTT structure

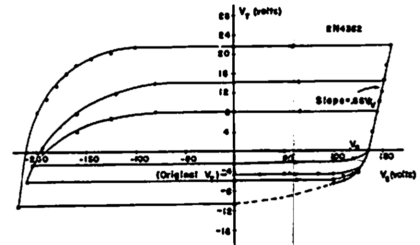

Figure 2: Threshold voltage characteristic of p-channel VTT

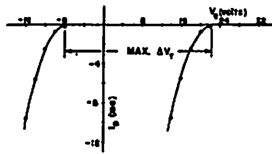

Figure 3: Transfer characteristic of 2N4352 (illustrating the range of threshold voltages)

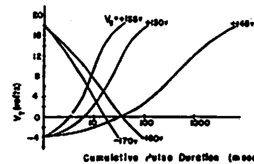

Figure 4.1: Threshold voltage versus bias voltage cumulative pulse duration

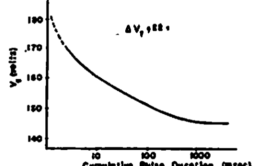

Figure 4.2: Bias voltage versus cumulative pulse duration.

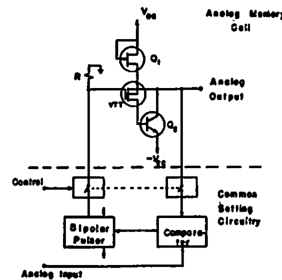

Figure 6: Block diagram of VTT analog memory

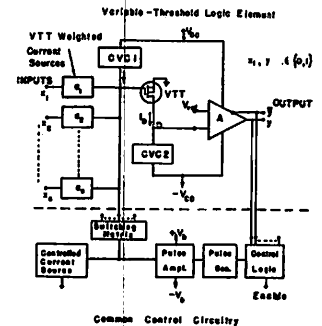

Figure 5: Block diagram of variable-threshold logic scheme