resistance, whereas that of the grounded-base stage is high. A shunt-feedback stage can, of course, be designed to have unity current gain; one merely chooses $R_L = R_F$ when

$$A_I \equiv -\frac{R_T}{R_L} \rightarrow 1.$$

Similarly, if one chooses R_L for a grounded-base stage equal to R_F, the stage transfer resistance becomes

$$R_T \equiv -A_I \times R_L \rightarrow +R_F.$$

However, these two special cases do not constitute equivalence of the circuits.

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A Second-Generation Current Conveyor and Its Applications

A recent publication [1] introduced the concept of current conveying and an implementation in the form of a circuit building block termed the current conveyor (CC). This block has proven to be useful in many instrumentation applications, some of which have already been tested and reported [2], [3], while others are still under investigation. This correspondence introduces another new building block embodying the current conveying concept, but with different and more versatile terminal characteristics. This new block is considered to be a second-generation current conveyor,[1] and hence is termed CC II.[2] Application of CC II to the areas of active network synthesis and analog computation will be considered.

Terminal Characteristics

The current conveyor is a grounded three-port network represented by the black box at the top right of Table I with the three ports denoted by x, y, and z. Its terminal characteristics can be represented best by a hybrid matrix giving the outputs of the three ports in terms of their corresponding inputs. For CC I this relationship can be stated as

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1}$$

while for CC II

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}. \tag{2}$$

It should be noted that all currents and voltages in (1) and (2) are total instantaneous quantities rather than incremental values. This property requires that any implementation of the current conveyor should be direct-coupled, should have no offset, and should exhibit linear ideal operation over a wide signal range. Circuit implementations for CC I have been previously reported [1], [3], while various implementations of CC II are under investigation. Details of circuit design are considered beyond the scope of this correspondence. Note that in the applications, the symbolic representation of the current conveyor will include a $\oplus$ or $\ominus$ sign to correspond with the sign of h_{32} in (1) and (2).

TABLE I
APPLICATION OF CURRENT CONVEYORS TO ACTIVE NETWORK SYNTHESIS

	2-PORT REALIZED	CHARACTERIZATION	REALIZATION USING CURRENT CONVEYOR
1	VOLTAGE-CONTROLLED VOLTAGE-SOURCE	$G = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	CCII
2	VOLTAGE-CONTROLLED CURRENT SOURCE	$Y = \begin{bmatrix} 0 & 0 \\ g & 0 \end{bmatrix}$	CCII
3	CURRENT CONTROLLED CURRENT SOURCE	$H = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	CCII
4	CURRENT CONTROLLED VOLTAGE-SOURCE	$Z = \begin{bmatrix} 0 & 0 \\ R & 0 \end{bmatrix}$	CCII, CCII, R
5	INIC	$G = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$	CCI, CCII
6	NIV	$Y = \begin{bmatrix} 0 & -g_1 \\ -g_2 & 0 \end{bmatrix}$	CCII, CCII
7	GYRATOR	$Y = \begin{bmatrix} 0 & -g \\ g & 0 \end{bmatrix}$	CCII, CCII

Application to Active Network Synthesis

Table I shows the use of the current conveyor to realize a few of the generating elements commonly used in active network synthesis. All designs are obtained by a direct implementation of the network-defining equations as given in column 2 of Table I. Although the table is self explanatory, we note the following.

1) Two different realizations are given for the NIC. In both realizations port 1 is short-circuit stable (SCS), while port 2 is open-circuit stable (OCS). Although in the realization using CC I, terminal z is assumed to be grounded, this is not a necessary condition. Since z carries an equal current as that through x and y, it can be used to monitor the current flowing in the negative impedance without causing any disturbance to the NIC. This unique three-port NIC has some interesting applications [4].

2) In the gyrator realization, the gyration conductance g is explicity available through two grounded resistances. This makes possible the realization of time-variable gyrators [5] by simple electronic variation of both of the conductances g. The same general remark applies for the NIV.

The Current Conveyor as an Analog Computer Element

If current is made to correspond to the computation variable in an analog computer, it is possible to use the current conveyor as the fundamental unit of such a computer. Table II illustrates the use of CC II to obtain the basic analog computation func-

Manuscript received August 5, 1968; revised October 28, 1968 and April 7, 1969. This work was supported in part by the National Research Council of Canada under Grant A-3148.

[1] Patent applied for.
[2] We will refer to the current conveyor previously reported as CC I.

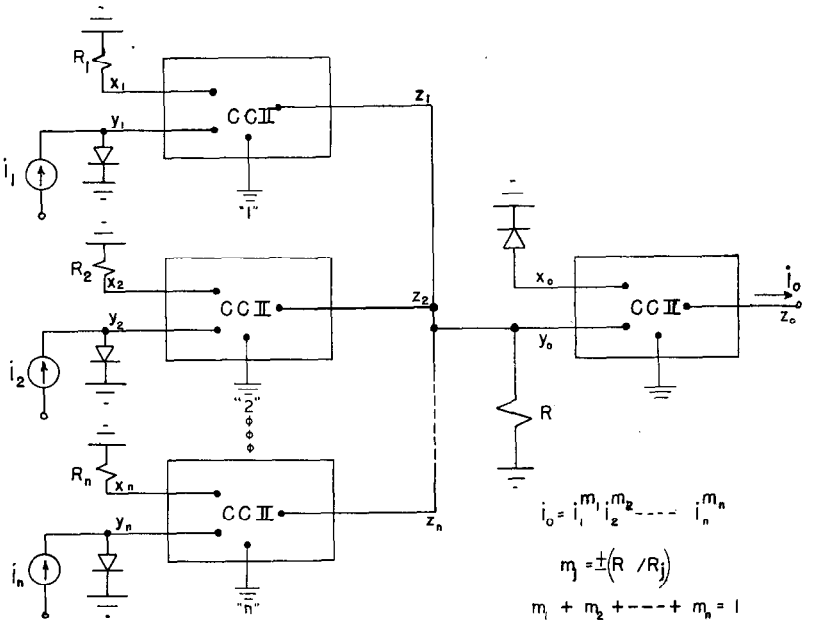

Fig. 1. A generalized function generator.

TABLE II
APPLICATION OF CURRENT CONVEYORS TO ANALOG COMPUTATION

	FUNCTIONAL ELEMENT	FUNCTION	REALIZATION USING CURRENT CONVEYOR
1	CURRENT — AMPLIFIER	$I_o = (R_1/R_2) I_1$	
2	CURRENT — DIFFERENTIATOR	$I_o = CR \frac{dI_1}{dt}$	
3	CURRENT — INTEGRATOR	$I_o = \frac{1}{CR} \int I_1 dt$	
4	CURRENT — SUMMER	$I_o = -\sum_1^n I_j$	
5	WEIGHTED CURRENT SUMMER	$I_o = -\sum_1^n I_j \frac{R_j}{R}$	

tions. Note that all passive elements have a grounded terminal. It is relatively easy then to provide direct digital control of the gain and time constants by switching some resistors in a binary-weighted fashion. Also the fact that the integrator capacitor has a grounded terminal simplifies the application of initial conditions.

Another powerful analog computation block is shown in Fig. 1. Fundamentally it is a generalized function generator with inputs $I_1, I_2, \cdots, I_n$, and output I_0. Using the terminal characteristics of CC II given in (2) and assuming ideal matched logarithmic characteristics for all diodes, it can be shown that

$$I_0 = \prod_{j=1}^{n} (I_j)^{m_j} \tag{3}$$

where

$$\sum_{j=1}^{n} m_j = 1$$

$$m_j = \pm\left(\frac{R}{R_j}\right)$$

with the sign corresponding to that of the jth conveyor.

Many useful functions can be obtained from this generalized function generator by the choice of the number of conveyors and appropriate values for the powers m_j. As an example, an analog multiplier-divider requires that $n = 3$, $m_1 = +1$, $m_2 = +1$, and $m_3 = -1$ and provides the relation

$$I_0 = \frac{I_1 I_2}{I_3}$$

where I_2 and I_3 may be considered, alternatively, as variables or constants. Although one quadrant operation is implied by the diagram of Fig. 1, four quadrant operations can be provided by some additions.

CONCLUSIONS

The second-generation current conveyor introduced is a convenient building block that provides a simplified approach to the design of linear analog systems. Although its circuit implementation is not considered in this correspondence, it seems that the versatility of the device warrants its production in integrated form.

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On the Selection of Isolated Regions in Computer-Aided Design of Integrated Circuits

I. Introduction

Bipolar integrated circuits cannot be fabricated if electrical isolation is not provided between some groups of components [1]. The determination of these groups is one of the initial tasks in integrated-circuit design. Since the increasing complexity of circuits that can be integrated makes the use of computers more and more necessary to the designer [2], [3], the problem of selecting isolated regions (IR's) by computer has been investigated.

In a preceding paper [4], an algorithm has been presented that determines the so-called "maximal IR-compatibility" classes of components, from which all allowable partitions of the circuit can be derived. This is the first step toward the solution. To minimize the circuit area, a maximum partition, i.e., a partition with the minimum number of IR's, should be selected. However, there are generally several maximum partitions. The problem of selecting one of them is discussed in this correspondence. In Section II the theoretical background of the algorithm for maximal classes is summarized. A design criterion for defining the optimum partition and the problems encountered in its implementation are illustrated in Section III. Section IV finally describes an algorithm based on the results of the investigation performed in Section III.

II. Background

In this section we shall recall the definition of a maximal IR-compatibility class and show that generally these classes are not disjoint, i.e., many maximum partitions do exist. The algorithm for determining maximal classes will not be described here; the interested reader can find it and a more detailed description of its theoretical basis in a preceding paper [4].

A list of preliminary definitions will now be given.

Definition 1

A partition $P = \{B_1; B_2; \cdots; B_n\}$ of a set S is a collection of n disjoint and exhaustive subsets of S. Subsets $B_1, B_2, \cdots, B_n$ are said to be the *blocks* of P.

Definition 2

A partition P of a circuit S (considered as the set of its components) is said to be *realizable* (with respect to the problem of IR's) if the components of each block of P can be fabricated together without isolation. *A maximum partition* is a realizable partition with the minimum number of blocks.

Definition 3

Two or more components of a circuit S are said to be compatible with respect to an IR (*IR-compatible*) if they can be included in a block (of a realizable partition of S) corresponding to that IR.

Definition 4

A subset s of a circuit S is an *IR-compatibility class* if there exists a realizable partition of S having s among its blocks.

Definition 5

A *maximal IR-compatibility class* is a class that is not included in any other IR-compatibility class.

In the set of the blocks of all realizable partitions of a circuit, the maximum blocks correspond to the maximal IR-compatibility classes (Definition 4). We can therefore state the following theorem.

Theorem 1

A partition of a circuit is realizable if and only if its blocks are included in the maximal IR-compatibility classes of the circuit.

By Theorem 1, any realizable partition can be derived very easily from maximal classes. According to the main design objective, that is the minimization of circuit size, a maximum partition should be selected,[1] since the area required by such a partition to separate the IR's from one another is minimum [5]

To show that many maximum partitions may exist, let us limit, for the sake of simplicity, our discussion to integrated circuits with a reverse-biased p–n junction isolation and a p-type substrate.[2] We shall state the requirements for IR compatibility in terms of conditions to be satisfied by component terminals. The terminal of an n-type region that constitutes an IR corresponds to a node in the circuit schematic only if the region is used also as a part of one or more components (e.g., as the collector of an n-p-n transistor).

Definition 6

The terminal of an IR is said to be its *fundamental terminal.*[3]

Definition 7

For each component the terminal indicated in Table I is called the *primary terminal.*

There are two types of components in Table I: the topological-constraint components (*TC-components*) and the electrical-constraint components (*EC-components*); EC-components are indicated in Table I by a star. The differences between these two types are explained in the statement of the following theorem.

Theorem 2

A component can be included in an IR-compatibility class if and only if its primary terminal:

a) is connected to the fundamental terminal of the class (condition for a TC-component); or
b) has a voltage not greater than the voltage of the fundamental terminal (condition for an EC-component).

As shown by this theorem, the constraint for EC-components is such that they may often be included in more than one maximal IR-compatibility class. Because of the existence of *multiclass components*, i.e., of EC-components belonging to several maximal classes, these classes are generally not disjoint.

Manuscript received August 3, 1968; revised November 11, 1968. This work was supported in part by the Comitato di Ingegneria, Consiglio Nazionale delle Ricerche, Rome, Italy.

[1] Note that sometimes there are some constraints to be taken into account, for example, the area of the IR's containing transistors whose performance is highly sensitive to capacitive loading should be minimized. These cases can be easily dealt with by the algorithm described in the paper cited above [4].
[2] Extending what will be said to other isolation techniques or to the case of n-type substrate is straightforward.
[3] Note that each IR-compatibility class is an IR in some realizable partitions, hence its fundamental terminal is always perfectly defined.