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# Through the Looking Glass

*Trend tracking for ISSCC 2012*

**A**t the IEEE International Solid-State Circuits Conference (ISSCC), there is a long tradition of working to maintain the conference's role as the foremost global forum for the presentation of advances in solid-state circuits and systems on a chip (SOCs). But this implies a great deal of effort on the part of many people. One of the most important elements of this effort is the structuring and organization of the Program Committee, including its subdivision into ten subcommittees focusing on diverse technical areas and its dynamic growth and adaptation through the selection of world-renowned specialists. One of the many techniques used by the subcommittees to remain at the forefront of evolving technology is the identification and maintenance of trend information, on the basis of which new developments become startlingly clear.

The intent of the present article is to share with IEEE Solid-State Circuits Society (SSCS) membership a sampling of the views held by the diverse group of experts represented by the Program Committee, which for ISSCC 2012 is composed of 159 members. These members are divided into ten subcommittees whose size ranges from 12 to 18 people. This year, the subcommittees are focusing on the following areas: analog; data converters; energy-efficient digital; high-performance digital; imagers, microelectromechanical systems (MEMS), medical, and displays; memory; radio frequency; technology directions; wireless; and wireline.

What follows is a sampling of recent analyses and predictions from each of the ten subcommittees.

## **Analog**

Analog circuits continue to play a key role in modern technology. For example, analog signal amplification is fundamental to interfacing with antennas, microphones, speakers, headphones, and image sensors. Analog circuits are bridges between the digital world and the analog real world. Just as with the bridges on our roads, analog circuits often become bottlenecks, and their design is critical to overall performance, efficiency, and robustness. Nevertheless, digital circuits such as microprocessors drive the market, and therefore semiconductor technology has been relentlessly optimized over the past 40 years to reduce the size, cost, and power consumption of digital circuits. Analog circuitry, however, has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased,

*Digital Object Identifier 10.1109/MSSC.2011.2177577*  
*Date of publication: 14 February 2012*

the range of analog voltage they can handle has also decreased, and the variation observed in their analog performance has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits: One is to forgo the latest digital IC manufacturing technologies, and instead fabricate analog circuits in older technologies, which can be augmented to accommodate the high voltages demanded by medical, automotive, lighting, and industrial applications. Other applications dictate a second trend: accepting full integration of analog and digital circuits in the most modern digital semiconductor technology. In such applications, advances in analog interfaces are needed to realize the full potential of digital processing.

#### THE 2012 ISSCC PROGRAM COMMITTEE

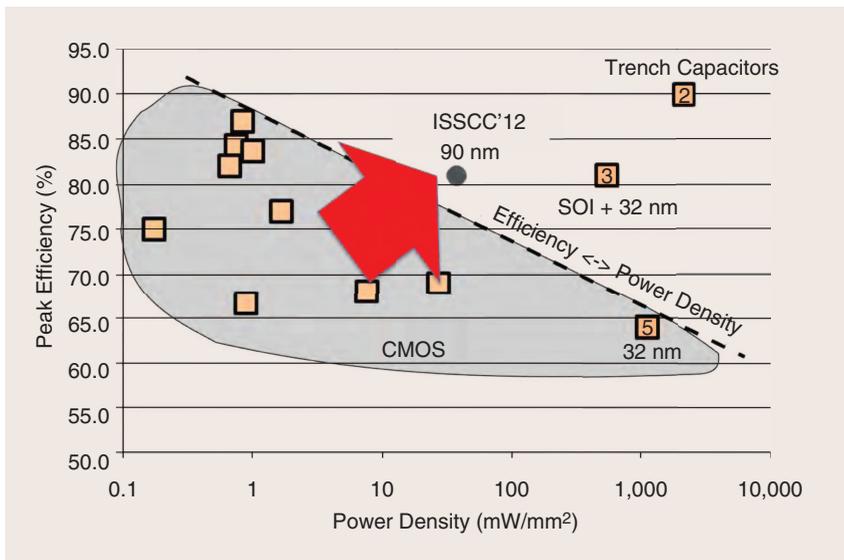
FRONT ROW, FROM LEFT: DAVID SU, TZI-DAR CHIEUH, BRAM NAUTA, LAURA FUJINO, HIDEYO HIDAKA, HOI-JUN YOO, AND KEVIN ZHANG. BACK ROW, FROM LEFT: ROLAND THEWES, BILL REDMAN-WHITE, AARNO PARSSINEN, ANANTHA CHANDRASKAN, VENU GOPINATHAN, ANDREA CATHELIN, STEFAN RUSU, DAVID FRIEDMAN, MAKOTO IKEDA. NOT PICTURED IS SUBCOMMITTEE CHAIR SIVA NARENDRA.

For example, mobile systems with multicore digital processors routinely have their battery life limited by the power consumption of traditional analog audio-playback circuits. Modern analog circuits have embedded within them digital signal-processing elements that help overcome analog-circuit limitations; moreover, low-power analog circuits are being embedded within digital ICs to monitor their performance and manage their power consumption. Hence, the distinction between analog and digital circuit design is blurring, spawning new advances in the state of the art for both.

The efficient control, storage, and distribution of energy are worldwide challenges and an increasing focus of research in analog circuits. Whereas the manipulation and storage of information is efficiently performed digitally, the manipulation and storage of energy must fundamentally be performed using analog systems. As a result, the key technologies for power management are predominantly analog. Consequently, there is a great deal

of activity in architectures for dc-dc converters for many applications, such as lighting, multiple-output-voltage generation, and inductorless fully integrated power conversion. There is also an increase in the use of circuits that harvest energy from many sources, such as ambient light, heat, and motion, and then store it and convert it into usable voltages and currents. Currently, much effort is being directed to simultaneously increasing the energy efficiency and power density (power-handling ability per unit of size) of power management circuits, as shown in Figure 1. Future power management systems will begin to make use of sources with voltages well below 100 mV. At the same time, the power consumption of analog circuits is being aggressively scaled down in order to enable these low-power systems. Micropower instrumentation amplifiers and oscillators and highly efficient audio power amplifiers are two examples of this trend. Together, these technologies will permit devices to be powered indefinitely from sustainable sources,





**FIGURE 1:** Trends in integrated power conversion. Each year, more and more is integrated in standard CMOS technologies, optimizing efficiency versus power density. At ISSCC 2012, these trends are evident in a shift to higher performance, as shown by the arrow.

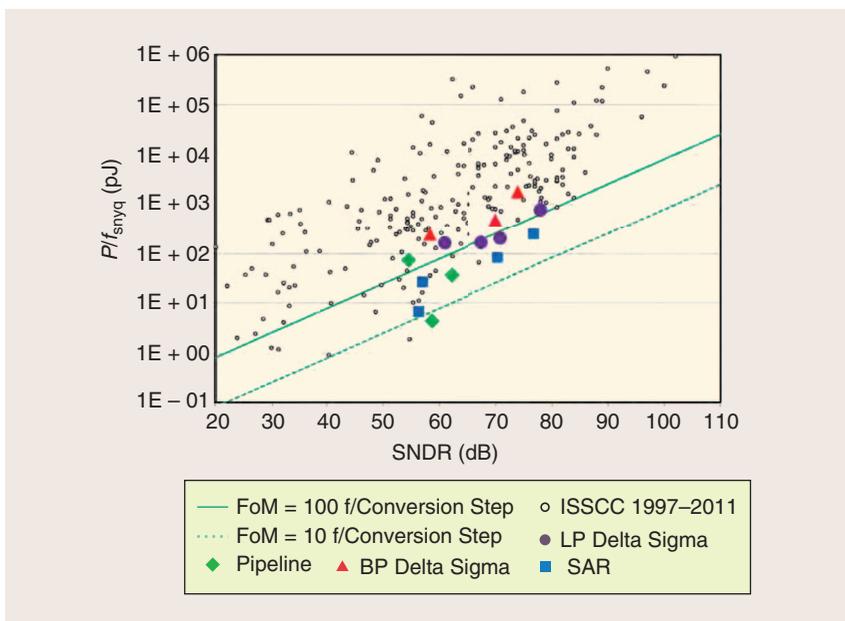
opening the door to ubiquitous sensing, environmental monitoring, and diverse medical applications.

### Data Converters

The march of progress in converter designs involves exploiting the inherent trade-offs between signal-to-noise ratio (SNR), bandwidth, sampling frequency, and power efficiency, especially when all need to be improved. This year, at ISSCC 2012,

new and improved design combinations are being presented.

Figure 2 shows power efficiency in terms of power dissipation per Hertz at the Nyquist frequency versus signal-to-noise-and-distortion ratio (SNDR). Since higher SNDR requires more power, constant figure-of-merit (FoM) trend lines in the plot are proportional to SNDR. The small dots in the graph are previously published ISSCC results,



**FIGURE 2:** Power efficiency versus SNR, highlighting ISSCC 2012 results.

while the ISSCC 2012 contributions are indicated by the large triangles, squares, and circles. As the plot indicates, ISSCC 2012 data converters have once again extended the state-of-the-art.

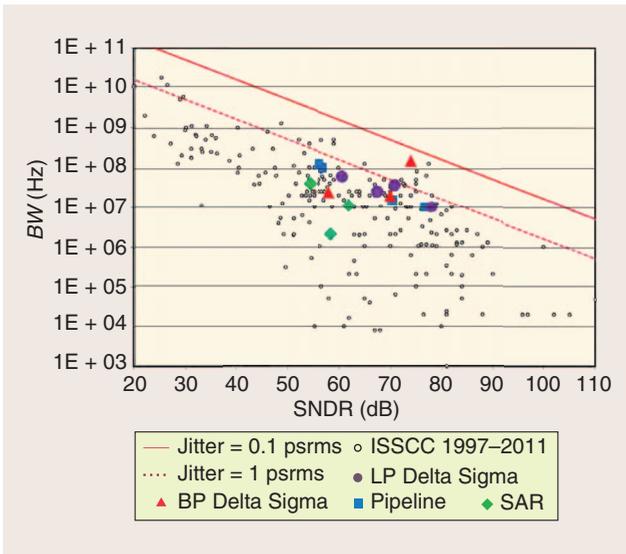
Figure 3 shows bandwidth versus SNDR. Generally speaking, bandwidth is lower at higher SNDR, as is indicated in the figure. The trend lines correspond to two values of clock jitter, 0.1 and 1 ps root mean square (psrms). In this figure, it can be seen that bandpass delta-sigma converters are especially pushing the state of the art.

Figure 4 shows the FoM versus Nyquist-bandwidth. At low frequencies, the FoM is optimal (low FoM is better), but as the graph shows, the FoM is deteriorating at higher frequencies. This is primarily caused by the speed limitation of presently available technology. As can be noted, designs presented at ISSCC 2012 show good progress, with a successive-approximation register (SAR) pushing the state of the art at lower frequencies and a pipeline design breaking the barrier at higher frequencies.

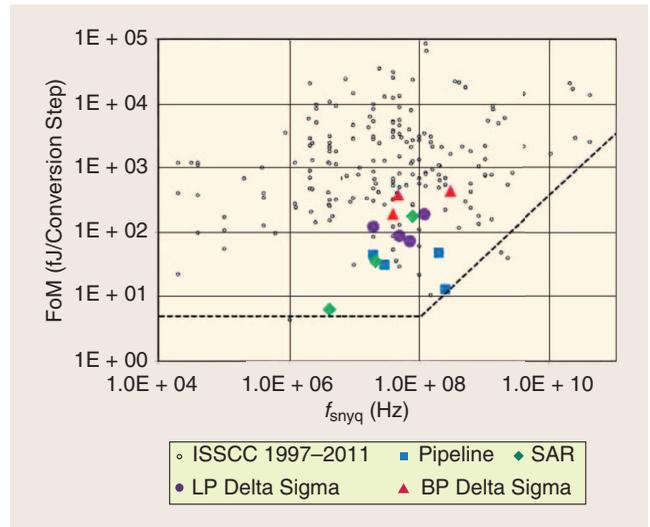
### Energy-Efficient Digital

The energy efficiency of digital circuits becomes increasingly important as larger and larger numbers of transistors are integrated on a single chip. This is particularly important for mobile applications in multimedia and communications.

Multimedia and communication technologies have enhanced the lives of mobile consumers by increasing productivity, enhancing the social networking experience, and delivering improved visual and audio quality for communication links and entertainment. In this development, the performance of embedded CPUs has increased to meet the rising demands of general-purpose computations. At the same time, dedicated multimedia accelerators provide a solution for well-defined, energy-efficient signal processing constrained by the physical limitations of advanced



**FIGURE 3:** Bandwidth versus SNDR.

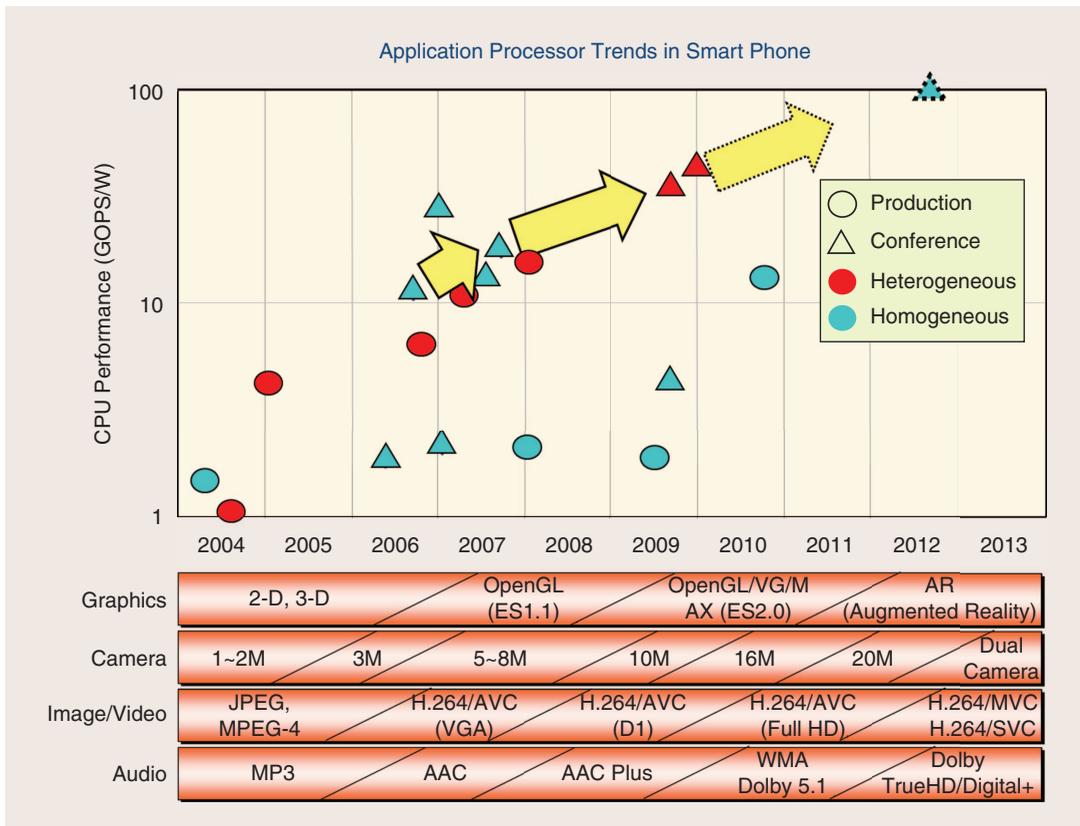


**FIGURE 4:** FoM (energy per conversion step) versus Nyquist-bandwidth for various converters.

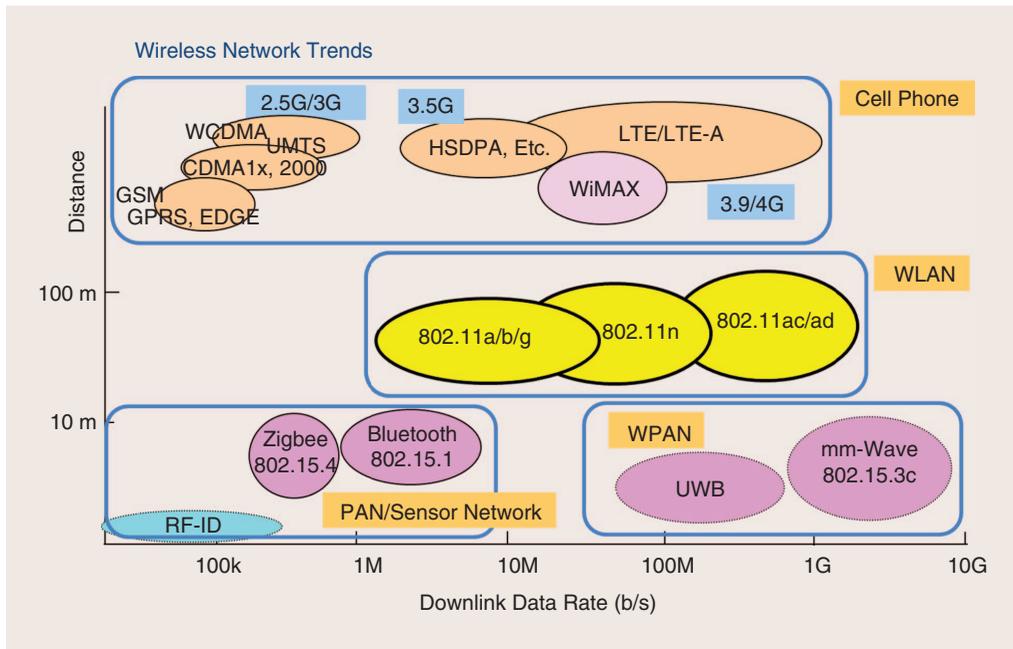
process technologies. But consumer expectations for increasing mobile functionality will continue unabated into the foreseeable future. This fact necessitates advances in low-voltage technologies coupled with progress in architectures and designs.

Figure 5 illustrates the energy efficiency of the main CPU in a smart phone application processor. As can be seen, CPU performance has continually increased in both heterogeneous and homogeneous SOCs. But because of the thermal and power

limitations of handsets, the energy efficiency of the CPU has also had to increase in order to sustain the thermal and power envelopes. There is still room for further increases in CPU frequency, number of cores, and memory capacity. Additional power



**FIGURE 5:** Trends in application processors for smart phones.



**FIGURE 6:** Trends in wireless networks.

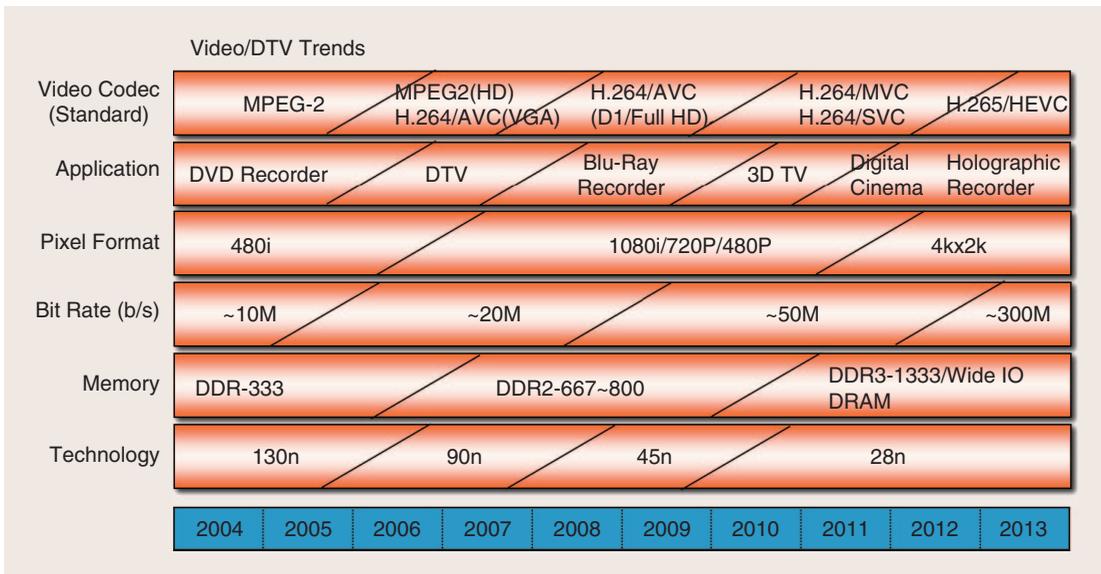
efficiency from technology, along with circuit and architectural improvements, must be incorporated, however, so as to offset the higher CPU clock frequencies, additional cores, and greater amounts of memory.

Historically, many multimedia applications were first implemented in general-purpose CPUs or other programmable processors. The multimedia computational requirements have increased faster than the ability

of programmable devices to reasonably address them, however. Originally this occurred with graphics, imaging, and video. Semiprogrammable and hard-wired cores are now required to remain within thermal limits and meet economic considerations. There will be a continued need for circuit, architectural, and system innovations to maintain this growth trend. New areas in which dedicated processors are particularly

needed include gesture-based user interfaces and computational imaging, to name only two.

Figure 6 presents current trends in the wireless-communication standards that are employed to achieve various link lengths and data rates. Wireless-networking standards can be roughly segmented into four categories: cell phones, with the greatest link distance; wireless LANs (WLANs), with just over 100 m in link distance;



**FIGURE 7:** Trends in digital TV and video.

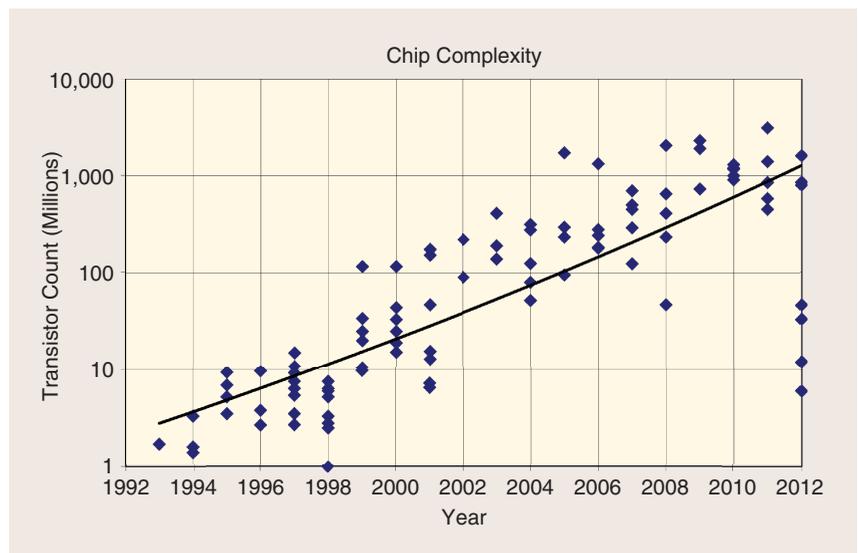
personal area networks (PANs), with up to 10 m of range at data rates of up to 10 Mb/s; and wideband PANs (WPANs), with up to 10 m of range at data rates of up to 10 Gb/s. In each of these categories, the data rate has increased over time, typically providing an increased computational load, so as to move closer and closer to the theoretical channel capacity of the system.

Figure 7 presents video and digital-television trends. Generally speaking, modern video requires a very large number of computations to keep up with increasing video bit rates, increasing resolution and frame rates, increasing complexity of the standards for video compression, and new applications such as 3-D and multiview video that demand higher resolution and greater numbers of concurrent streams. Dedicated high-performance and low-power video processor architectures and high-bandwidth external dynamic random-access memory (DRAM) interfaces are essential to meet these dramatically increasing performance requirements. Mobile video also requires energy efficiency in implementing video streaming, encoding, and decoding for high-definition video. Both low-power video engines and low-power memory architectures leveraging new technology such as wide-I/O, low-capacitance direct interfaces to DRAM are paramount.

As process technology continues to advance, enabling integration on a massive scale, this year at ISSCC 2012 we are seeing processors originate from a wide variety of technological backgrounds. New ground is being broken in the key areas of transistor integration, performance-per-unit power, and functional integration. This is being accomplished across varied process technologies (65-nm, 45-nm, 40-nm, and 32-nm) and for bulk and silicon on insulator (SOI) CMOS technologies.

### High-Performance Digital

Rapid progress in the reduction of CMOS feature size in commercial



**FIGURE 8:** Chip complexity.

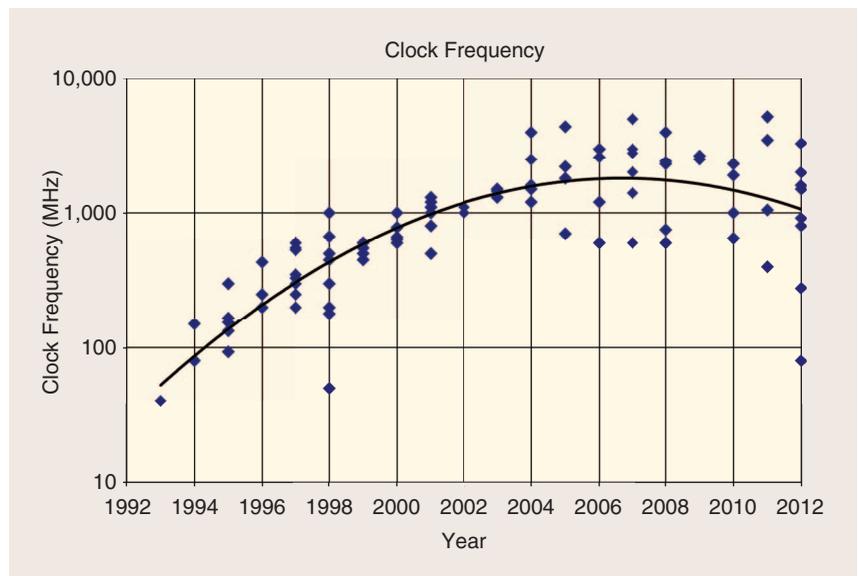
products continues to drive applications of high-performance digital technology.

At ISSCC 2012, the continuing progress in CMOS technology provides us with the first 22-nm commercial microprocessor featuring new vertical device architectures with triple gates. These developments enable further improvements in area and energy efficiency.

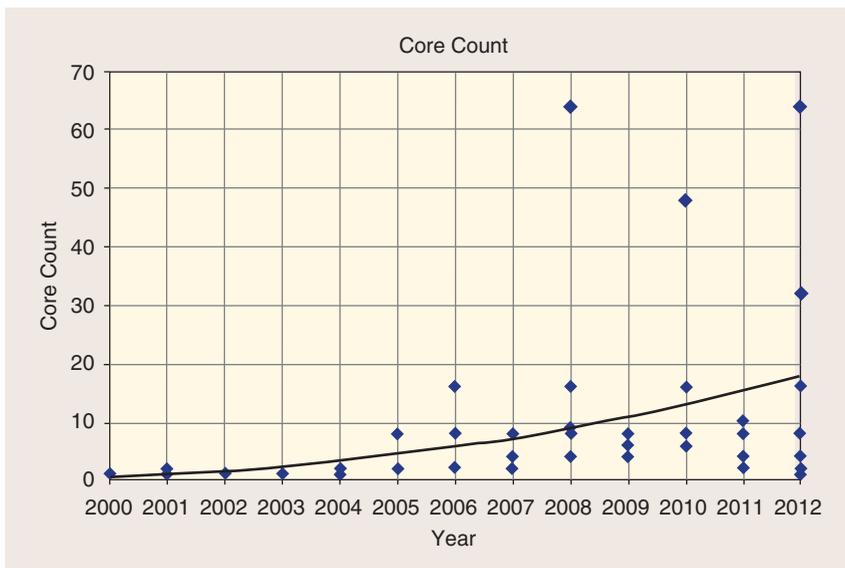
The chip complexity chart in Figure 8 shows the trend in transistor integration on a single chip over the past two decades. While the 1 bil-

lion-transistor integration level was first achieved five years ago, last year marked the first commercial product exceeding 3 billion transistors on a single die. This trend persists: Average complexity continues to increase, with 1.4 billion transistors on the first 22-nm commercial microprocessor chip.

As power reduction becomes mandatory in every application, the trend toward lower clock frequencies also continues, as shown in the frequency trends chart in Figure 9. This is driven by decreased supply voltages,



**FIGURE 9:** Clock frequency.



**FIGURE 10:** Core count.

with processors operating in the near-threshold or even the subthreshold voltage domain. The performance loss resulting from reduced voltages and clock frequencies is compensated for by further increased parallelism. Leveraging sophisticated strategies to lower leakage and manage voltage, variability, and aging has bolstered the continuing reduction in total power dissipation. This is helping to rein in the immense power demands from PCs, servers, and similar systems. Consequently, it yields solutions with less cost and reduced cooling requirements, resulting in greener products.

In addition to the trend toward integrating more cores on a single chip, shown in the core trend chart in Figure 10, additional dedicated coprocessing units for graphics and communications are now commonly integrated on these complex SOCs. It is worth noting that the design of such SOCs requires broad collaboration across multiple disciplines, including circuits, architecture, graphics, process technology, system design, energy efficiency, and software.

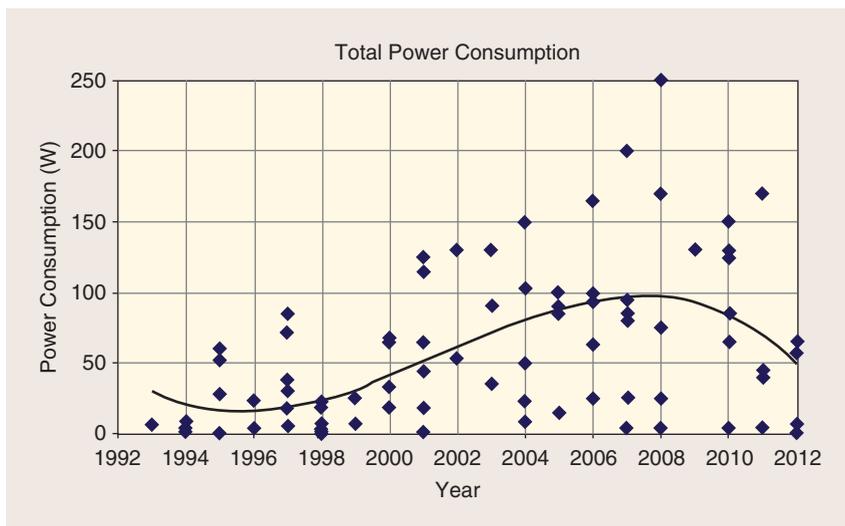
High-performance and power-efficient computing techniques continue to be introduced for targeted critical applications, such as floating-point

and single-instruction, multiple-data (SIMD) processors. As a result, we can see a downward trend in power consumption, as shown in the power trend chart in Figure 11.

ISSCC 2012 marks the wider introduction of massively parallel, 3-D-integrated systems. In such systems, a third dimension of integration becomes available by stacking monolithically integrated dies and interconnecting them by applying innovative TSV technologies. The result of this integration is a new level of performance in a power-efficient package.

Another trend evident this year is the continued emergence of all-digital phase-locked loops (PLLs) and delay-locked loops (DLLs) to better exploit deep-submicron-feature-size scaling, thereby reducing power and area costs. Due to the application of highly innovative architectural and circuit-design techniques, the features of these all-digital PLLs and DLLs have improved significantly over the past several years. The rms-jitter-versus-power diagram in Figure 12 shows the improvement of the widely accepted FoM for PLLs and multiplying delay-locked loops (MDLLs).

Clearly, the rapid downward reduction of feature size continues to force the replacement of traditionally analog techniques.



**FIGURE 11:** Total power consumption.

### Imagers, MEMS, Medical, and Displays (IMMD)

The common thread that unites the constituents of IMMD is a concern for interfaces with the physical world—both the human body and its environment. Conventionally, we consider this broad area in terms of both task and tool: imagers, MEMS, medical, and displays, as discussed in the following subsections.

#### Imagers

The CMOS image sensor business remains one of the fastest-growing segments of the semiconductor industry, due to the proliferation of cell phone cameras and other digital-imaging

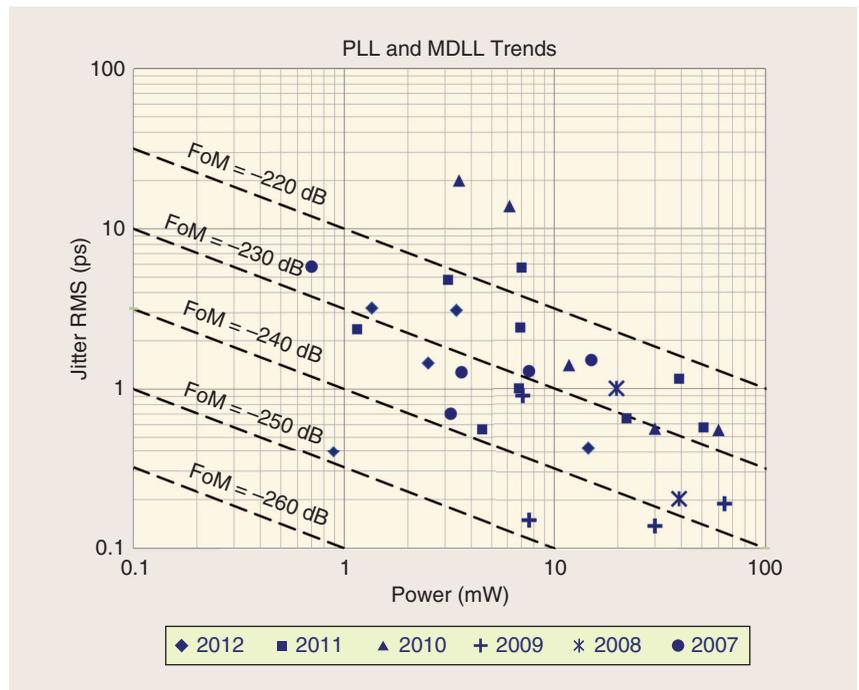
applications. The intense adoption of cell phone cameras led to approximately 90% market penetration in 2009. Currently, 3G mobile technology is accelerating the utilization of multiple cameras in each cell phone. Of course, other emerging digital-imaging markets include traditional digital still cameras (DSCs) and camcorders. But other potentially high-volume markets are emerging: Web cameras, security cameras, automotive cameras, digital-cinema cameras, and gaming cameras.

For all cameras, the resolution and miniaturization races are ongoing; while the performance requirements remain constant, pixel size continues to scale down. Pixel resolutions of more than 20 million are commercially available, employing enhanced small-size pixels. A column-parallel approach based on pipelined and multiple-sampling implementations is emerging for low-power, high-speed, low-noise analog-to-digital converters (ADCs) for high-resolution DSC and video applications.

In this race, innovative new technologies are under constant development. These include advanced sub-100-nm CMOS image-sensor fabrication processes, backside illumination, and wafer-level imaging. Backside illumination is now a mainstream technology for mobile imaging. Most producers rely on bulk silicon rather than the more expensive SOI approach for back-side thinning.

The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise and compensate for optical limitations. The level of sensor computation is increasing to thousands of operations per pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts, there is a trend throughout the image sensor industry toward higher levels of integration, in order to reduce system costs.

High dynamic range (HDR) is now well established in low-cost con-



**FIGURE 12:** Trends in PLL and MDLL technology.

sumer imaging. High-speed, low-power, low-noise, column-parallel ADCs are becoming a key technology for high-definition video imagers. But many barriers must be overcome in order to maintain market growth in the image sensor industry. These challenges include better image quality, higher sensitivity, higher sensor resolution, lower cost, higher data-transfer rate, higher system-level integration, lower power consumption, and “consumer-priced” integrated 3-D imaging. So-called sensor-plus-companion-chip solutions are replacing SOCs except for the most compact camera modules, where back-side imaging is combined with 3-D integration.

More developers are demonstrating subelectron readout noise performance for low-light imaging applications. For nonconsumer low-light-level applications, imager arrays based on 2-D single-photon-avalanche diodes (SPAD) with increased resolution and smaller pixel size are beginning to compete with electron-multiplying CCD (EMCCD) technology. These deep-submicron CMOS SPADs are now capable of meeting the requirements for high resolution and high timing

accuracy using highly parallel implementations of time-to-digital converters (TDCs) with small pixel pitch and better fill factor.

Trends in emerging digital camera markets include lower-bandwidth communication for surveillance cameras, wider dynamic range and optical-communication functions for automotive cameras, faster read-out for digital-cinema cameras, and 3-D imaging for gaming. These markets are placing ever increasing functionality and performance demands on today’s image sensors, which are in turn delivering an exponential rate of growth in both complexity and performance to ensure that they can keep pace.

One very hot R&D topic is 3-D imagers, given the current push toward 3-D entertainment, security, and automotive applications. Rapid increases in integrated logic functionality are driving a dramatic increase in imager functions and features. Such possibilities include merging 2-D with 3-D imaging by interlacing 3-D time-of-flight pixels with a standard RRGB pixel architecture as a path toward simultaneous color and depth imaging.

The market share for CCDs continues to shrink in machine vision, compact DSC, and security applications. Only within top-end broadcast and top-end digital cameras do CCDs still maintain a significant market share.

### Sensors and MEMS

CMOS temperature sensors continue to improve, reaching higher temperatures (200 °C), with finer resolution (100 $\mu$  °C/ $\sqrt{\text{Hz}}$ ), in shorter conversion times (10  $\mu$ s), with simpler calibration (using voltage rather than temperature), and using smaller die sizes (0.006 mm<sup>2</sup>).

New technologies for temperature sensors are maturing; in particular, thermal diffusivity is proving to be a valuable sensing phenomenon, reaching both high temperatures and good accuracy. Small-area, high-speed temperature sensors in highly scaled 22-nm CMOS technology will be important for microprocessors so as to limit die temperatures to safe values.

MEMS oscillators are improving. Phase noise is now low enough for demanding RF applications; 12-kHz–20-MHz jitter is now below 1 ps; and frequency accuracy is now better than 0.5 ppm. MEMS microphones, accelerometers, and pressure sensors continue to improve as they become common in consumer and automotive applications.

### Biomedical

There is an increasing interest in neural applications, with significant R&D activity in the field of biopotential sensors for neural recording and stimulation. Such activity includes the following trends:

- Closed-loop systems are being commercialized: a closed-loop, acceleration-sensor-enabled neurostimulation device is CE-marked in Europe, and a closed-loop epilepsy device has completed clinical trials. The latter is a major innovation that leverages the latest sensor and circuit technology for neural interfacing, allowing for

novel diagnostics based on chronic recording.

- Brain-machine interface systems are now transferring into pilot clinical trials, although there continues to be some debate about “best methods.” While acute human testing shows that only a low degree of freedom is needed to control robotic arms in paralyzed patients, methods are being extended for a broader range of neural applications.
- Continuing efforts are enabling high-spatial-resolution, multichannel neural stimulators (such as those for retinal stimulation) and stimulators with recorders (such as those used in brain research). For example, a retinal implant with 60 pixels has received a CE mark, a step forward in the design of a sophisticated prosthesis. Work to increase complexity by another order of magnitude is ongoing.

The demand for telemedicine, remote sensing, and economical design is expanding as the population ages and cost pressures increase. These pressures are growing significantly with health care reform; the economic value of technical solutions is now being considered along with safety and efficacy.

Silicon technology is enabling new paradigms for biological signal processing. Examples include:

- Along with 32-bit processing cores, 0.13- $\mu$ m foundry-based CMOS technology is stabilizing as a low-power process for biomedical purposes. The partitioning of signal processing between the analog and digital domains is still being debated, with both modalities reaching levels that allow for chronic monitoring with minimal energy drain.
- Silicon-based arrays are emerging for analyzing genomes and immunoassays. Multiple paradigms are being explored to eliminate the need for expensive optical components. It is being proposed not only to perform hybridization assays on-chip but to allow direct DNA sequencing as well.

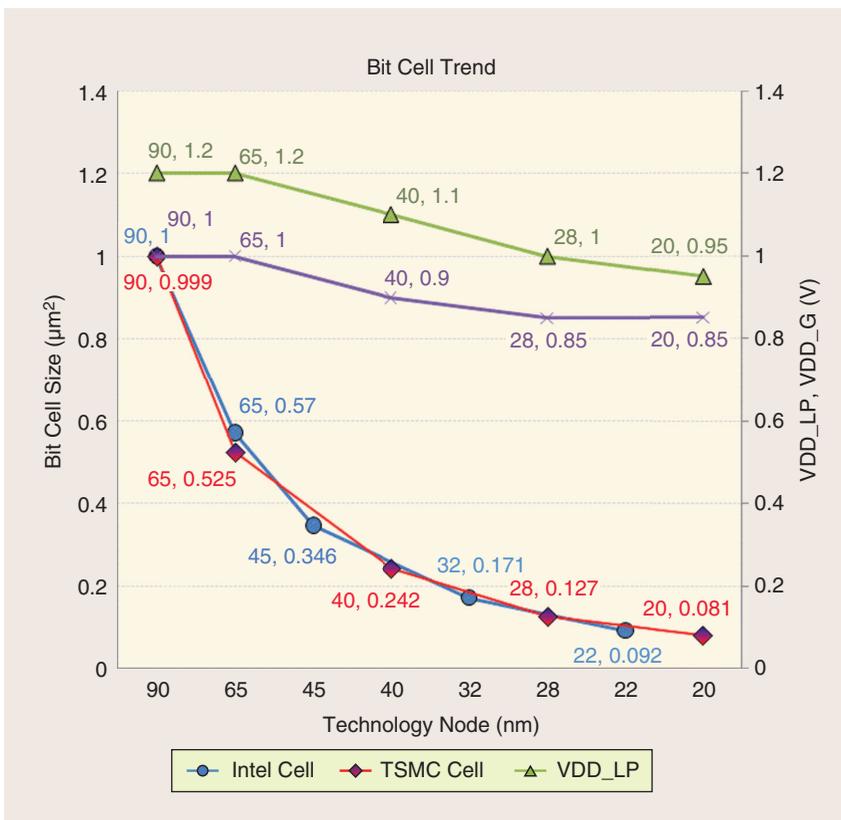


FIGURE 13: Trends for SRAM bit cells.

## Displays

Single-chip sensing and driving for touch-integrated liquid-crystal display (LCD) panels is one of the display-technology trends for much thinner and lower-cost realizations. Advanced 3-D LCD TV technologies are opening up a new era of 3-D home theater. The current focus is on how to make more realistic views that are comfortable to the eye. Technologies for 3-D realization that do not require glasses and their driving electronics are emerging for mobile and notebook applications.

## Memory

Development of mainstream memory technologies continues unabated. The major thrust concerns embedded memories, i.e., static random-access memory (SRAM), DRAM, and floating-gate-based flash, for very broad applications. As processes continue to shrink in an effort to follow Moore's law, however, each incumbent technology is encountering difficulty in maintaining the trend line. Cells in SRAM, DRAM, and flash are becoming ever more difficult to scale. In response to the challenges, we see logic processes adopting trigate/3-D devices, along with assist circuits for SRAM read and write. Meanwhile, certain emerging memory technologies are making rapid progress toward product introduction, including phase-change RAM (PCRAM) and magnetoresistive RAM (MRAM), while resistance RAM (ReRAM or RRAM) is gaining ground for future applications.

Current state-of-the-art results from ISSCC 2012 include:

- the first SRAM using FinFETs operating at 4.6 GHz using trigate devices with assist circuits for lower  $V_{CC_{min}}$
- a density-record-beating 19-nm, 128-Gb TLC NAND flash memory
- a new DDR4 3.2-Gb/s/pin, 4-Gb, 30-nm SDRAM with PVT-tolerant data fetch
- a high-speed 443-MB/s-write-throughput, multilayered, cross-point ReRAM macro.

## SRAM

Embedded SRAM continues to be an important element in a wide range of very large scale integration (VLSI) applications, from high-performance processors to handheld devices. Historically, the SRAM bit cell has followed Moore's law, shrinking in area by about 50% with each new generation, as shown in Figure 13. This reduction has enabled designers to put more SRAM bits on each die, improving performance. Another key performance metric for SRAM design is the

lowest reliable operating voltage. A low value lets memory blocks operate reliably with the same (or better) power envelope, as compared with the previous generation. As the transistor feature size marches below 20 nm, device variation has made it very difficult to shrink the bit-cell area at the 50% rate while maintaining or lowering  $V_{CC_{min}}$  between generations. Starting at 45 nm, the introduction of high- $\kappa$  metal gates has reduced the  $V_t$  mismatch and enabled further device scaling by significantly reducing the equivalent

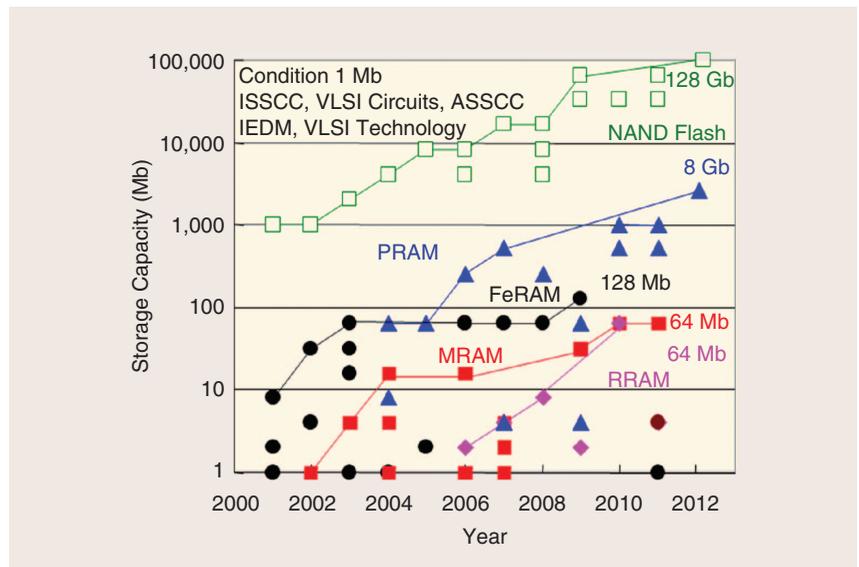


FIGURE 14: Trends in emerging NVM memory capacity.

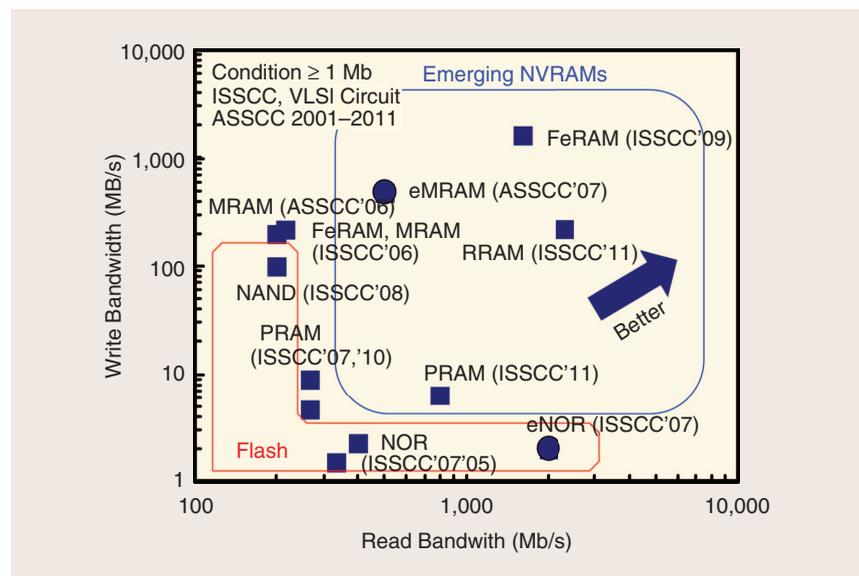
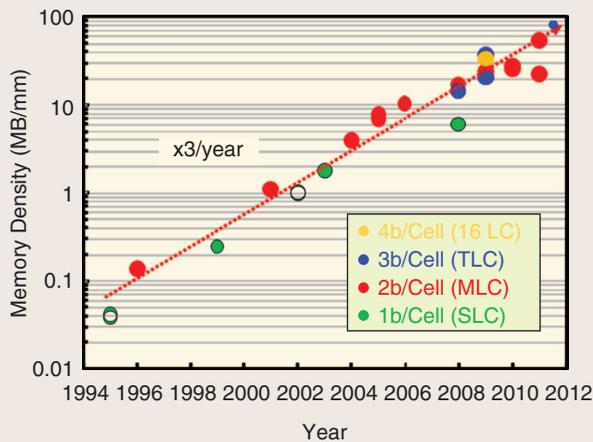
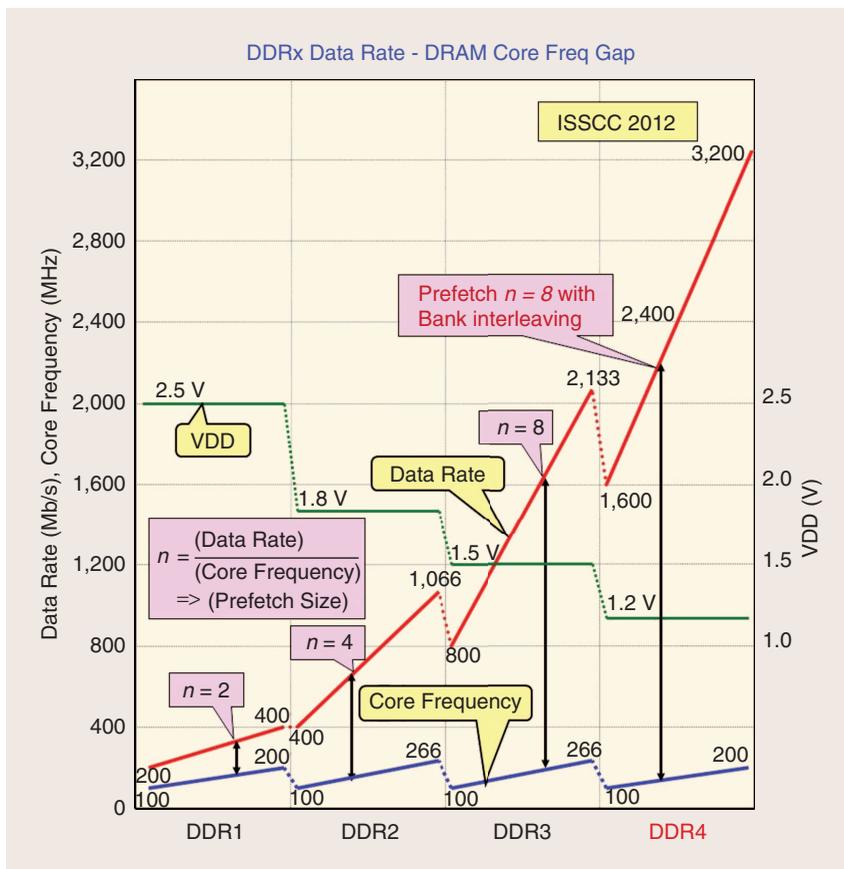


FIGURE 15: Trends in read/write bandwidth for NVMs.



**FIGURE 16:** Trends in NAND flash memory.



**FIGURE 17:** Trends for DRAM and high-speed I/O for DDRx.

oxide thickness. Design solutions such as read/write assist circuitry have been used to improve the  $V_{CC_{min}}$  performance at the memory-macro level for 32 nm and beyond. New transistor structures such as Fin-FET and FD-SOI are emerging as the replacement for planar devices to

enable further area reduction and  $V_{CC_{min}}$  scaling of SRAM bit cells.

### Nonvolatile Memories

In recent years, technological and chip development for emerging nonvolatile memories (NVMs) has been intensified, using advanced materi-

als. The emerging NVMs, such as PCRAM, ferroelectric RAM (FeRAM), MRAM, and ReRAM, all have excellent read/write and endurance performance, as well as low power requirements as compared with flash memory. These new NVMs offer the potential to open up new markets and applications. Commercial uses have been very slow to appear because of the rapid reduction of per-bit costs of conventional flash memory technologies already on the market, as shown in Figure 14. But the new technologies seem set to capture some specific markets by taking advantage of merits such as high read/write bandwidth (in the hundreds of megabytes per second), as shown in Figure 15. This year, ISSCC 2012 will report on a number of high-density 20-nm and sub-20-nm designs.

### NAND Flash Logic

Over the past few years, significant developments in NAND flash memory have resulted in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard disk drives by solid-state disks (SSDs). With physical scaling, accompanied by advancing multilevel storage cell concepts, a 128-Gb/die capacity is being demonstrated at ISSCC 2012, using 19-nm technology with 3-b/cell operation. Figure 16 shows the observed trend in NAND flash capacities presented at ISSCC over the past 17 years. As process feature size shrinks, error rates rise, requiring system designers to develop more-sophisticated controllers to compensate, some of which are utilized outside the NAND silicon, in the system-memory controller.

### DRAM and High-Speed I/O

The gap between on-chip memory and processor frequencies and external data rates continues to increase as conventional high-speed wired interface schemes [such as DDRx and graphics DDRx (GDDRx) for DRAM and NAND flash memory]

evolve, as shown in Figures 17 and 18. This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. Alternatives that accommodate high data rates through the use of wider or differential interfaces will, however, face the problems of increased pin counts and enlarged silicon areas. Combined with 3-D integration of memory and memory logic in near-future commercial products, new interface technologies with more memory stacking will yield lower-power and higher-bandwidth interfaces. This year, at ISSCC 2012, the first implementations of new standards of LPDDR3 and DDR4 enabled by through-silicon via (TSV) technologies for 3-D ICs will be described.

### Radio Frequency (RF)

On the horizon for RF, there are three trends that are converging, driven by their applications. The first concerns the well-established cellular market, where the demand is focused on high-mobility terminals providing high data rates, such as LTE-dedicated devices. The second trend addresses the connectivity sector, where the demand of extremely high data rates (equal to or above 1 Gb/s) is essential in devices incorporating several coexisting standards. At the end of May 2011, a press release announced the first product on the market with extended connectivity features such as dual Wi-Fi, Bluetooth, and 60-GHz WiGig standard compliance. Finally, the third application-driven trend concerns sensor networks, where the major features are low data rates and, above all, ultralow power (including devices using self-contained power).

The implementation of all these product families relies on two technology trends. First of all, transceiver integration performed either monolithically or using a 3-D heterogeneous scheme pushes toward the ultimate air interface. Hence, a large majority of current devices show full integration up to the antenna(s), as

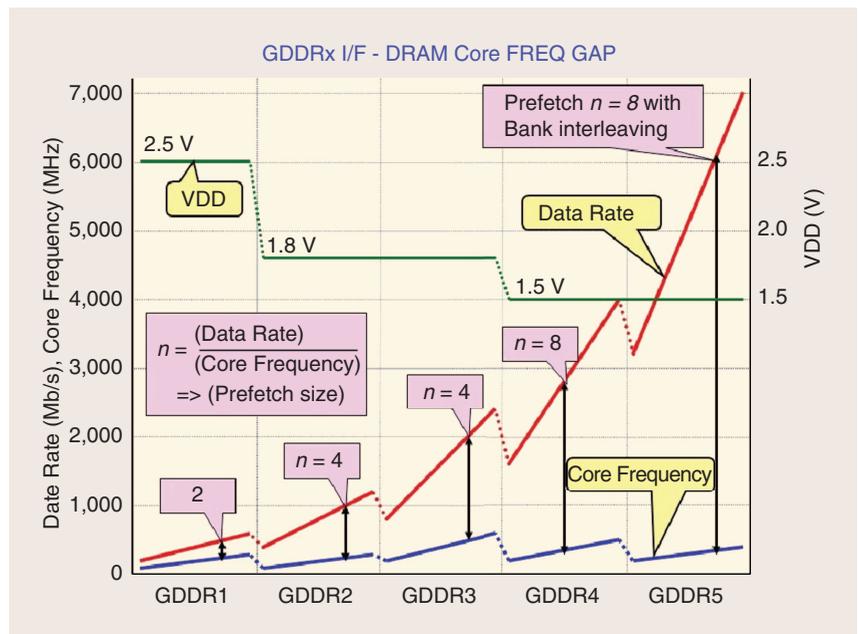


FIGURE 18: Trends in DRAM and high-speed I/O for GDDRx.

well as the absence of bulky external SAW or BAW filters at the RF interface. Second, there is a consolidating trend toward using multiradio SOCs in an increasing majority of products.

In emerging applications, the most advanced sub-nm CMOS technology has opened some application fields reserved thus far for III-V electronics. Over the past few years, more and more academic and research institutions have investigated fully integrated CMOS ICs for THz imaging and sensing. Furthermore, carrier frequencies above 100 GHz are well placed for very-high-data-rate communications (10–20 Gb/s), an application formerly reserved for wireline technology.

ISSCC 2012 is highlighting the following critical building blocks addressing these applications.

### Cellular Voltage-Controlled Oscillators (VCOs)

The VCO and its digital counterpart, the digitally controlled oscillator (DCO), form a traditional bottleneck in radio design, where they provide the RF reference frequency needed in all transceivers. The key features of VCOs and DCOs are oscillation frequency, frequency-tuning range,

spectral purity (usually quoted in terms of phase noise), and power consumption. A typical trade-off in VCO and DCO design involves phase noise, power consumption, and tuning range. Achieving the phase noise performance mandated by the 2G, 3G, and 4G cellular radio standards requires a VCO/DCO power consumption that is often a significant part of the total power budget, especially if a large tuning range is needed in order to cover many bands and standards.

A noticeable trend in VCO and DCO design is to let them oscillate at a center frequency of approximately 8 GHz with a sufficiently large tuning range and to recover cellular frequencies via frequency division by four or eight. This is shown in Figure 19, which displays the phase noise at 1 MHz versus the oscillation frequency of some of the most significant VCOs and DCOs published in the past five years. It is apparent that the rate at which phase noise increases with frequency is reduced thanks to the “free-running” solution, which also allows for a substantial improvement of the phase-noise FoM, demonstrating the noise-power trade-off, as shown in Figure 20. A second trend is to design VCOs and DCOs with a larger tuning range to cover newer



## Power Amplifiers (PAs)

Since the introduction of CMOS cellular PAs in 2002, continuing efforts and new design techniques have improved their performance. While in the beginning an attempt was made to deliver enough output power using 2G and 2.5G standards, recently the focus has shifted to supporting non-constant-envelope modulations, improving power efficiency, and supporting more bands with one PA. All the PAs introduced at ISSCC 2012 target wide-band code division multiple access (WCDMA), with a need to support 64QAM; one of them covers three bands, as shown in Figures 21 and 22.

With respect to power amplifiers at millimeter-wave frequencies, the new trend is toward higher power-added efficiency (PAE) while maintaining compliance with process-reliability concerns. The 77-GHz PA reported at ISSCC 2012 demonstrates a record in PAE and a near record in saturated output power, as shown in Figure 23.

### Technology Directions (TD)

The role of the Technology Directions Subcommittee is to identify and encourage developments of potential importance in the ongoing evolution of ISSCC. Characteristically, a wide variety of topics are covered, some new and some continuing, with success achieved by the transference of the emerging technique to one of the evolving mainstream subcommittees.

### Large-Area, Low-Temperature Electronics

A clear breakthrough in research for large-area electronics in the past decade has been the development of thin-film transistor (TFT) processes with an extremely low temperature budget. Thanks to the low temperatures required in manufacturing (<150 °C), these TFTs can be placed on flexible and inexpensive substrates like plastic films and paper.

The semiconductor materials used for these developments have for a long time been carbon-based organic molecules such as pentacene (a p-type

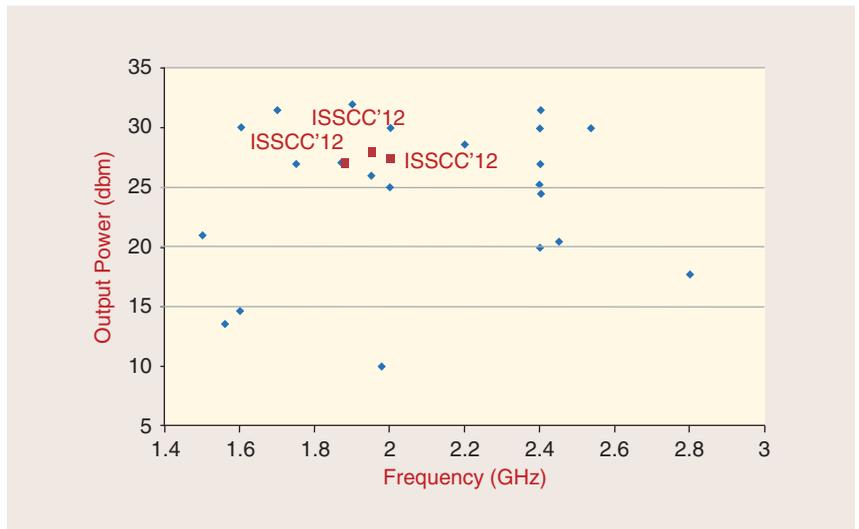


FIGURE 21: Frequency (GHz) versus output power (dbm) for RF PAs.

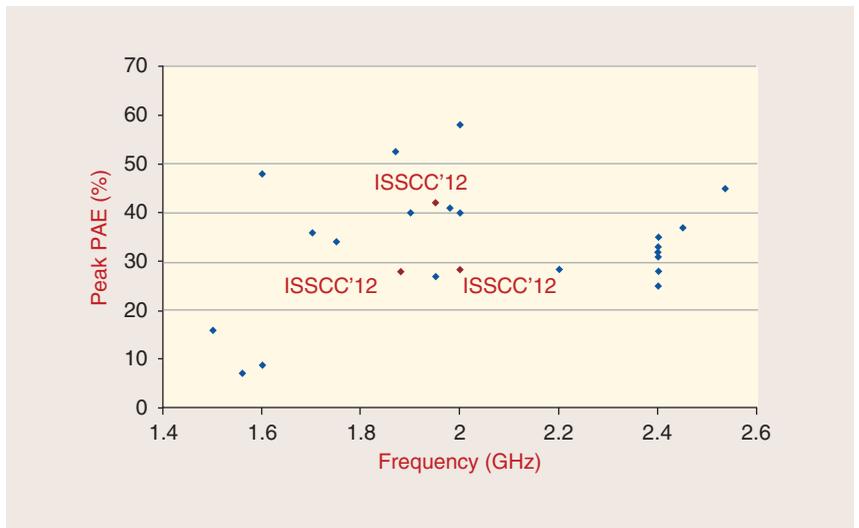


FIGURE 22: Frequency (GHz) versus peak PAE for RF PAs.

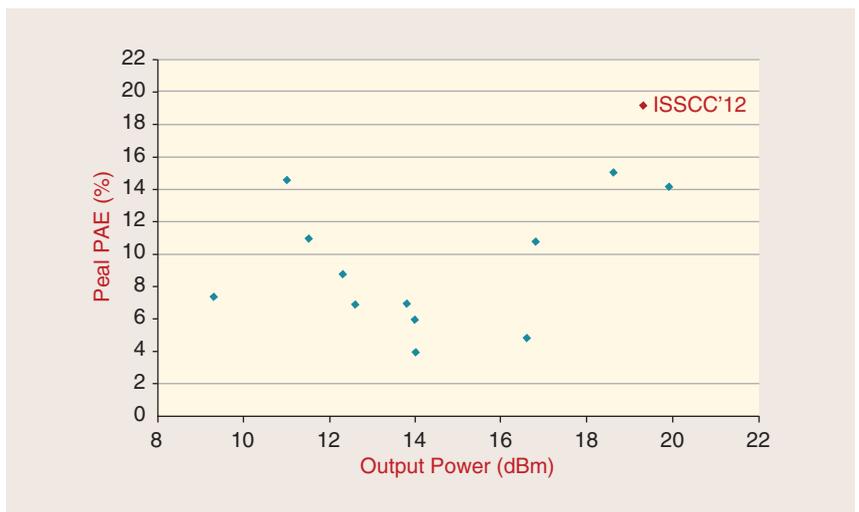
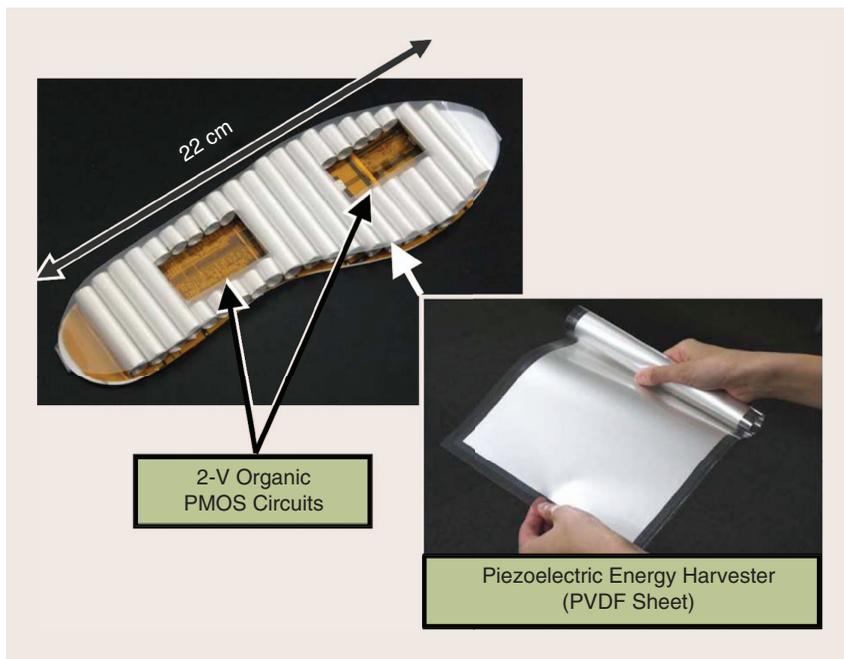


FIGURE 23: Saturated output power (dBm) versus peak PAE for millimeter-wave PAs.



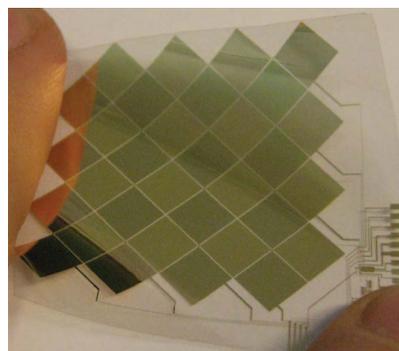
**FIGURE 24:** A flexible insole pedometer: a device that counts steps while being powered by the movement of the foot itself, made with an organic piezoelectric foil (PVDF) coupled to an organic p-type circuit. (Used with permission from ISSCC.)

semiconductor). More recently, organic n-type semiconductors and amorphous metal oxides, which are also n-type semiconductors, have emerged. Popular metal-oxide semiconductors are zinc oxide (ZnO) and amorphous indium-gallium-zinc oxide (IGZO or GIZO). The mobility of n- and p-type organic materials has reached values around  $1 \text{ cm}^2/\text{V}_s$ , while metal oxides have surpassed the  $10\text{-cm}^2/\text{V}_s$  mark. The operational stability of all semiconductor materials has greatly improved and should be sufficient to enable commercial applications, especially in combination with the large-area compatible barrier layers used to seal the transistor stack.

At the current state of the art, p-type-only, n-type-only, and complementary technologies are available. Most TFTs are still manufactured with subtractive methods based on lithography, but there is a clear emphasis on the development of additive technologies that could provide higher production throughput. These are based on various technologies borrowed from the graphic printing world, such as gravure, screen printing, and offset.

The technology road map in the field of large-area and low-temperature electronics thus focuses on lowering the cost per unit area instead of increasing the number of functions per unit area, which is the focus of monocrystalline Si technology according to Moore's law.

Traditional applications such as flexible displays and electronic RFID tags integrated in the wrapping of retail goods, together with the improvement of TFT performance, reliability, and aging stability, have enabled first prototypes of applications integrating sensors and actuators with low-



**FIGURE 25:** A touch pad using a capacitive sensor employing organic p-type transistors. (Used with permission from ISSCC.)

temperature TFTs. Examples include signage, pressure- and light-sensitive foils, sheets capable of distributing RF power to appliances, and energy-scavenging devices.

Following this trend, ISSCC 2012 features a flexible pedometer powered by foot motion, a flexible touch pad based on organic TFTs, an RFID capable of bidirectional communication using organic and metal-oxide TFTs, and an IGZO DAC that can be used as an integrated column driver in OLED display backplanes, as shown in Figures 24 and 25.

### Wireless

Data rates for modern wireless standards are increasing rapidly. This is evident from cellular standard trends, as shown in Figure 26. In fact, the data rate has increased by a factor of 100 over the past decade, and another increase by a factor of ten is projected over the next five years. This trend has been maintained by using more complex modulation techniques such as orthogonal-frequency-division multiplexing (OFDM) for better spectral efficiency but has come at the cost of increased requirements for digital signal processing (DSP). In addition, the expansion of channel bandwidth is also an effective way to achieve a data-rate increase. This can be seen in the wireless-connectivity trend chart (for 802.11x) in Figure 27. It is clear from the figure that channel bandwidth for the WLAN standards has increased from the traditional 20 MHz (802.11g) to 40 MHz (802.11n), then to 160 MHz (802.11ac), and finally to >1 GHz (802.11ad). Because the available spectrum is limited in the low-GHz range, to achieve >1-GHz channel bandwidth, the carrier frequency has been moved from 2.4/5 GHz (802.11a/b/g/n) to 60 GHz (802.11ad) in the millimeter-wave range.

With the spectrum available in the 60-GHz range, data rates greater than 1 Gb/s can be achieved with modest modulation. The initial feasibility of 60-GHz CMOS was demonstrated in

2009. Then a Silicon Valley start-up, SiBeam, demonstrated a complete end-to-end system that supports a robust wireless link in 60 GHz and achieves 3.8 Gb/s in 1.76 GHz. This demonstration ignited more research and development from both academia and industry in millimeter-wave communication.

An old problem sees a new solution. As wireless applications proliferate, the spectrum is becoming very crowded because of the many licensed and unlicensed uses occupying most of the assigned frequency bands. But cognitive radio is an answer: it promises to identify and utilize spectral “white space” in the presence of many other wireless applications. And so the current trend for cognitive radio is to design highly linear transceivers that can cover a very wide frequency range, with various channel bandwidths. As a consequence of these high-linearity wide-band design requirements, distortion-cancellation and tunable-RF channel-selection techniques are critical. Most transceivers in this category are adopting digital calibration and analog feedback techniques to increase the linearity performance for a very tunable front end so as to cover a wide range of frequencies.

On another front, wireless sensor networks (WSNs) require ultralow-power radio to increase the lifetime of the battery—or better still, to eliminate the battery completely using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. Wake-up radio thus becomes one of the main building blocks of each WSN node. Once the radio awakens, power efficiency becomes the main target for both high- and low-data-rate communication. Such WSNs will enable electronics for sustainability.

### Wireline

Wireline continues to be an important application of semiconductor technology as the need for wired

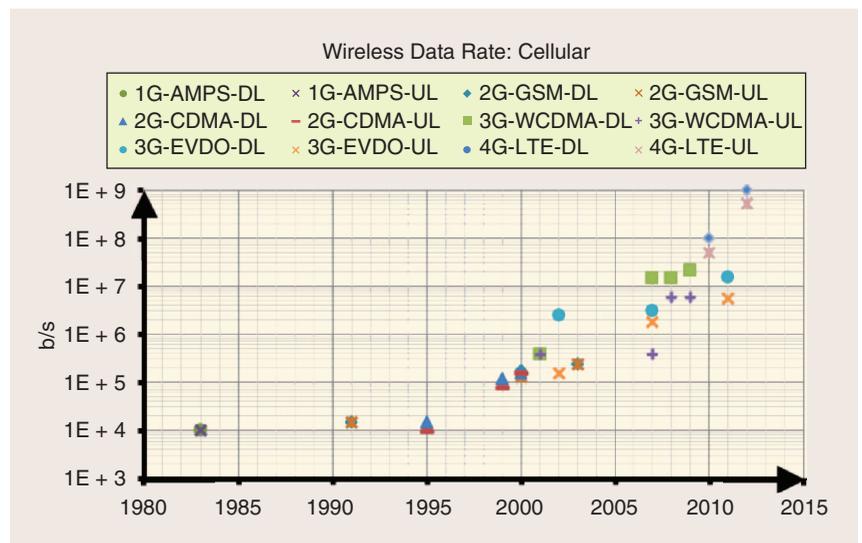


FIGURE 26: Trends in cellular-standards data rates.

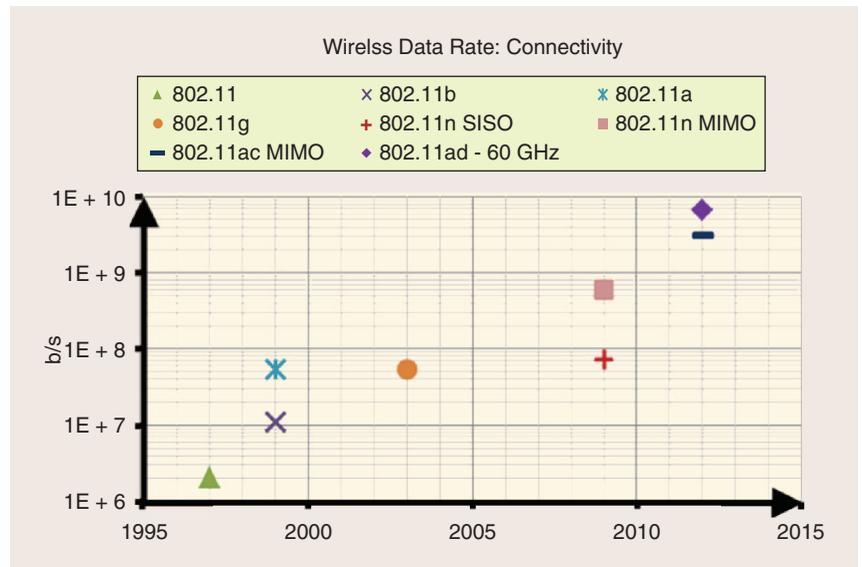


FIGURE 27: Trends in the data rates of wireless-connectivity standards (802.11x).

communication flows out from its long distance origins into smaller and smaller environments, through backplanes to inter- and intrachip connection. A continuing challenge in this evolution is the adaptation of techniques that originated on a large scale to shrinking environments.

High-speed I/O bandwidth needs are increasing by about a factor of two each year as the requirements for data transmission gather momentum, driven by the use of the cloud and data streaming. Along with the increase in data rates, such systems are also rapidly approaching power limits that constrain the I/O band-

widths. There is also a need for backward compatibility across the legacy-interconnect chassis that adds to the development challenge.

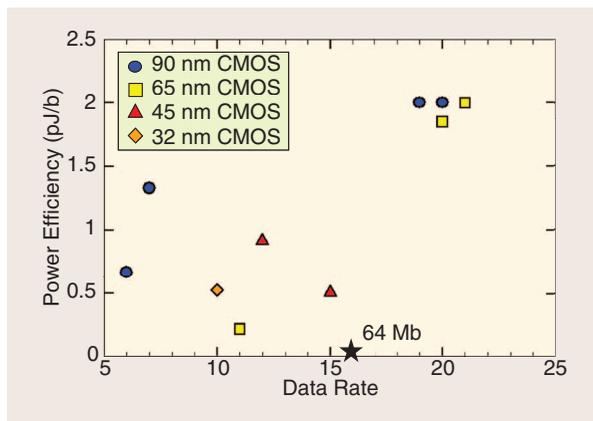
Wireline interconnects using serial links—once a niche application in high-speed network routers—are now used in a wide range of applications, from high-speed microprocessors to data converters. To meet integration requirements, these serial links must have lower power, even as performance increases. Hence, a typical FoM considers the energy required per transmit/receive bit or pJ/bit, which is the ratio of the power in milliwatts to the data rate in gigabits per second, or mW/Gb/s.

The past five years have seen serial-link speeds increasing from 1 Gb/s, but a barrier appears to be approaching fast. Although limited, specialized 40 Gb/s links have been developed for telecom applications, and initial 40 Gb/s links have been demonstrated in the lab; links able to support a broad set of applications at rates above 40 Gb/s or able to support 50 Gb/s rates at all are conspicuously absent commercially.

Therefore, although the system challenges require data bandwidth to increase by a factor of about two each year, existing technology only allows data rates to increase by a factor of two every five years. At the same time, the need to support a variety of data channels, including legacy compatibility, with a very large number of parallel links means that equalization techniques are essential for robust data transmission. Receiver equalization methods include the “linear” type, for boosting the signals for shorter and less complex channels, and “decision feedback,” for more complex channels with interchannel crosstalk. These equalization techniques add to the power consumed by the links, however.

Figure 28 shows the energy efficiency per bit of equalizing receivers reported since 2007. The state of the art is around 0.5 pJ/b for equalizers operating at less than 20 Gb/s. At higher data rates, however, the energy efficiency is still greater than 1 pJ/b. This year, ISSCC 2012 is presenting best-in-class performance in terms of data rate at 16 Gb/s with energy efficiency of less than 0.5 pJ/b, showing the extension of low-power equalizers to higher data rates.

For a combined transmitter and receiver channel, the mW/Gb/s FoM depends on the target application. Today, for short-reach serial



**FIGURE 28:** Power efficiency of equalizing receivers. The star represents the low-power equalizer operating at 16 GB/s and consuming <0.5 pJ/b, as reported at ISSCC 2012.

links where the equalization is not as complex, achievable power numbers are of the order of 1–5 mW/Gb/s; state-of-the-art 10-Gb/s links typically consume between 10 and 50 mW. For higher data rates (in the range of 25–30 Gb/s), the efficiency is typically lower because of the additional clock and analog performance requirements imposed by the high data rate. The state of the art at these data rates is therefore in the range of 8–10 mW/Gb/s.

Long-reach links and more complex channels such as copper backplanes that include multiple connectors have much higher power consumption and lower efficiency in terms of mW/Gb/s. This year, ISSCC 2012 is presenting the first 28-Gb/s transceiver to address medium-reach applications using 32-nm SOI and consuming 693 mW for 35 db of channel loss with an FoM of 24.75 mW/Gb/s.

These trends in integration, power consumption, and applications bring new challenges to wireline communications. New techniques are required to ensure continued downscaling of the links, and improvements in equalization techniques, transmitter design, receiver design, and clock distribution are essential. ISSCC 2012 will highlight many of the new techniques that continue to enhance the field.

## Summary

Developments reported at ISSCC 2012 continue to present breakthroughs in the broad domain of solid-state circuits and systems. In this rich environment, presentations at ISSCC characteristically predict ways in which electronics techniques will fulfill the present and future needs of society. In this role, ISSCC continues to present a road map of things to come, both in the immediate future and in the longer term.

## Acknowledgments

The authors wish to acknowledge the creators of the original material from which this article has been structured. While this has been largely a team effort by several members of each subcommittee, each has operated under the direction of his or her subcommittee chair, as listed below:

- Analog: Bill Redman-White, NXP Semiconductors
- Data Converters: Venu Gopinathan, Texas Instruments
- Energy-Efficient Digital: Tzi-Dar Chiueh, National Chip Implementation Center
- High-Performance Digital: Stefan Rusu, Intel
- Imagers, MEMS, Medical, and Displays: Roland Thewes, TU Berlin
- Memory: Kevin Zhang, Intel
- Radio Frequency: Andreia Cathelin, STMicroelectronics
- Technology Directions: Siva Narendra, Tyfone
- Wireless: David Su, Atheros Communications
- Wireline: Daniel Friedman, IBM Thomas J. Watson Research Center.

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