Print:
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University of Toronto
Faculty of Applied Science and Engineering

Midterm Examination – October 1997

ECE352F – Computer Organization

Examiner – Paul Chow

1. There are 5 questions and **12** pages. Do **all** questions. The total number of marks is 80.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. Please put your final solution in the box if one is provided.
4. **No calculators or other computing devices allowed.**
5. **Paper Type D** – You may use a VHDL reference manual.

1 [20]	
2 [15]	
3 [15]	
4 [15]	
5 [15]	
Total [80]	

[20 marks] 1. An asynchronous circuit has two inputs, x_1 and x_2, and one output Z. The output is 1 if and only if the input is $x_1 = x_2 = 1$ and the preceding state is $x_1 = 0$ and $x_2 = 1$.

(a) Show the primitive flow table.

(b) Show the implication table and the merger graph. Indicate the set of compatibles that you will use in a reduced flow table.

(c) Show a reduced flow table, and fill in all of the outputs.

(d) Do a state assignment and show the state table.

(e) Derive the equations and show a circuit diagram.

[15 marks] 2. A soon to be bankrupt company wants to implement a new computer called the $N\Psi$-352 using a single-bus structure as shown in Figure 1. It shows the PC, MDR (memory data register), MAR (memory address register), register bank (r0-r31), IR (instruction register), IMMED (immediate field in the instruction) and the ALU. Also given are the control signals. For example, the microcode word:

PC.out, Y.in

transfers the contents of the PC to the Y register.

(a) Give a possible three-bus structure for the $N\Psi$-352. Two buses are for the source operands and one is for the result. The register file cannot be read and written in the same cycle. Show the necessary control signals in the same format as in Figure 1.

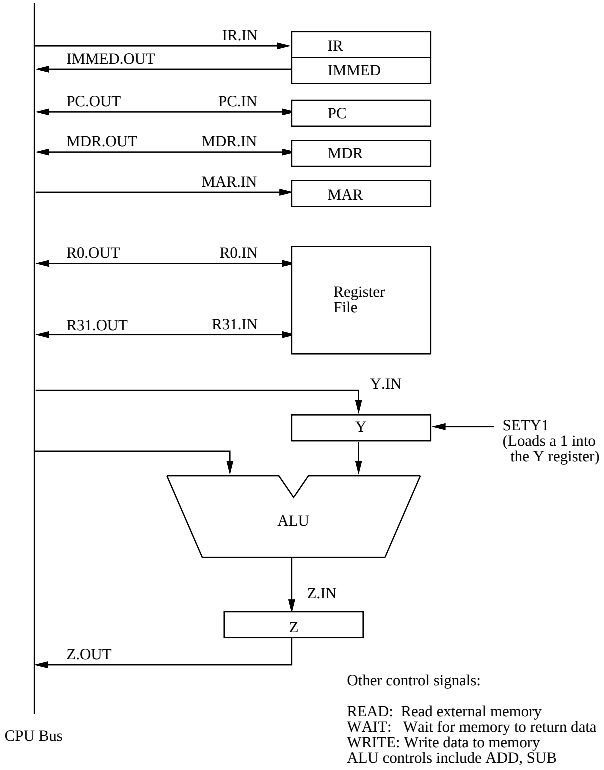

Figure 1: Internal structure of the $N\Psi$-352

(b) For the $N\Psi$-352 instruction

```
add r1,r2,r3      % r3 <- r1 + r2
```

give the microcode sequences using the single-bus structure of Figure 1 and your three-bus structure. Remember to update the PC and be sure to comment your microcode clearly.

Comment on the differences between the microcode for the two structures, and the hardware needed to implement the two structures.

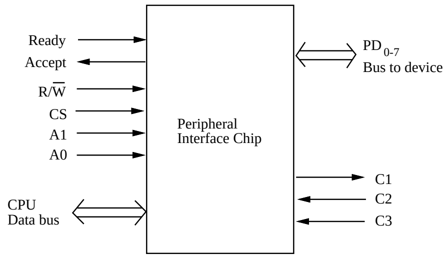

Figure 2: Simple peripheral interface

[15 marks] 3. A simple peripheral interface chip (PIC) is shown in Figure 2. The signals are defined as follows:

Ready Set to 1 by the CPU to indicate that the Address is valid. Set to 0 by the CPU to indicate the end of the transfer.

Accept Set to 1 by the PIC when the data has been accepted (during a write by the CPU) or when data is valid (for reading by the CPU).

R/$\overline{\mathbf{W}}$ Set to 1 by the CPU during a read operation and 0 during a write operation.

CS Chip select. Set to 1 during all bus transactions.

A1,A0 Address lines to access the PIC registers.

PD0-7 Peripheral data bus.

C1 Output control line.

C2 Input control line.

C3 Input control line.

(a) The CPU has a 16-bit address bus. The PIC is to be located in the address range $BEEC_{16}$ to $BEEF_{16}$. Show the logic and connections needed between the CPU address bus and the PIC.

(b) You are to use the PIC as an interface to a printer with an 8-bit parallel data bus. The printer bus has three control lines:

DSTROBE This is pulsed low to indicate that there is valid data on the data bus.
P_ACK The printer pulses this line low when it has latched the data on the data bus.
P_BUSY This is set high by the printer when the printer cannot accept new data.

Show how the PIC can be connected to the printer control lines and data bus.

Give a timing diagram to specify the required actions of **C1**, **C2**, and **C3** to reliably transfer data on $\mathbf{PD}_{0-7}$ using asynchronous control with full handshaking. Your timing diagram should show all of the control signals on the bus, and the times when data must be valid on the data bus.

[15 marks] 4. Write a synthesizable VHDL description for the printer interface described in Question 3b. The printer interface will obviously have some logic to control the actual printer mechanism once it has the data to print. Just indicate with comments where this would go in your code. Use the back of the page for extra space. Indicate this clearly.

[15 marks] 5. Assume that you have full adder circuits that have inputs x_i, y_i, and c_i. The outputs, s_i and c_{i+1}, are stable after 2 gate delays from the inputs. There are 4-bit carry-lookahead (CLA) units where the P_i and G_i values are available after 1 gate delay.

A 16x16 multiplier is to be built. Compare the delay using an array implementation and an implementation using a carry-save adder tree. You may use as much CLA logic as you can to make long adders faster. If you need other gates, assume that they have a delay of 1.

Show clearly with diagrams the structure of your multipliers and how you are deriving your delays. Structure does not mean that you have to draw the whole circuit, just enough to show how it is being put together.