Print:

First Name:............................ Last Name:............................

Student Number:..

University of Toronto
Faculty of Applied Science and Engineering

Midterm Examination – November 1998

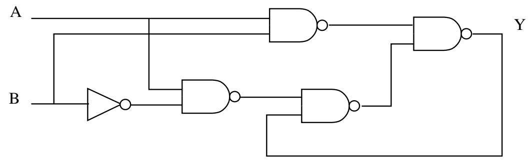
ECE352F – Computer Organization

Examiner – Paul Chow

1. There are 5 questions and **10** pages. Do **all** questions. The total number of marks is 80. The duration of the test is 90 minutes.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. Please put your final solution in the box if one is provided.
4. **No calculators or other computing devices allowed.**
5. **Paper Type D** – To help you with VHDL, you may use a VHDL reference manual, text, or reference notes.

1 [15]	
2 [12]	
3 [20]	
4 [20]	
5 [13]	
Total [80]	

1. Consider the asynchronous circuit shown below:



[8 marks] (a) Derive the transition table for this circuit.

[1 marks] (b) How many stable states does this circuit have?

[3 marks] (c) How can this circuit be used as memory element to store data?

[3 marks] (d) Assuming the two inputs are allowed to change at the same time, are there any critical races? Prove your answer.

2. Consider the following flow table for an asynchronous state machine:

	x_1x_2			
	00	01	11	10
a	$\boxed{\text{a}}$,0	b,-	-,-	e,-
b	a,-	$\boxed{\text{b}}$,0	c,-	-,-
c	-,-	d,-	$\boxed{\text{c}}$,0	e,-
d	a,-	$\boxed{\text{d}}$,1	-,-	-,-
e	f,-	-,-	c,-	$\boxed{\text{e}}$,0
f	$\boxed{\text{f}}$,1	d,-	-,-	e,-

[5 marks] (a) Find the compatible pairs using an implication table.

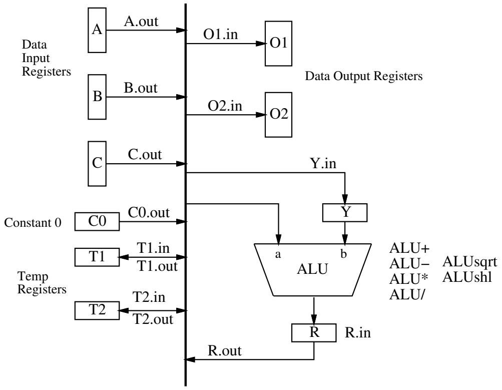
[3 marks] (b) Find the maximal compatibles

[4 marks] (c) Find a closed covering set of compatibles and give a reduced flow table. Only combine the minimum number of states necessary to get the minimum number of states.

3. With the datapath and control signals shown below you are to compute the function:

$$\begin{aligned} O1 &= -b - \sqrt{b^2 - 4ac} \\ O2 &= -b + \sqrt{b^2 - 4ac} \end{aligned}$$

Note that the ALU operations assume **a OP b** where **OP** is one of **+ − * /**. The unary operations, square root and shift left one bit, operate on input **a**.



[10 marks] (a) Give the control steps required to compute the functions for *O1* and *O2*. If you need extra resources (like more temporary registers) or other control signals, you may add them, but be sure to document what they are and why you need them. You may assume that the registers are edge-triggered. Try to minimize the number of control steps. **Comment your code.** *The easier it is to understand, the easier it is to give more marks!*

[4 marks] (b) Show the structure for a microcode controller and how it could be used to control this datapath.

[4 marks] (c) Assuming that the controller for this datapath will use horizontal microcode, show the contents of the microcode memory for the first three steps in your control sequence.

[2 marks] (d) What are the advantages and disadvantages of microcoded control versus hardwired control?

4. You have available any number of full-adder cells (FA) and 4-bit carry lookahead units (CLA). Assume that a FA has a delay of 2 units from any input to any output and a CLA has a delay of 3 units from any input to any output.

You need to add four 16-bit numbers and generate a 16-bit result. You may assume that the result will fit in 16 bits.

[1 marks] (a) If you had to assume the worst case result size, how many bits would you have in your result? Explain your answer.

Bits = $\boxed{}$

[2 marks] (b) What is the delay for a 16-bit ripple carry adder? Explain.

Ripple delay = $\boxed{}$

[2 marks] (c) What is the delay for a 16-bit CLA adder? Explain.

CLA delay = $\boxed{}$

[1 mark] (d) Assume that you were going to carry out the addition in the following way:

$$((A+B)+C)+D$$

What would be the worst case delay using CLA adders?

CLA delay = $\boxed{}$

[1 mark] (e) Assume that you were going to carry out the addition in the following way:

$$(A+B)+(C+D)$$

What would be the worst case delay using CLA adders?

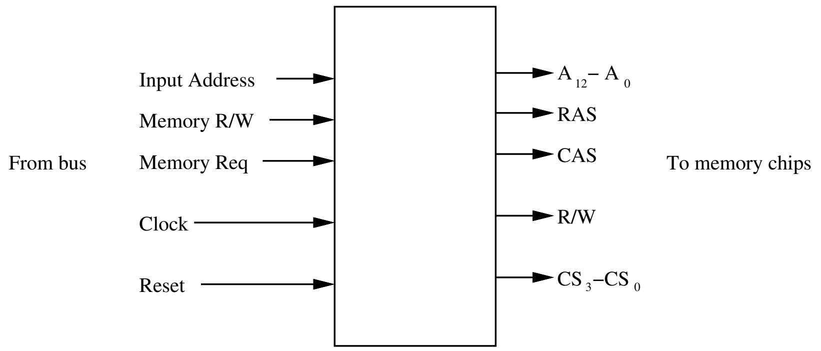
CLA delay = $\boxed{}$

[10 marks] (f) Draw the circuit diagram showing the connections needed at the bottom four bits (i.e., you do not need to show the connections for all 16 bits) for a *carry-save* adder (CSA) that can be used to add the four numbers. Build the fastest adder.

[3 marks] (g) What is the delay of this adder? Explain.

CSA delay = $\boxed{}$

5. A simple DRAM controller is pictured below:



The output lines connect to the memory chips in the memory bank. Their functions are:

$A_{12} - A_0$ Address lines to memory

RAS and CAS Row and column address strobes

R/W Read/Write line to memory

$CS_3 - CS_0$ Chip selects.

For the inputs:

Input Address These are the address lines from the bus.

Memory R/W Indicates whether to read or write

Clock Clock for the controller

Memory Request Starts a memory cycle when it goes high

Reset Puts the controller in a known state

Assume that the memory is 8-bits wide and accessed one byte at a time. The DRAM chips are 1-bit wide, with a single data port for reading and writing.

[2 marks] (a) What is the largest DRAM chip that can be handled by this controller? Explain.

Chip size = $\boxed{}$

[2 marks] (b) What is the largest memory, in bytes, that can be handled by this controller? Explain.

Memory size = $\boxed{}$

[9 marks] (c) Show how to connect the DRAM controller to the memory chips for the largest memory that this controller can handle.

[No marks] 6. Sorry no VHDL question :-)