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Foundation Express User Guide

Introduction

Installation and Security

Tutorial

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Preface

About This Manual

This manual describes Xilinx's Foundation Express, a synthesis tool used to implement FPGA and CPLD designs. It describes how to install and license Foundation Express, and ways to apply its features to your chosen HDL design flow and FPGA or CPLD architecture.

Before using this manual, you should be familiar with the operations that are common to all Xilinx's software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *Development System Reference Guide.*

Other publications you can consult for related information are the *Foundation Express Application Note Supplement*, *Foundation User Guide* and the *Foundation Quick Start Guide.*

Manual Contents

This manual covers the following topics.

- Chapter 1, "Introduction," discusses what Foundation Express is, its benefits, and how to use it in your design flow.
- Chapter 2, "Installation and Security," explains how to install Foundation Express and how to set up your license.
- Chapter 3, "Tutorial," explains how to create design source files, set up a project, and synthesize a design. It also explains how to enter design constraints, optimize the design logic, analyze timing, and how to generate an optimized FPGA netlist and reports.

Conventions

Typographical

This manual uses the following conventions. An example illustrates each convention.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement.

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

  - Emphasis in text

    If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  `edif2ngd` [*option_name*] *design_name*

  Square brackets also enclose footnotes in tables that are printed out as hardcopy in DynaText®.

- Braces "{ }" enclose a list of items from which you choose one or more.

  `lowpwr ={on|off}`

- A vertical bar " | " separates items in a list of choices.

  `symbol` *editor_name* `[bus|pins]`

- A vertical ellipsis indicates repetitive material that has been omitted.

  ```
  IOB #1: Name = QOUT'
  IOB #2: Name = CLKIN'
  .
  .
  .
  ```

- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2* `...` *locn;*

Online Document

Xilinx has created several conventions for use within the DynaText online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click on the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click on the blue-underlined text to open the specified cross-reference.
- There are several types of icons.

  Iconized figures are identified by the figure icon.

Figure 1-1 Naming Conventions 

Iconized tables are identified by the table icon.

Table 13-14 Carry Modes 

The Copyright icon displays in the upper left corner on the first page of every Xilinx online document.

The DynaText footnote icon displays next to the footnoted text.

Macro 

Double-click on these icons to display figures, tables, copyright information, or footnotes in a separate window.

- Inline figures display within the text of a document. You can display these figures in a separate window by clicking on the figure.

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Chapter 1

Introduction

Welcome to Foundation Express, the Xilinx FPGA logic-synthesis solution. Foundation Express provides a powerful combination of Synopsys logic-synthesis and optimization technology, high-level design methodology, and an easy-to-use user interface to the FPGA design desktop.

This chapter discusses what Foundation Express is, its benefits, and how to use it in your design flow.

What Is Foundation Express?

Foundation Express is a complete FPGA logic-synthesis and optimization tool. With Foundation Express, you can create optimized FPGA netlists from VHDL code, Verilog HDL code, and existing, unoptimized FPGA netlists.

The Foundation Express performs the following steps:

1. Provides an integrated text editor you can use to enter VHDL® and Verilog® HDL source code for your design. You can use the text editor in the analysis step (described next) for easy design source file debugging.
2. Analyzes HDL (VHDL and Verilog HDL) design source files for correct syntax using the Synopsys® industry-standard HDL policy. Foundation Express accepts any combination of VHDL, Verilog HDL, and FPGA netlist files as sources for a single design. For example, you can use functions or subdesigns that are created in schematic capture and Verilog HDL within a VHDL top-level design.

   After you identify the design sources, Foundation Express analyzes the HDL files. If there are errors in the source files, the

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output window and text editor help you to find and correct problems.

3. Synthesizes logic from VHDL, Verilog HDL, and FPGA netlist source files, targeting a specific FPGA or CPLD architecture and device. Foundation Express synthesizes the logic of your design, using architecture-specific algorithms to target Xilinx devices. In this part of the design flow, each design module is elaborated and the design hierarchy is created and linked to form a unique design implementation.
4. Optimizes logic for speed and area as directed by your design constraints, generating an FPGA netlist file that is ready for place and route by the Xilinx implementation tools. Foundation Express optimizes the design as directed by your design constraints. With Foundation Express' graphical user interface (GUI), you can enter constraints for your design in editable tables. The constraints contain performance requirements and optimization options for architecture-specific optimization engines. When it has completed optimization, Foundation Express generates a netlist ready for place and route. Foundation Express also creates reports of its results.
5. Extracts and displays accurate post-synthesis delay information for timing analysis and debugging. Foundation Express displays timing information beside your design constraints and highlights timing violations so you can easily decide whether to place and route the design or make design changes.

How Foundation Express fits into the design flow is illustrated in the following figure.

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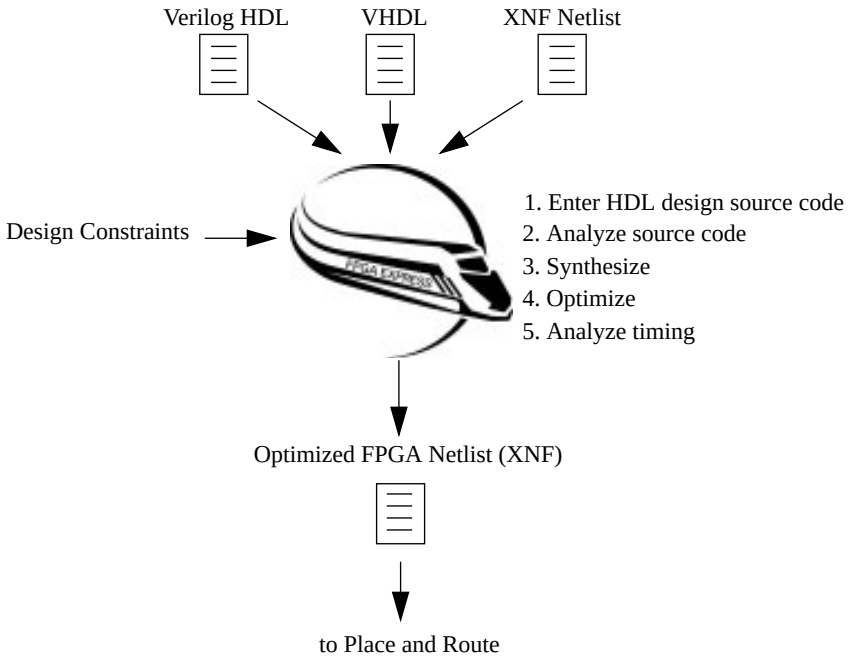

Figure 1-1 How Foundation Express Fits in the Design Flow

Benefits of Using Foundation Express

The benefits of using FPGA include adding control to the design process and assisting in migration to an HDL design methodology while using common, familiar systems.

Adding Control to the Design Process

Using Foundation Express, you can produce desired results without multiple design iterations. Because the target performance is entered in advance with design-specific constraints, there is little or no time spent in iteration cycles. System clock speed, port and path delay are some of the constraints that you can specify.

Migrating to HDL Design Methodology

If you are migrating from a schematic-based to an HDL-based design methodology, Foundation Express adds HDL logic synthesis and

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optimization to your current FPGA design environment. You can completely define an FPGA design with HDL source code or use a mixture of schematics and HDL source code to enter a design into Foundation Express.

Using an HDL-based design methodology increases productivity because HDL source code is vendor-independent, retargetable, and reusable. Because Foundation Express takes HDL source code as input, you have these advantages in addition to the Foundation Express optimization programs specifically tuned for each Xilinx device family.

Using Common, Familiar Systems

You can target the largest FPGAs and CPLDs using Windows 95® or Windows NT® operating systems. Foundation Express' Windows-compliant GUI uses standard commands and procedures to accept all your input values; no command scripts are required for constraint entry. If you need more information, context-sensitive and fully indexed online help is available.

Looking Inside Foundation Express

The Foundation Express logic synthesis and optimization tools convert HDL source code and unoptimized schematic netlists into optimized FPGA netlists. The synthesis design flow includes a small number of mandatory and optional tasks. The "Foundation Express Design Flow" figure shows the main tasks in the design flow.

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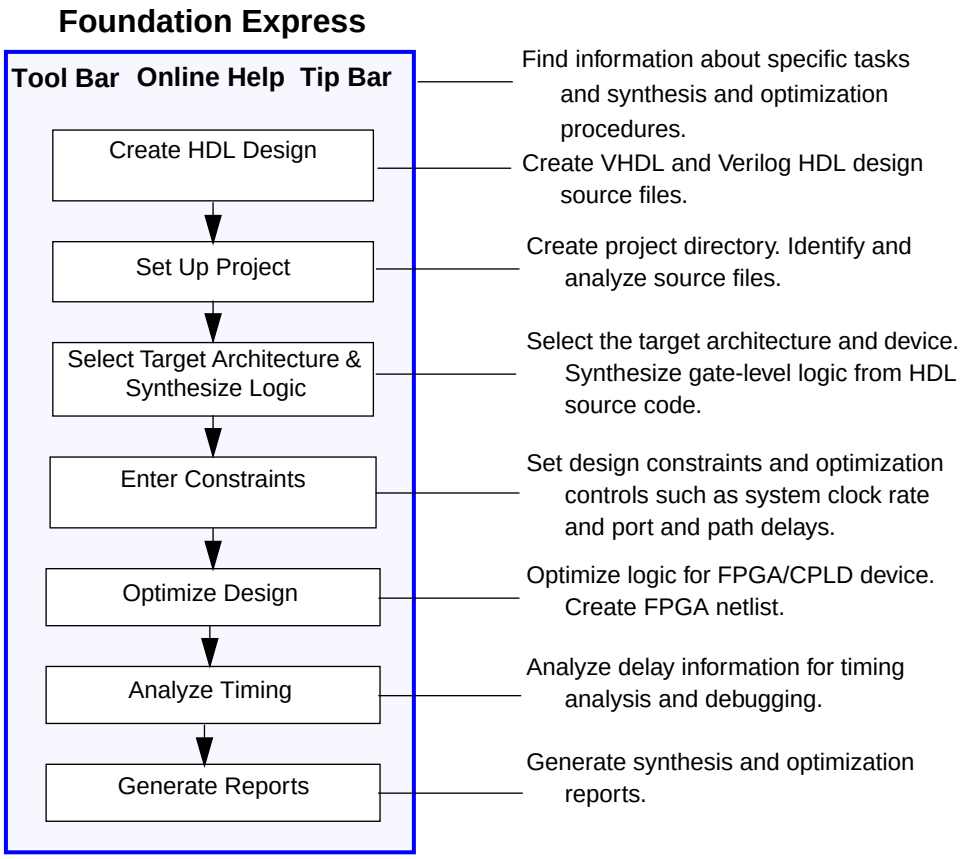

Figure 1-2 Foundation Express Design Flow

Foundation Express is designed so that you concentrate on your design rather than on the design tools. The tools and operations are logically arranged according to their function within the design flow so you can understand the process intuitively. To capture your design information, Foundation Express uses familiar, Windows-compliant dialog boxes and data entry windows.

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Using Foundation Express in Your Design Flow

Your design methodology determines how you use Foundation Express in your design flow. These are the three main FPGA design methodologies:

- HDL-based design methodology uses only HDL source code for design entry.

  You can enter one or more VHDL or Verilog HDL files describing any hierarchical design structure. You can then split the design into hierarchical, functional blocks or create a single flattened design description. This feature makes it easy to reuse modules from a common design library or design source.

- Schematic-based design methodology uses schematics for design entry.

  This design methodology adds only one step to a traditional FPGA design process, but it can produce improved area and performance.

- Mixed design methodology uses a combination of HDL source code and schematics for design entry.

  In this design methodology, the HDL source code is synthesized, combined with netlists from schematic entry, and optimized into a netlist ready for FPGA place and route tools.

  You can divide a design between HDL and schematic input in any proportion and create virtually any design hierarchy. You can also use functional blocks made from both schematics and HDL to reuse modules from common design libraries or design sources.

The “Different Design Environments” figure shows the flow of Foundation Express with other tools in the different design environments. The steps in this procedure are similar for the three environments; only the method of entering the design into Foundation Express differs. Using simulation to verify your design is an optional step.

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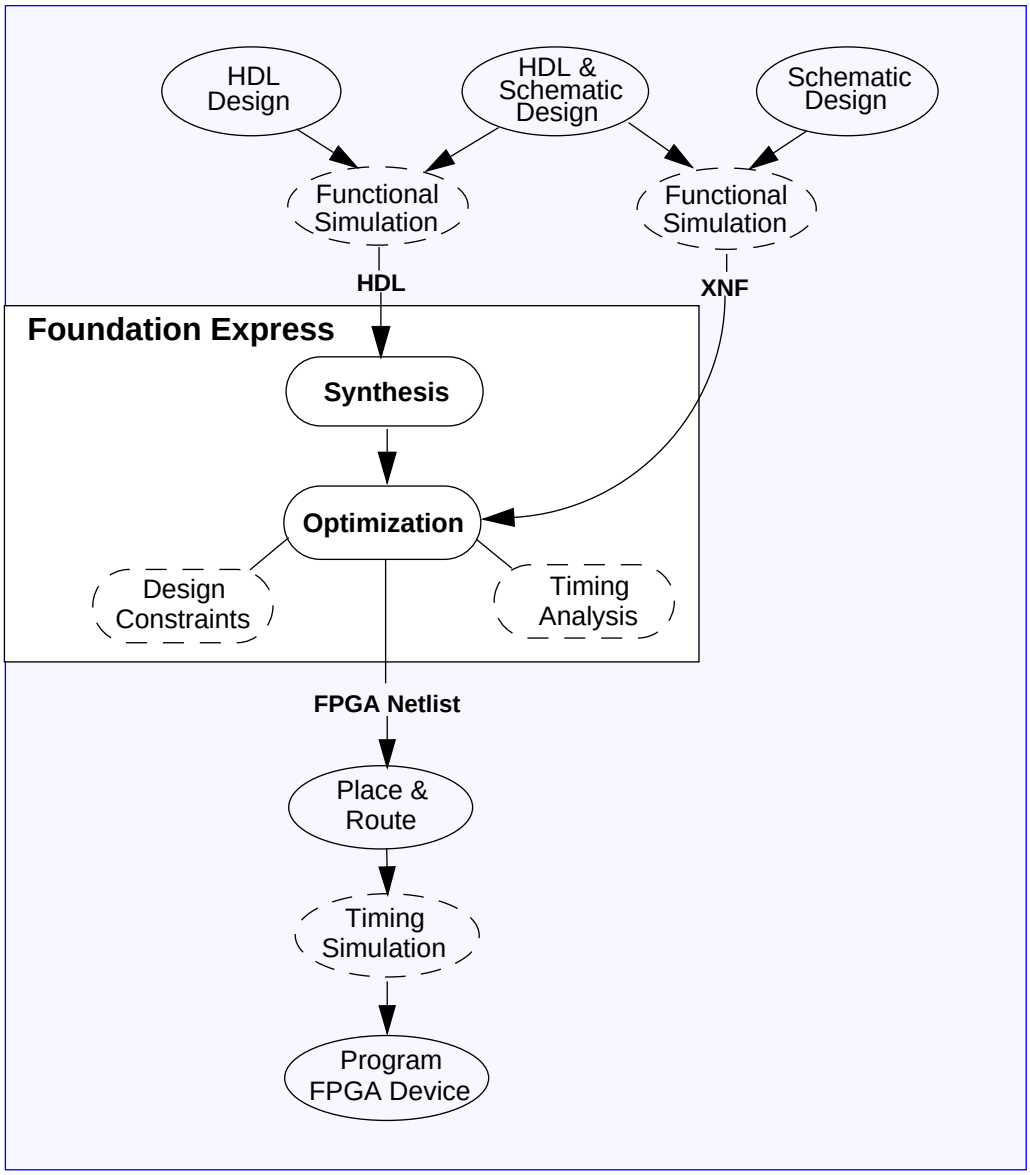

Figure 1-3 Different Design Environments

This is the procedure for using Foundation Express in your design environment:

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1. Create the design.
   - For an HDL-based design methodology, write the HDL source code for the design. Foundation Express processes the HDL code to produce an optimized netlist that is ready for FPGA / CPLD place and route tools.
   - For a schematic-based methodology, capture the design schematics.
   - For a mixed (HDL and schematic) design methodology, write the HDL source code for the parts of the design you have decided should be described in HDL. Capture the schematics for the rest of the design.
2. (Optional) Verify the design functionality. For HDL code, use an HDL simulator. For schematics, use a gate-level simulator.
3. In Foundation Express, set up the design and analyze the source files.
4. In Foundation Express, select the target device and optionally enter design constraints.
5. In Foundation Express, synthesize and optimize the HDL source code to produce an optimized FPGA netlist.
6. (Optional) In Foundation Express, analyze timing information to verify acceptable circuit performance.
7. Place and route the design with the FPGA vendor's development system.
8. (Optional) Simulate the design with back-annotated timing delays.
9. Program the FPGA / CPLD device.

Finding Help and Information

For information about procedures and dialog boxes in Foundation Express, see the online help system, this book, and the Xilinx or Synopsys WorldWide Web sites.

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Online Help System

The online help system is the most complete source of information about Foundation Express. You can find the answer to almost any question about Foundation Express using the online help system and documentation. For more information about the online help, see Chapter 3, “Tutorial.”

Tool Bar and Tip Bar

The tool bar and tip bar guide you through the design flow. The tool bar contains icons representing each step in the design flow. Clicking all the buttons from left to right automatically takes you through the entire design flow—from project creation to netlist generation.

The tip bar provides information at each stage of the design flow. It automatically detects the state of the design and identifies the next logical step in design flow. The tip bar also provides a brief explanation of the function and purpose of each step.

The “Tool Bar and Tip Bar” figure shows the tool bar and tip bar.

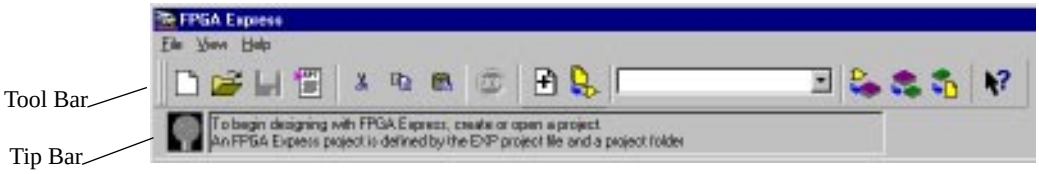

Figure 1-4 Tool Bar and Tip Bar

Context-Sensitive Help

For a brief description of a specific feature of Foundation Express, use the context-sensitive help. Click the question mark button on the tool bar or press Shift-F1, then click the item.

Detailed Online Help

For more detailed information, choose the Help Topics item from the Help menu. You can access specific help topics through a table of contents, an alphabetical index, or a text search.

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Output Window Information

A separate window displays errors, warnings, and messages about each action you perform in Foundation Express.

Contacting Xilinx

For your convenience, Xilinx provides several points of contact regarding Foundation Express.

- E-Mail Support

  Send e-mail to the Xilinx Hotline at

  hotline@xilinx.com

- Telephone Support

  Call Xilinx (United States and Canada) at

  1-800-255-7778

  between the hours of 6:30 a.m. and 5:00 p.m. PST.

- Automated Assistance

  Find answers to your technical questions or enter a support call on the World Wide Web at

  http://www.xilinx.com

HDL Reference Manuals from Xilinx

Online reference manuals for VHDL and Verilog HDL contain complete language descriptions and their application to Foundation Express synthesis and optimization. You can find the HDL reference manuals at **`START`** → **`Xilinx Foundation Series`** →.

Contacting Synopsys

As a Foundation Express customer, you have access to the Synopsys World Wide Web site at

http://www.synopsys.com

The Synopsys Web site offers technical and general information, including:

- Synopsys product descriptions and announcements

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- Descriptions of Synopsys training and support services
- SOLV-IT! on the Web, an interactive interface to SOLV-IT!, the Synopsys electronic knowledge base

  SOLV-IT! on the Web, offers you the latest technical information, including datasheets and documentation, answers to frequently asked questions, defects and workarounds, and system administration information. It is the most up-to-date source of information available.

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Chapter 2

Installation and Security

This chapter describes how to install and set up security for the Foundation Express software.

To use the Foundation Express software, you must set up the Xilinx security software. This security system must be set up on networked installations or standalone installations. After completing installation, refer to the "Setting Up Security for Foundation Express" section later in this chapter for details.

System Requirements

Following are the minimum system requirements for the Foundation Express Release.

Type of PC:

IBM®-compatible Pentium® class-machine recommended. Suggested 120 MHz clock speed, 2 GB disk space

Operating System: Windows 95 or Windows NT 4.0 (with Service Pack 2 installed)

System Memory (RAM) and Swap Space:

While the following table indicates the system requirements for typical designs, the unique characteristics of each individual design will affect the actual system resources required. Using memory, processor and disk monitoring utilities provide designers with an understanding of the exact system resources being utilized during each phase of the design cycle. The operating system adds additional memory overhead, as do any active applications. Some designs can be implemented using less than the specified memory while other complicated or large designs may require additional memory.

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It is recommended that each designer monitor the system resources being utilized and adjust these resources if necessary.

Table 2-1

Xilinx Device	RAM	Virtual Memory
XC4003E/L through XC4008E/L XC4005XL through XC4008XL XC9500 (small devices)	32 MB	32 MB-64 MB
XC4010E/L through XC4025E/L XC4028EX through XC4036EX XC4010XL through XC4028XL XC9500 (medium devices)	64 MB	64 MB-128 MB
XC4036XL through XC4062XL XC9500 (large devices)	128 MB	128 MB -256 MB

Note: When virtual memory is running out, the following message displays:

```
System Process - Out of Virtual memory. Your system is
running low on virtual memory. Please Close some
applications. You can then start the system option in
the Control Panel and choose the Virtual Memory button
to create an additional paging file or to increase the
size of your current paging file.
```

If you are using Windows NT 4.0, you must have Administrator permissions to alter the paging file.

Hardware and software requirements for installing Foundation Release software are:

Required Disk Space For Foundation Express CD: up to 26 MB

Typical— 25.3 MB
Compact — ~ 18MB
Custom
Program Files— 9.55 MB
Common Library Files— 6.89 MB
Sample Files— 1.73 MB
Help files— 5.46 MB
Xilinx Macros— 1.23 MB

Required Disk Space For Esperan 2.0 Tutorial: ~3 MB

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Directory Permissions:

Write permissions must exist for all directories containing design files to be edited.

Monitor:

SVGA 17” monitor

Mouse:

2-button (Microsoft Windows compatible) or 3-button (Microsoft Windows compatible). On a 3-button mouse, the middle button is not used.

CD-ROM Drive:

4x CD-ROM drive needed if installing the Foundation Release software from CD-ROM.

Ports:

Two ports (one for a pointing device and one parallel port for the parallel download cable, if needed). You can share the parallel port used for the parallel download cable.

Network Compatibility:

The Xilinx installation program supports TCP-IP networks.

Installing Foundation Express

This section explains how to install Foundation Express software on a Windows NT 4.0 and Windows 95.

During installation, changes are made to the System Registry in Windows 95/NT. For Windows 95, these variables are set up in the autoexec.bat file.

Note: If you have a dual boot system (that is, you can boot either Windows 95 or Windows NT), registry changes are made only for the Window system from which you are installing the Xilinx software.

No items are uninstalled when installing software.

When installing Foundation Express software on a Windows NT system, if you want all users to have the Foundation Express software, you must have System Administrator permissions when you install the software.

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1. Ensure that your system meets the requirements described in the System Requirements sections of the Foundation Series Installation Instructions.
2. Insert the Foundation Express CD into your CD-ROM drive. Determine the CD-ROM drive letter, *drive* (for example, D:). Select **`Start`** → **`Run`**. Type *drive*`: setup.exe` in the Open field of the Run window and click OK.
3. Follow the instructions in each of the windows.

Some basic information that you need to install the software is described in the following subsections.

Serial Number

Your serial number is printed in the lower right hand corner of the barcode label attached to the outside of the shipping package. The serial number is also printed on the registration card in your package.

Typical Installation

This option installs the most common configuration of files. This configuration includes sample files, help files, and macro files.

Compact Installation

This option installs only the program files and the common library files.

Custom Installation

Select this option if you want to specify which components of the software are installed. If you do not want a software component installed, you must deselect it from the Select Components window.

Other Considerations

The LM_LICENSE_FILE environment variable is used by the FLEXlm 5.12 software to enable the various components of the Foundation Express. If you are not currently running FLEXlm software, the installation program will define the variable to be C:\FNDTN\DATA\license.dat.

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If your PC already has the LM_LICENSE_FILE variable defined, the installation program will not modify the variable. After completing installation, you need to read the "Setting Up Security for Foundation Express" section.

Uninstalling Xilinx Software

To uninstall Xilinx software, perform the following steps.

1. Double-click the My Computer icon.
2. Double-click the Control Panel icon.
3. Double-click the Add/Remove Programs icon.
4. Ensure that the Install/Uninstall tab is selected in the Add/Remove Program Properties window.
5. From the list, select Foundation Express.

Setting Up Security for Foundation Express

This section explains how to set up security for the Design Implementation Tools and the Foundation Express tool. Security for the Foundation Express and Foundation design implementation tools is initiated using FLEXlm™ 5.12 license manager. (In the past, FLEXlm was known as the Highland License Manager.) For more information about FLEXlm, see the website, http://www.globetrotter.com.

This chapter explains how to set up FLEXlm on your PC.

To implement Xilinx security, you can use either of these types of licensing methods:

- Node-locked licenses—Xilinx supports node-locked on PCs only. It allows unlimited use of the product on a single PC. Access to the software is controlled by the settings in a licensing file. Node-locked licensing is the default PC licensing method.
- Floating licenses—Allows multiple PCs on a network to access the Foundation design implementation software. Any computer on the network can use the software, up to a limit which is set in a licensing file.

  Floating license security is implemented using a license manager daemon called lmgrd running on a server in conjunction with a Xilinx-specific license daemon called xilinxd.

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The following sections describe how to set up these two licensing systems.

- If have Foundation 1.3 software installed, proceed to the "Upgrading an Existing FND-STV or FND-BSV License File" section.
- If you are a new customer, proceed to the "Licensing for New Customers" section.

Upgrading an Existing FND-STV or FND-BSV License File

For customers who are upgrading from the Foundation Standard VHDL (FND-STV-PC) and Foundation Base VHDL (FND-BSV-PC) packages to Express, the following FLEXlm license file PACKAGE entries are provided. Users who wish to upgrade from F1.3 STV and BSV packages to F1.4 Express packages should replace the existing license file PACKAGE entry with those provided below. These PACKAGE upgrades will only work with existing valid INCREMENT lines for either FND-BSV-PC or FND-STV-PC.

1. Locate the existing FLEXlm license file (the typical location of this file is C:\FLEXLM\license.dat).
2. Copy the appropriate upgrade (Base V or Standard V) PACKAGE definition from below into the license.dat file. You can find these definitions in the pkgver.txt file located in the \fndtn directory. These definitions are shown in Figures 2-1 and 2-2 also.

```
#--- PACKAGE definition for FND-BSV-PC upgrade to Base Express -------
#
# This PACKAGE definition redefines a license for FND-BSV-PC to
# to support the FND-BSX-PC product. It will only work with
# a valid INCREMENT line for FND-BSV-PC.
#
# To update an existing FND-BSV-PC license, replace the existing
# PACKAGE definition with the following PACKAGE definition
#
PACKAGE FND-BSV-PC xilinxd 1.000 C0000031F4381921A984 \
COMPONENTS="system-PC bit-PC \
        xc3000D-PC xc4000E-PC xc5200E-PC \
        ngd2vhdl-PC verilog-PC \
        Foundation-PC X-VHDL-PC \
        FPGA-Express:1997.110 \
```

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```
        FPGA-Express-VHDL-Base:1997.110 \
        FPGA-Express-VLOG-Base:1997.110 \
        FPGA-Express-XC3k-Optimizer:1997.110 \
        FPGA-Express-XC4k-Optimizer:1997.110 \
        FPGA-Express-XC5k-Optimizer:1997.110 \
        FPGA-Express-XC9k-Optimizer:1997.110
#
#---------- End of FND-BSV-PC upgrade PACKAGE definition -------------
```

Figure 2-1 Base V Package Definition

```
#-- PACKAGE definition for FND-STV-PC upgrade to Foundation Express --
#
#-----------------------------------------------------------------------
#
# This PACKAGE definition redefines a license for FND-STV-PC to
# to support the FND-EXP-PC product. It will only work with
# a valid INCREMENT line for FND-STV-PC.
#
# To update an existing FND-STV-PC license, replace the existing
# PACKAGE definition with the following PACKAGE definition
#
PACKAGE FND-STV-PC xilinxd 1.000 A0C0B031665095562C90 \
        COMPONENTS="system-PC bit-PC \
        xc3000D-PC xc4000X-PC xc5200X-PC \
        ngd2vhdl-PC verilog-PC \
        Foundation-PC X-VHDL-PC \
        FPGA-Express:1997.110 \
        FPGA-Express-VHDL-Base:1997.110 \
        FPGA-Express-VLOG-Base:1997.110 \
        FPGA-Express-XC3k-Optimizer:1997.110 \
        FPGA-Express-XC4k-Optimizer:1997.110 \
        FPGA-Express-XC5k-Optimizer:1997.110 \
        FPGA-Express-XC9k-Optimizer:1997.110 \
        FPGA-Express-Constraint-Mgr:1997.110 "
#
#---------- End of FND-STV-PC upgrade PACKAGE definition -------------
```

Figure 2-2 Standard V Package Definition

3. Comment out the old PACKAGE definition by using a number sign (#) in the first column of the file.

The following represents an example license.dat file which has been upgraded from FND-STV-PC to FND-EXP-PC:

```
#------ Begin c:\flexlm\license.dat Example ---------
#
# This is a comment line
#
#-------------------------------------------------
#
# This license is nodelocked to laptop, HOSTID=00A024A9EA43
#
INCREMENT FND-STV-PC xilinxd 1.000 1-jan-0 0 2CD307B166DE8021473E \
        "XSJ_davet" 00a024a9ea43
#
#-------------------------------------------------
#
##
#PACKAGE FND-STV-PC xilinxd 1.000 809090A1DB4A34918DB2 \
#       COMPONENTS="system-PC bit-PC \
#       xc3000D-PC xc4000X-PC xc5200X-PC \
#       ngd2vhdl-PC verilog-PC \
#       Foundation-PC X-VHDL-PC "

PACKAGE FND-STV-PC xilinxd 1.000 A0C0B031665095562C90 \

        COMPONENTS="system-PC bit-PC \
        xc3000D-PC xc4000X-PC xc5200X-PC \
        ngd2vhdl-PC verilog-PC \
        Foundation-PC X-VHDL-PC \
        FPGA-Express:1997.110 \
        FPGA-Express-VHDL-Base:1997.110 \
        FPGA-Express-VLOG-Base:1997.110 \
        FPGA-Express-XC3k-Optimizer:1997.110 \
        FPGA-Express-XC4k-Optimizer:1997.110 \
        FPGA-Express-XC5k-Optimizer:1997.110 \
        FPGA-Express-XC9k-Optimizer:1997.110 \
        FPGA-Express-Constraint-Mgr:1997.110 "

#

#-------- End c:\flexlm\license.dat example ----------
```

Figure 2-3 Upgraded FND-STV License File

Licensing for New Customers

When you install the Foundation Express software, a temporary license file (license.dat) is copied to c:\FNDTN\DATA on your system. This Xilinx temporary license file expires on 01/01/99. In

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addition, if your LM_LICENSE_FILE file variable was not previously set, is automatically set to point to this temporary license file.

This temporary license allows you to begin using the Xilinx implementation tools immediately. The temporary license has two limitations:

- The license allows design of only Base components.
- No bitstreams can be created for downloading.

As a new customer, you need to obtain the FND-EXP or FND-BSX license. To obtain a permanent license, proceed as follows:

- For a node-locked license, see the "Obtaining Authorization Codes" section.
- For a floating license, see the "Preparing the License.dat File" section.

Setting Up Security Using Node-Locked Licenses

A node-locked license allows unlimited use of the product on a single PC. To set up security using node-locked licenses, you must:

1. Set up an LM_LICENSE_FILE environment variable pointing to the license.dat file.
2. Obtain license codes from Xilinx.
3. Set up a license file as specified by the LM_LICENSE_FILE variable and place the license codes into this file. If you are a current user of FLEXlm 5.12 of Xilinx software, you can add the Xilinx license codes to the existing license file.

The following sections describe how to perform each of these steps.

Setting Up the LM_LICENSE_FILE Variable

The LM_LICENSE_FILE environment variable points to the FLEXlm license file (typically license.dat).

If you already had an LM_LICENSE_FILE variable defined when you ran the Foundation installation, the installation program will not modify the variable. To allow Foundation Express to access the temporary license file, the LM_LICENSE_FILE variable must be set to point to the temporary license file as shown below.

Note: Make sure that you do not have the LM_LICENSE_FILE variable set in both the System Variables area and the User Variables area.

If you were instructed to set the LM_LICENSE_FILE variable after the Foundation installation, set it up as follows:

Windows NT 4.0

1. From the Start Menu, Select the Settings folder and click on the Control Panel icon.
2. In the Control Panel, double click the System icon.
3. Select the Environment tab from the System Properties window.
4. In the Variable field, type LM_LICENSE_FILE.
5. In the Value field, type in the drive letter or network letter and full path of the license.dat file. For example, for the temporary license.dat file on the C drive located in \FNDTN\DATA, you would type the following;

   `c:\FNDTN\DATA\license.dat`

Note: If you are already running FLEXlm security as part of another vendor's software, you can set up the LM_LICENSE_FILE variable to point to the Xilinx license.dat file and the vendor's license file. You can specify multiple license files in the LM_LICENSE_FILE Value and separate each with a semicolon (;), as in the following example.

```
c:\other_vendor\license.dat; c:\FNDTN\DATA\license.dat
```

6. Select Set and Apply to set the variable.
7. Select OK.
8. To verify that you set the variable, select **`Start`** → **`Programs`** → **`Command Prompt`**. In the Command Prompt window, enter the following command:

   `echo %LM_LICENSE_FILE%`

   The full path that you set as the value of the variable should display.

Note: If you do not set the LM_LICENSE_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the

LM_LICENSE_FILE environment variable must be set as described previously.

Note: Make sure you do not have an LM_LICENSE_FILE variable set in the System Variables area and another one set in the User Variables area; the variable must be set in one area only.

Windows 95

1. Add the following line to your autoexec.bat file.

   `set LM_LICENSE_FILE=c:\FNDTN\DATA\license.dat`

Note: If you are already running FLEXlm security as part of another vendor's software, you can set up the LM_LICENSE_FILE variable to point to the Xilinx license.dat file and the vendor's license file. You can specify multiple license files in the LM_LICENSE_FILE Value and separate each with a semicolon (;), as in the following example.

`set LM_LICENSE_FILE=c:\`*`other_vendor`*`\license.dat; c:\FNDTN\DATA\license.dat`

2. Reboot your system so that the autoexec.bat file is reread. Otherwise, the change has no effect.
3. To verify that you set the variable, select **`Start`** → **`Programs`** → **`MS-DOS Prompt`**. In the DOS window, enter the following command:

   `echo %LM_LICENSE_FILE%`

   The full path that you set as the value of the variable should display.

Note: If you do not set the LM_LICENSE_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the LM_LICENSE_FILE environment variable must be set as described previously.

Obtaining Authorization Codes

You must obtain permanent authorization codes to operate the Foundation software. You write these codes into your license.dat file.

Be prepared to supply Xilinx Customer Service the product name and serial number, the Ethernet address or C drive serial number, your end-user ID number, and the network name of your PC.

For existing customers, the end-user ID number is located on the shipping box label (example 1234-01-01-A). New customers will receive their end-user ID after registering the product.

- The product name and serial number are located in the lower right hand corner of the barcode label located on the package or on the registration card inside the package.
- You can obtain the Ethernet address by logging onto the PC and running the lmtools.exe application located in C:\FNDTN\SYNTH\bin-win-32. When the lmtools window appears, click on Hostid.

  You can obtain the C: drive Volume Serial Number for your PC by logging onto the PC, accessing a Command Prompt, and entering the following command at the C: prompt:

  ```
  vol C:
  ```

  Xilinx strongly recommends that you use the Ethernet address instead of the C: drive serial number.
- To obtain the network name of your PC, proceed as follows:

  a) From the Start Menu, select the Settings folder and click on the Control Panel icon.

  b) In the Control Panel, double click the Network icon.

  c) Select the Identification tab to see the Computer name. This is the network name required for the license.
- Contact Xilinx Customer Service in any of the following ways:
  - Call Xilinx Customer Service to obtain the authorization codes. International customers may also contact their local distributor or sales representative.

    US and Canada 1-800-624-4782
    (Monday through Friday, from 8:00 a.m. to 5:00 p.m. Pacific Time)

    United Kingdom 01932-333550

    Belgium 0800-73738

    France 0800-918333

    Germany 0130-816027

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Italy	1677-90403
Netherlands	0800-918333
Other European Countries	(44) 1932-333550
Japan	81-3-3297-9153

Southeast Asia/ROW and international countries not listed: Contact your local Xilinx distributor

- Complete the M1 License Request Form enclosed in your package and FAX to:

United States and Canada	408-559-0115
United Kingdom	01932-828521
Other European Countries	(44) 1932-828521
Japan	81-3-3297-9189

Southeast Asia/ROW and international countries not listed: Contact your local Xilinx distributor

- Obtain authorization codes from the World Wide Web. Go to the Xilinx home page (http://www.xilinx.com), click on the Support hyperlink and then click on the Software Licensing and Registration hyperlink.
- If you are a European customer, you may provide the required information via email to m1license@xilinx.com

Your Xilinx Customer Service Representative will email or fax you a file with your authorization codes.

Setting Up the license.dat File

The file your Xilinx Customer Service Representative will email or fax to you includes information similar to the following file.

License Information With Ethernet Address

```
#----------------------------------------
#
# This license is nodelocked and uncounted.
# It does NOT require or SUPPORT running lmgrd.
#
# Set the LM_LICENSE_FILE variable to point to this
# license file; like:
```

```
#
# setenv LM_LICENSE_FILE /usr/xilinx/data/license.dat
# or
# set    LM_LICENSE_FILE=C:\xilinx\data\license.dat
#
#-------------------------------------------------
#
# This license is nodelocked to togo,
HOSTID=DISK_SERIAL_NUM=C102011D5
#
INCREMENT FND-EXP-PC xilinxd 1.000 1-jan-0 0 FC93B64832A8A3DE4DAB \
"XSJ_davet" DISK_SERIAL_NUM=C102011D5
#
#-------------------------------------------------
#
PACKAGE FND-EXP-PC xilinxd 1.000 30A0C0B1948681FADED8
  COMPONENTS="system-PC bit-PC \
  xc3000D-PC xc4000X-PC xc5200X-PC \
  ngd2vhdl-PC verilog-PC \
  Foundation-PC X-VHDL-PC \
  FPGA-Express:1997.110 \
  FPGA-Express-VHDL-Base:1997.110 \
  FPGA-Express-VLOG-Base:1997.110 \
  FPGA-Express-XC3k-Optimizer:1997.110 \
  FPGA-Express-XC4k-Optimizer:1997.110 \
  FPGA-Express-XC5k-Optimizer:1997.110 \
  FPGA-Express-XC9k-Optimizer:1997.110 \
  FPGA-Express-Constraint-Mgr:1997.110
#
#-----------------------------------------------------------------

# License checksum:
#
#      82: INCREMENT FND-EXP-PC xilinxd 1.000 1-jan-0 0
FC93B64832A8A3DE4DAB  "XSJ_davet" DISK_SERIAL_NUM=C102011D5
#
#    (From lmutil lmcksum -c <license file>)
#
#---------------------------------------+
```

If you supply a disk drive serial number, the INCREMENT line will have the text “DISK_SERIAL_NUM”. For the previous sample file, the INCREMENT line looks like the following:

```
INCREMENT FND-EXP-PC xilinxd 1.000 1-jan-0 0 FC93B64832A8A3DE4DAB \
"XSJ_davet" DISK_SERIAL_NUM=C102011D5
```

This information in this file must appear in your license.dat file.

Xilinx strongly recommends that you use the Ethernet address as your host id instead of the C: drive serial number.

You can use the information you receive in these ways:

Note: Your temporary license is located in C:\FNDTN\DATA, but Xilinx recommends not placing your permanent license file in this directory. Instead, place your permanent license file in the directory that will not be overwritten by any reinstallation of the Foundation Series software (for example C:\FLEXLM). You may have to create the directory C:\jFLEXLM to place the license file in this location.

Wherever you place your permanent license.dat file, you must ensure that the LM_LICENSE_FILE variable points to the location of this file. Refer to the "Setting Up the LM_LICENSE_FILE Variable" section.

- If the Customer Service Representative sent the information by email, you can remove the email header from the file and copy the file to the correct location.
- If the Customer Service Representative sent the information in a fax, you can use a text editor to create a file containing the information and place the file in the correct location.

  The default license file contains PACKAGE definitions for all the base packages Xilinx supports (devices with 10,000 or fewer gates). Most will not be relevant to your installation, but they may be left in the license file. You *must* include a package definition which corresponds to any products mentioned in `INCREMENT` lines. For example, the `PACKAGE FND-STV-PC` line in the sample file, License Information With Ethernet Address, must be matched by an INCREMENT `FND-STV-PC` line.

  Each `INCREMENT` line must be a single line. If the text overflows to another line, use the backslash character as a continuation character at the end of the line.

  If you use the backslash, make sure that it is the last character on the line. No tabs or spaces may follow the backslash.
- If you are adding the information to an existing license.dat file, place the new Xilinx information *before* any existing information pertaining to floating licensing. This information usually begins with a SERVER line.

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When the license.dat file contains the proper information and is in the proper directory, you can run the Foundation software.

Setting Up Security Using Floating Licenses

This section describes how to implement security using floating licenses. Floating licenses allows multiple systems on a network to access the Foundation software. Any systems on the network can use the software, up to a limit which is set in a licensing file called license.dat. The temporary license file supplied during install is not a floating license file. See the "Setting Up Security Using Node-Locked Licenses" section for information on how to set up the temporary license file.

Please note that this release includes FLEXlm version 5.12. If you are running an older version, including the FLEXlm version 4.1 which was included in the earlier releases, you must restart your license manager and daemon using the new FLEXlm version 5.12 software.

Selecting a License.dat File

If you do not already have a license.dat file, contact Xilinx Customer Service to obtain a license.dat file. Refer to the "Preparing the License.dat File" section for information about contacting Customer Service.

If you are a current user of FLEXlm 5.12 of Xilinx software, then your current license will work with this new software, and you do not have to change it. However, you may need to stop the license daemon and restart it.

If you are running in a networked environment, the license.dat file should be copied to a flexlm directory on one of the servers accessible by your PC. Multiple users can then use the same copy of the license manager.

Setting Up the LM_LICENSE_FILE Variable

The LM_LICENSE_FILE environment variable points to the FLEXlm licensing file, named license.dat. You can set this variable when you install the Foundation software. The default (and recommended) LM_LICENSE_FILE setting is C:\FNDTN\DATA\license.dat.

If you already had an LM_LICENSE_FILE variable defined when you ran the Foundation installation, the installation program will not modify the variable.

If you were instructed to set the LM_LICENSE_FILE variable after the Foundation installation, set it up as follows:

Windows NT 4.0

1. From the Start Menu, Select the Settings folder and click on the Control Panel icon.
2. In the Control Panel, double click the System icon.
3. Select the Environment tab from the System Properties window.
4. In the Variable field, type LM_LICENSE_FILE.
5. In the Value field, type in the drive letter or network letter and full path of the license.dat file. For example, for a license.dat file on the C drive located in \FLEXLM, you would type the following.

   `c:\FLEXLM\license.dat`

Note: If you are already running FLEXlm security as part of another vendor's software, you can set up the LM_LICENSE_FILE variable to point to the Xilinx license.dat file and the vendor's license file. You can specify multiple license files in the LM_LICENSE_FILE Value and separate each with a semicolon (;), as in the following example.

   `c:\`*`other_vendor`*`\license.dat;c:\FLEXLM\license.dat`

6. Select Set to set the variable.
7. Select OK.
8. Log out and log in again to insure that the current value of the environment variable LM_LICENSE_FILE is being used.
9. To verify that you set the variable, select **Start** → **Programs** → **Command Prompt**. In the Command Prompt window, enter the following command:

   `echo %LM_LICENSE_FILE%`

   The full path that you set as the value of the variable should display.

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Note: If you do not set the LM_LICENSE_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the LM_LICENSE_FILE environment variable must be set as described previously.

Windows 95

1. Add the following line to your autoexec.bat file.

   `set LM_LICENSE_FILE=c:\FLEXLM\license.dat`

Note: If you are already running FLEXlm security as part of another vendor's software, you can set up the LM_LICENSE_FILE variable to point to the Xilinx license.dat file and the vendor's license file. You can specify multiple license files in the LM_LICENSE_FILE Value and separate each with a semicolon (;), as in the following example.

`set LM_LICENSE_FILE=c:\`*other_vendor*`\license.dat; c:\FLEXLM\license.dat`

2. Reboot your system so that the autoexec.bat file is reread. Otherwise, the change has no effect.
3. To verify that you set the variable, select **`Start`** → **`Programs`** → **`MS-DOS Prompt`**. In the DOS window, enter the following command:

   `echo %LM_LICENSE_FILE%`

   The full path that you set as the value of the variable should display.

Note: If you do not set the LM_LICENSE_FILE variable, FLEXlm looks for the license.dat file in the default location, which is c:\flexlm\license.dat. If the file cannot be found in that location, the LM_LICENSE_FILE environment variable must be set as described previously.

License Management

You will need to contact your Xilinx customer support to obtain authorization codes for your new Xilinx products.

To use the Xilinx software, you will need the following:

- FLEXlm license manager, Version 5.0 or greater
- Xilinx license.dat file

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- Appropriate authorization codes to add to license.dat

The FLEXlm license manager is included on the media shipped to you by Xilinx, and is copied with the software into your installation directory by the Install program.

You must obtain your template license.dat file from Xilinx customer support. For information about how to contact Customer Service, refer to the "Preparing the License.dat File" section.

Adding New Products

If you are installing for the first time or are adding new products to your Xilinx installation, you must call Xilinx to obtain the authorization codes for the components you have purchased. Refer to the "Preparing the License.dat File" section for information about contacting Customer Service.

To enable an installation, you must update the template license.dat with the authorization codes and start the license manager as described in the following sections.

If you plan to add the Xilinx license information to an existing license file, you must ensure that you obtained authorization codes for the same server as the existing license and then you must ensure that the license.dat file contains the new DAEMON and INCREMENT lines, and that this file includes the PACKAGE section for each INCREMENT line. Please note that this release requires a new vendor daemon, xilinxd.

Preparing the License.dat File

The license.dat file is commonly located in c:\flexlm. (This is the default for FLEXlm.) The template license file has PACKAGE definitions for the Xilinx products. You will need to add the INCREMENT lines containing your authorization codes. You will also need to modify the DAEMON line so that it contains the correct path to your copy of xilinxd.

To obtain your authorization codes:

Be prepared to supply Xilinx Customer Service the nine digit end-user ID number, product name and serial number, the Ethernet address or C drive serial number, and the network name of your PC.

For existing customers, the end-user ID number is located on the shipping box label (example 1234-01-01-A). New customers will receive their end-user ID after registering the product.

- The product name and serial number are located in the lower right hand corner of the barcode label located on the package or on the registration card inside the package.
- You can obtain the Ethernet address by logging onto the PC and running the lmtools.exe application located in C:\FNDTN\SYNTH\bin-win-32. When the lmtools window appears, click on Hostid.

  You can obtain the C: drive Volume Serial Number for your PC by logging onto the PC, accessing a Command Prompt, and entering the following command at the C: prompt:

  ```
  vol C:
  ```

  Xilinx strongly recommends that you use the Ethernet address instead of the C: drive serial number.
- To obtain the network name of your PC, proceed as follows:

  a) From the Start Menu, select the Settings folder and click on the Control Panel icon.

  b) In the Control Panel, double click the Network icon.

  c) Select the Identification tab to see the Computer name. This is the network name required for the license.

  If you plan to add the new Xilinx information to an existing license file, you should use the network name from the SERVER line(s) in the existing file. You *must* use the same information if you plan to use the same computer for your license server.
- Contact Xilinx Customer Service in any of the following ways:
  - Call Xilinx Customer Service to obtain the authorization codes. International customers may also contact their local distributor or sales representative.

    US and Canada 1-800-624-4782
    (Monday through Friday, from 8:00 a.m. to 5:00 p.m. Pacific Time)

    United Kingdom 01932-333550

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Belgium	0800-73738
France	0800-918333
Germany	0130-816027
Italy	1677-90403
Netherlands	0800-918333
Other European Countries	(44) 1932-333550
Japan	81-3-3297-9153

Southeast Asia/ROW and international countries not listed: Contact your local Xilinx distributor

- Complete the M1 License Request Form enclosed in your package and FAX to:

United States and Canada	408-559-0115
United Kingdom	01932-828521
Other European Countries	(44) 1932-828521
Japan	81-3-3297-9189

Southeast Asia/ROW and international countries not listed: Contact your local Xilinx distributor

- Obtain authorization codes from the World Wide Web. Go to the Xilinx home page (http://www.xilinx.com), click on the Support hyperlink and then click on the Software Licensing and Registration hyperlink.
- If you are a European customer, you may provide the required information via email to m1license@xilinx.com

Your Xilinx Customer Service Representative will email or fax you a file with your authorization codes.

Understanding License Codes

The file your Xilinx Customer Service Representative will email or fax to you includes information similar to the following.

```
SERVER  edapc89      DISK_SERIAL_NUM=C031946D 2200
DAEMON  xilinxd  C:\XILINX\BIN\NT\XILINXD.EXE
```

```
INCREMENT PR-4EX-PC xilinxd 1.000 28-MAY-97 1 0B242B17C9F07F15EA92
"XSJ_dan"
```

Note: You must use the full path name for the location in the DAEMON line. Also you cannot use variable names such as %XILINX% in your path description. The INCREMENT line must be a single line.
If the text overflows to another line, use the backslash character as a continuation character at the end of the line. If you use the backslash, make sure that it is the last character on the line. No tabs or spaces may follow the backslash.

You *must* retain the package definition which corresponds to any products mentioned in INCREMENT lines. For example, the INCREMENT above won't work without a package definition:

```
PACKAGE PR-4EX-PC xilinxd 1.000 0070A051667FD9D49EA8 \
     COMPONENTS="system-PC bit-PC xc3000D-PC xc4000X-PC \
     mentor-PC synopsys-PC viewlog-PC ngd2vhdl-PC verilog-PC " \
     OPTIONS=SUITE
```

Note: The previous four lines are actually a single line. The backslash (\) at the end of the first three lines is a continuation character indicating that each line wraps to the next line. If you use the backslash character, it must be the last character on the line, and no tabs or spaces may follow the backslash This package definition is only an example.

Starting the License Server

Once the license file has been updated, you must start (or restart) the license server. If you were not already running FLEXlm 5.0 or a higher version, you must use the new lmgrd, delivered with your Xilinx software. The command, **`lmgrd -v`**, will cause lmgrd to display its version number.

Note: The license server will not start automatically when you run the Xilinx software. You must start up the lmgrd daemon explicitly to allow the software to run.

Before starting a lmgrd (FLEXlm license manager), you must meet the following requirements.

- You must have a license file for a floating license.
- The DAEMON line in the license file must point to a valid path for the xilinxd daemon.

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You can run lmgrd from either a GUI window or from the DOS command line.

Using the GUI Window on Windows NT 4.0

To invoke the lmgrd from a GUI window:

1. Copy the following files from the CD-ROM into the Windows system32 directory:

   `copy flexlm.cpl` *system-drive*`:\winnt\system32`

   `copy lmgr325c.dll` *system-drive*`:\winnt\system32`

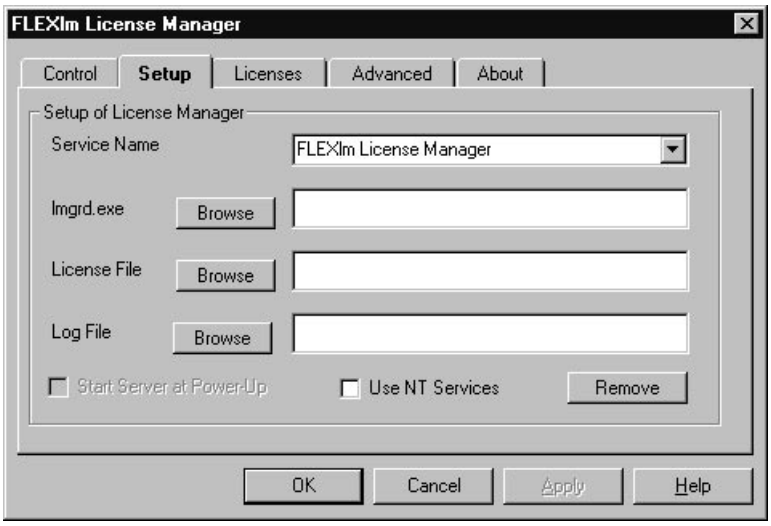
   The FLEXlm control panel, flexlm.cpl, is an applet that you install into the Windows NT Control Panel. You use it to control the execution of the FLEXlm license manager

   The library lmgr325c.dll is placed in the same directory as flexlm.cpl in this example, but it could be placed anywhere in the system search path.

Note: You can test FLEXlm by running lmgrd from a DOS prompt. This allows you to see diagnostic output and errors as they occur.

2. After placing flexlm.cpl into the system32 directory, open the Control Panel and launch the “Flexible License Manager”.

From the Control tab you can start, stop, and check the status of your license server. Select the Setup tab to enter information about your license server.



You can change the default service name of "FLEXlm License Manager" to something else. Fill out the rest of the form to configure lmgrd to serve licenses for your use.

3. The information you enter is stored in the registry under the service name you created:

`HKEY_LOCAL_MACHINE\SOFTWARE\FLEXlm License Manager\`*`Service-Name`*`\...`

Select the Control tab and press the Start button to turn on your license server. lmgrd.exe will be launched as a background application with the license file and log file locations passed as parameters.

4. If you want lmgrd.exe to start automatically, select the "Use NT Services" box. This will install lmgrd.exe as an NT service. You can then use the NT's Services control panel to adjust the start/stop behavior of lmgrd.exe.

   Because NT services do not have command line parameters, lmgrd.exe, when started as a service, locates its service name under "FLEXlm License Manager" in the registry. From there it recovers the license file and log file locations. Multiple instances of lmgrd.exe can be run as services as long as each has a different service name.

   You can switch back and forth between different instances of lmgrd.exe by going to the Setup tab and changing the selection in

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the Service Name field (this is only necessary if you have more than one product that is licensed with FLEXlm).

5. Use the remaining tabs in the control panel to perform functions similar to those available with the command line lmutil program. The Licenses tab provides information about the license file. The Advanced tab allows you to perform diagnostics and check versions.

Using the GUI Window on Windows 95

The procedure for using the FLEXlm control panel on Windows 95 is the same as for Windows NT 4.0, with the following exceptions:

1. Copy the following files from the CD-ROM into the Windows system32 directory:

   `copy flexlm.cpl` *system-drive*`:\windows\system`

   `copy lmgr325c.dll` *system-drive*`:\windows\system`

   Because services are not available on Windows 95, the "Use NT Services" check box is not available. Instead, a "Start Server at Power-Up" check box gives you the option to start the server when the system is booted.

   On Windows 95, FLEXlm uses a registry feature that launches programs automatically. The "Microsoft\Windows\CurrentVersion\RunServices" registry is used to launch the program lmgrd95.exe at power-on. This program scans the "FLEXlm License Manager" are of the registry and launches an instance of lmgrd.exe for each service name it finds.

Using the Command Line

To invoke the lmgrd from a command prompt:

1. Select **`Start`** → **`Programs`** → **`Command Prompt`**.
2. In the Command Prompt window, enter the following command:

   `lmgrd -app -c` *licensefile* **`-l`** *logfile*

   where *licensefile* is the actual name of your license file and *logfile* specifies the name you want for the log file. The log file stores information about checking out and checking in licenses.

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If a security error occurs, read the log file to determine the cause of the error.

Note: You must have the %XILINX%\bin\nt directory in your path, so that the license manager can find the required .DLL files.

If you attempt to close the Command Prompt window while lmgrd is running, the End Task windows will display. If you choose to terminate lmgrd, you will not be able to access the Xilinx software. You must be running lmgrd to use the Xilinx software.

Chapter 3

Tutorial

The fastest way to learn to use Foundation Express is to complete this tutorial, which follows the Foundation Express design flow. In this chapter, the tutorial explains how to do the following tasks.

1. Creating design source files
2. Setting up a project
3. Synthesizing a design
4. Entering design constraints
5. Optimizing the design logic
6. Analyzing timing
7. Generating an optimized FPGA netlist and reports

Using the Help System

The Foundation Express help system is always available when you need assistance. The help system is available in several forms including:

- Tool bar and tip bar
- Context-sensitive help
- Detailed Windows-style online help
- Output window information

Tool Bar and Tip Bar

In addition to standard Windows help features, Foundation Express includes the tool bar and tip bar. The tool bar is a group of icons that are logically arranged to represent the steps in the design flow.

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Clicking the sequence of buttons from left to right leads you through the entire design flow, from project creation to netlist generation.

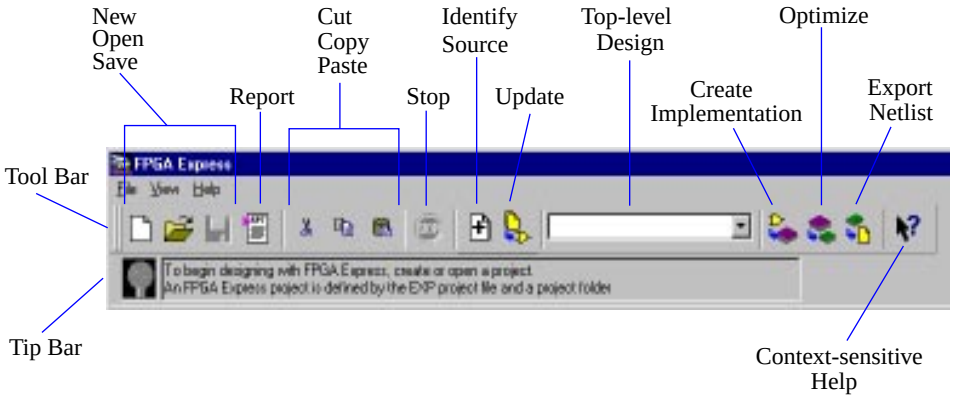

Figure 3-1 Using the Tool Bar and Tip Bar

The tip bar provides ideas and information at each stage of the design flow. The tip bar automatically detects the state of the active design and briefly describes the next logical step in the design flow, as well as the function and purpose of each step. For example, when you first run Foundation Express, the tip bar indicates that the first step is to create a design project.

To enable or disable the tool bar, use **`View`** → **`Toolbar`**.

Context-Sensitive Help

Context-sensitive help provides brief descriptions of specific commands and features in menus and dialog boxes.

To access context-sensitive help:

1. Select the ? button in the tool bar of any window or dialog box.
2. Choose an item in a menu, window, or dialog box.
3. Click the mouse button again to remove the help message.

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Detailed Windows-Style Help

Windows help features include detailed topical overviews, step-by-step instructions, and context-sensitive definitions. You can access detailed help through a table of contents, an index of topics, or a full-text search.

To access detailed help:

1. From the Help menu, click Help Topics.
2. Choose one of the three tabs (Contents, Index, or Find) to search for information.
   - *Contents* organizes help the way a reference book does, with broader subjects being the “chapters” of the “book.”
   - *Index* organizes the help alphabetically by topic.
   - *Find* lets you specify keywords or phrases to find the help on a particular topic.

Output Window Information

The output window automatically displays errors and warnings for each action you perform on a design source or chip. It also displays warnings and messages about selected chips. You can use the information in this window with the built-in HDL Editor for debugging.

Creating Design Source Files

The first step in the Foundation Express design flow is creating HDL source files. You can use any text editor to enter VHDL and Verilog HDL source code for your design. You generally perform this step outside of Foundation Express. However, you can also use the integrated Foundation Express HDL Editor (described later) to edit a design source file once it has been read into a project.

Setting Up a Project

The key components of a project are source files describing FPGA designs. Source file types are VHDL, Verilog HDL, or netlist. Netlist files usually originate from schematic capture systems or preoptimized macro libraries.

These are the steps in setting up a project in Foundation Express:

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1. Creating a project
2. Creating libraries of design source files
3. Analyzing and debugging source files

Creating a Project

After you prepare the design source files, start the Foundation Express design flow by creating a Foundation Express project. When you create a project, Foundation Express creates a new folder (directory) in which to store the project information.

To create a new project in Foundation Express:

1. Start Foundation Express from the Windows Start menu (**`Start`** → **`Programs`** → **`Xilinx Foundation Series`** → **`Foundation Express`**). This opens the Foundation Express main window.
2. When you start Foundation Express, you can open an existing project or create a new one. For now, create a new project by clicking in the New Project icon in the tool bar or by selecting New from the File menu.

   In the startup window, Foundation Express displays the Create New FPGA Express Project dialog box as shown in "Creating a New Project" figure.

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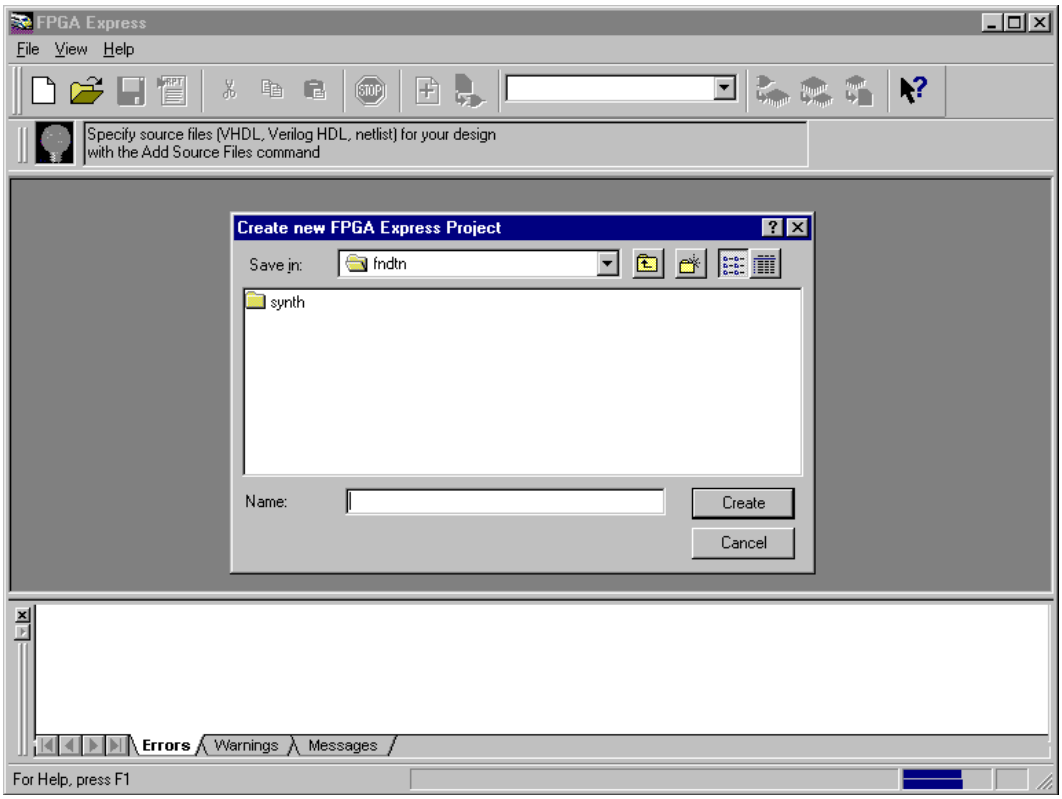

Figure 3-2 Creating a New Project

3. The “Create New FPGA Express Dialog Box” figure shows the Create New FPGA Express Project dialog box. In this dialog box, you can choose a location for the project. Use the drop-down list in the “Save in” field to navigate your directory tree. You can click the Create New Folder icon to create a new directory. Type the name **`tutorp`** for the project folder (directory) in the Name field. The `tutorp` directory is where project files will be stored. Click the Create button to create the new project. For this tutorial, push into the tutorial directory and crete the `tutorp` project. Then click cancel so you do not identify any source files.

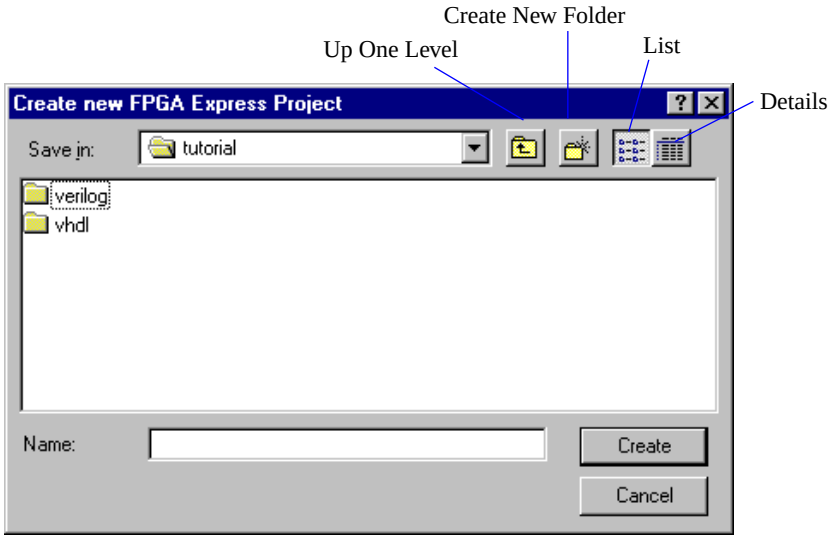

Figure 3-3 Create New FPGA Express Dialog Box

After it creates the tutorp project, Foundation Express displays the project window and extends the menu bar. The project window is divided into two windows: the Design Sources window and the Chips window. The Design Sources window displays the name, location, and status of the design's source files. The Chips window displays information for individual design implementations, such as name and device type. The project window title bar displays the name of the project. "The Design Sources and Chips Windows" figure shows these project windows.

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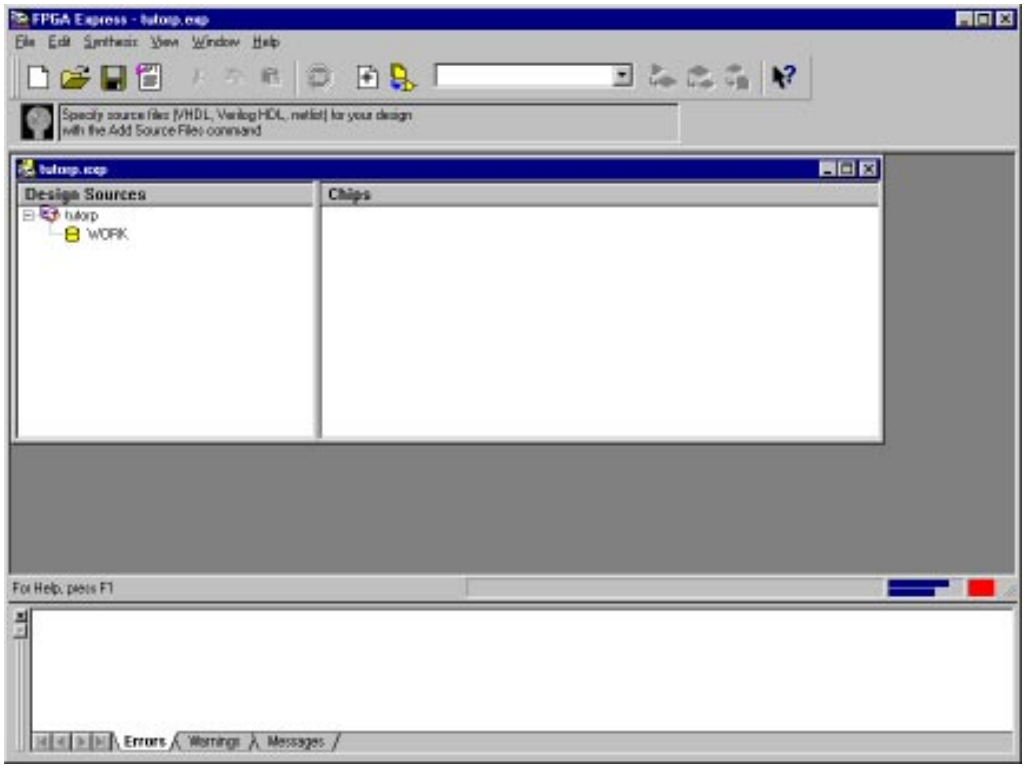

Figure 3-4 The Design Sources and Chips Windows

Creating Libraries of Design Source Files

After you create the project, the next step is to create libraries of design source files. Whenever you create a project, a default library named WORK is automatically put into the project folder.

Libraries contain design source files that you add (identify) to the library. Foundation Express source files can be any combination of VHDL, Verilog HDL, or FPGA netlist files. When you identify source files, Foundation Express automatically analyzes them for syntax errors, warnings, or any other information. If there are errors, you can find detailed explanations of the problems in the online help.

In VHDL environments, it is sometimes necessary to have multiple libraries. You can add a library at any time by clicking the right

mouse button in the Design Sources window and selecting New Library. Then you identify the design sources for that library in the same way you did for WORK. (In Verilog, there is no analogy to a library construct and therefore no advantage to creating new libraries.)

Note: Foundation Express does not copy design source files. When you identify these files, Foundation Express analyzes them in their current location. If you are required to make any changes to the files (indicated by a ? icon), you must click the Update icon in the tool bar or click the right mouse button in the Design Sources window and select Update File so that Foundation Express will reanalyze them and update the project.

To identify source files:

1. **Click Synthesis** → **Identify Sources** or click  in the tool bar. Foundation Express opens the Identify Sources dialog box. as shown in "Identify Sources Dialog Box" figure.

   Another way to reach the Identify Sources dialog box is to click your right mouse button in the Design Sources window and select Identify sources in WORK.

   You can also identify the Source Files immediately after you create the project folder.

2. Select source files from the Identify Sources dialog box. For this tutorial, use the tutor design files written in VHDL (tutor.vhd, counter.vhd) or Verilog (tutor.v, counter.v). These files are located in the **FNDTN** → **Synth** → **samples** → **tutorial** → **vhdl** or **verilog** directories.

   When you have selected your design sources, click Open.

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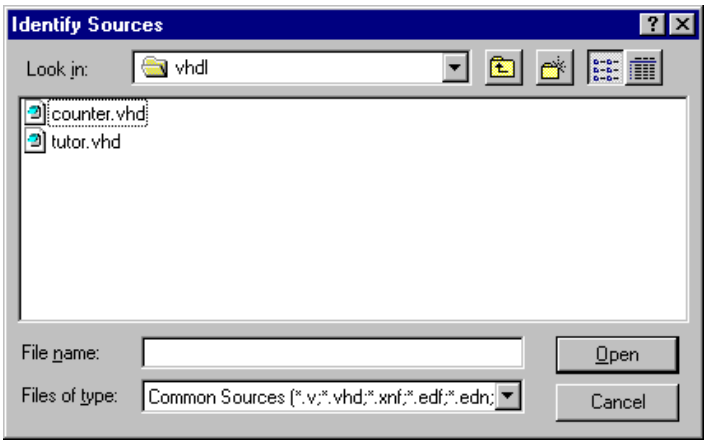

Figure 3-5 Identify Sources Dialog Box

Each source file is automatically analyzed as it appears in the project window. As shown in the "After Identifying Design Source Files" figure, the icon to the left of each file name indicates the results of the analysis. In this tutorial, the counter file has at least one error (indicated by the red cross) that must be corrected. The green check marks next to the other files indicate that the files have no errors or warnings. The error in the one source file is reflected up the hierarchy so that the library and the project icons are also marked with a red cross. See the online help for a list and explanation of each analysis status icon.

Notice that the output window at the bottom displays error messages about the selected source file.

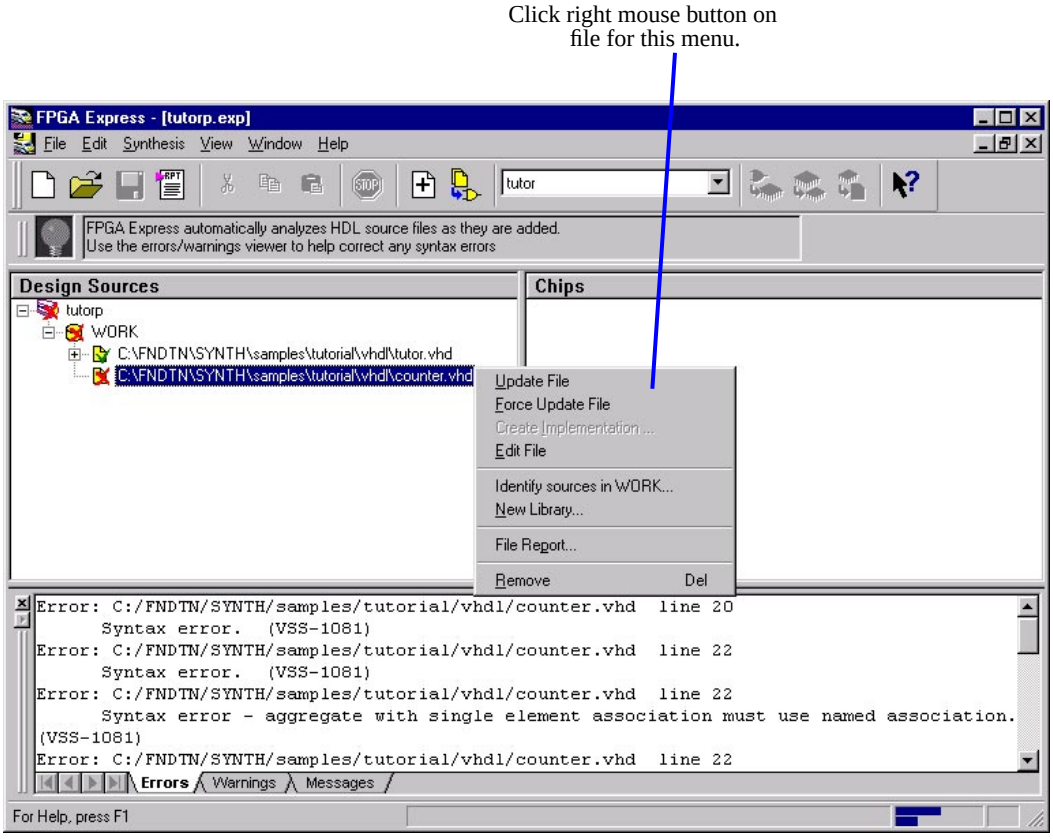

Figure 3-6 After Identifying Design Source Files

Analyzing and Debugging Source Files

To help find and correct errors and warnings in source files, use the error and warning pages in the Foundation Express output window. These pages show the file name, line number, and type of each error or warning. After viewing the messages, you can use the built-in HDL Editor to investigate and fix the source files.

To view and correct errors and warnings:

1. After selecting counter as the design source in the Design Sources window, view the errors in the output window. Read the error and warning messages.

2. Correct any errors in the design source file. There are two ways to open an HDL editor window directly to an error in a design source file:

   - To open a source file at the location of the *first* error, click the right mouse button in the Design Sources window and select Edit File.
   - To open a source file at the location of a *specific* error, double-click the text for that error in the output window. This method works only if there are multiple errors in the file.

If you selected the internal source editor (from the **`Synthesis`** → **`Options`** → **`General page`**), Foundation Express uses the built-in HDL Editor to edit the selected file. You can use the Foundation Express Edit menu to navigate in the text file. You can also use the HDL Editor menu that is displayed when you click your right mouse button in the HDL Editor window. If you did not select the internal source editor, clicking Edit File starts the editor you associated with the file type and opens it.

The "HDL Editor Window" figure shows the HDL Editor window and its menu of activities.

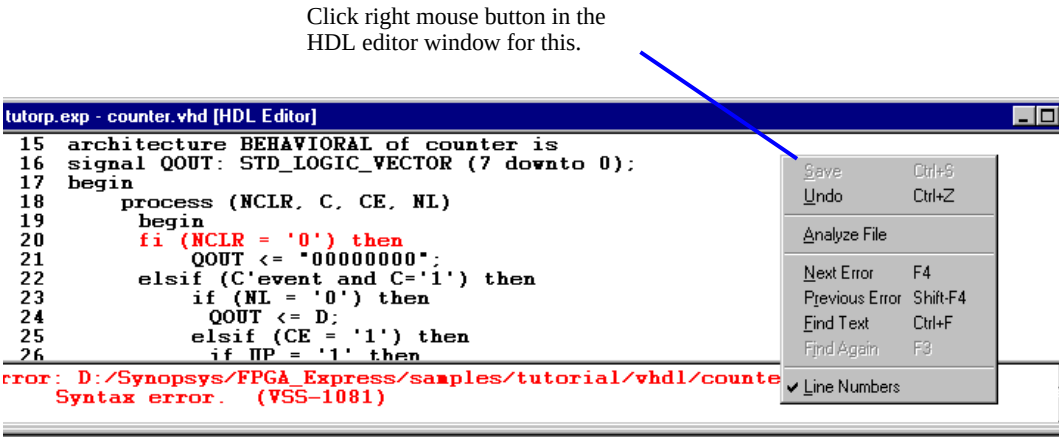

Figure 3-7 HDL Editor Window

The errors in the counter are caused by a typo in the if statement. Change the text from *fi* to *if* in the counter file. Save the file. The

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tutor.vhd icon contains a question mark, indicating that the file is out-of-date.

3. Update the file. Either return to the Design Sources window and click this icon on the tool bar or use Analyze File from the HDL Editor menu before closing the HDL Editor window.

   Based on the extent of your modifications, you can update a file, library, or the project. Foundation Express reanalyzes only the files that have been modified. If your changes are not evident to Foundation Express (if the changes are in a dependent file, for example), you can force an update with the Force Update File (Library or Project) command from the menu you get when you click the right mouse button in the Design Sources window.

After you finish identifying, analyzing, and debugging source files, you are ready to synthesize the design.

Synthesizing the Design

Foundation Express uses design configurations to specify a target device and design constraints, leading to optimized FPGA netlists. Each design configuration, together with the set of design files, determines a unique design implementation.

In this step, Foundation Express synthesizes a unique, unoptimized design implementation from your source files. It creates a generic, logical description of the design, then maps the description to a specific device technology. After you have completed this step, you can set design constraints and controls before optimizing.

These are the steps in synthesizing the design:

1. Identifying the top-level design
2. Specifying the target architecture
3. Setting the target clock frequency
4. Creating the design implementation

Identifying the Top-Level Design

To begin building a design implementation from analyzed source files, you identify the top-level entity (VHDL), module (Verilog), or

schematic design. Foundation Express uses this information to start building design hierarchy and interconnections.

Identify the top-level design in one of these two ways:

- Click the drop-down list of top-level designs in the tool bar to see a list of all entities, modules, and netlist designs in the source files. Scroll through the list to find and choose the top-level design. In this example, choose tutor from the list.

  The "Identifying the Top-Level Design" figure shows the top-level design drop-down list of top-level designs and the expanded design source file icon.

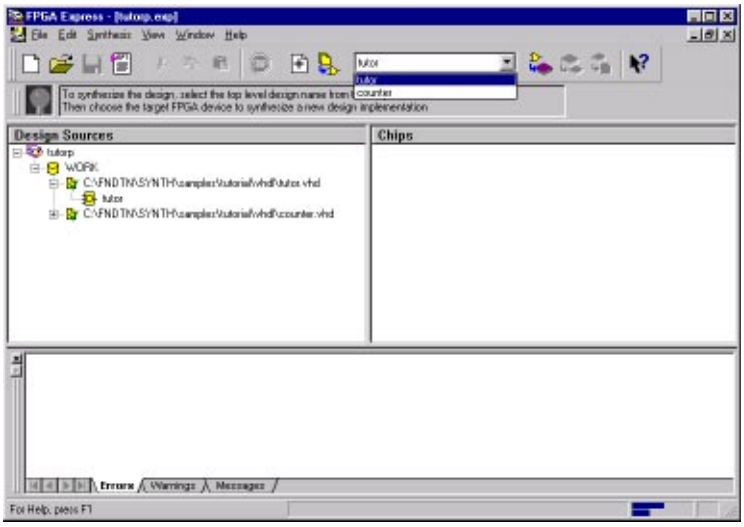

Figure 3-8 Identifying the Top-Level Design

The Create Implementation dialog box automatically appears. See the "Create Implementation Dialog Box" figure.

- Double click the source file to expand it and display an icon for the top-level design. Select the icon, click the right mouse button in the Design Sources window, and select Create Implementation. The Create Implementation dialog box appears.

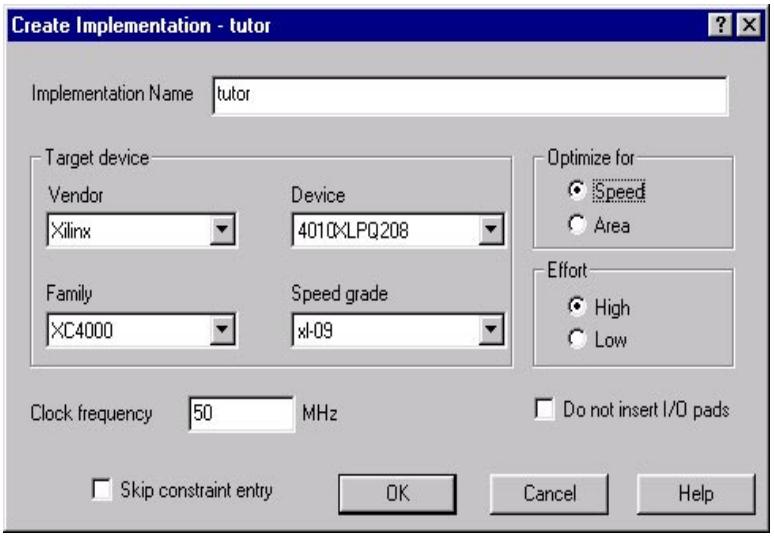

Figure 3-9 Create Implementation Dialog Box

You can also open the Create Implementation dialog box by clicking this icon on the tool bar.

Specifying the Target Architecture

To create a design implementation and synthesize logic, you must specify the target architecture in the Create Implementation dialog box.

To specify a target architecture:

1. Enter an implementation name. If you do not enter a name, Foundation Express automatically creates a unique implementation name.
2. Specify the family for the design.
3. (Optional) Specify the device type and speed grade.

For this tutorial, you can choose any family or device. The tutor design is small enough to fit any device family supported by Foundation Express.

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Setting the Target Clock Frequency

Set the target clock frequency for the design in the Create Implementation dialog box. This target frequency is used as the default value for all clocks in the design. After you synthesize the design implementation, you can change target clock frequencies in the design constraint tables.

Enter a target clock frequency in MHz. For this example, enter 50 MHz.

Creating the Design Implementation

After you set the target architecture and clock frequency, Foundation Express is ready to synthesize architecture-specific logic and create a design implementation.

To create a design implementation:

1. In the Create Implementation dialog box, verify the target architecture, clock frequency, and implementation name.
2. (Optional) Other specifications you can give in this dialog box include: choosing to optimize for speed or area with high or low CPU effort; choosing I/O pad insertion, if applicable; and choosing to skip constraint entry at this time (see Pushbutton Design Flow in the online help). For this tutorial, do not select Skip constraint entry.
3. Click OK.

   When Foundation Express has finished creating the design implementation, an icon, its name, and target device appear in the Chips window. The implementation icon indicates its status. See the "Creating the Design Implementation" figure.

   Check the output window to investigate errors and warnings.

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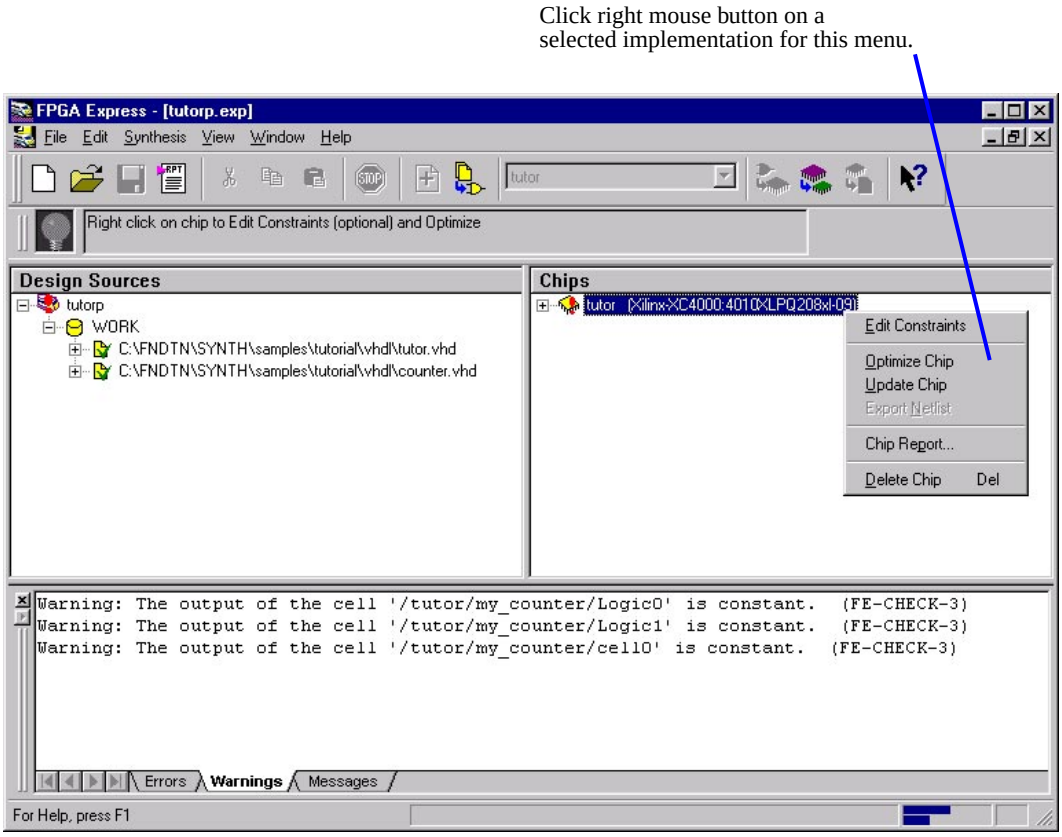

Figure 3-10 Creating the Design Implementation

To create the design implementation, Foundation Express synthesizes logic for each source file. It determines the complete hierarchical structure and topology of the design, including multiple-level links and references between subdesigns. With this information, Foundation Express produces an intermediate, unoptimized design implementation.

Entering Design Constraints and Controls (optional)

Before you start to optimize a design to a target device, you can set performance constraints, attributes, and optimization controls. Design constraints guide Foundation Express with specific optimization requirements.

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This step is optional, but it is highly recommended, and is only available for those how have purchased this feature. Entering your requirements in the constraint tables can improve the results of place and route tools. For example, entering constraints for an output port with restrictive speed requirements makes it easier for the place and route tool to fulfill those requirements. In another example, if a design is very large with many hierarchical levels, entering hierarchy constraints helps the place and route tool. If default constraints are not sufficient for your requirements, you might have to repeat creating and optimizing implementations to enter constraints.

Foundation Express separates constraint entries into logically related groups (for example, clocks, ports, and paths). Foundation Express extracts design-specific information such as clock names, port names, and design hierarchy from the design and displays it in FPGA / CPLD Xilinx-specific tables. You enter performance constraints, attributes, and optimization options directly into the tables. Each set of constraint tables and dialog boxes is specific to a particular target FPGA architecture. Controls for some target technologies are available through a Xilinx-specific dialog box that is displayed as another tab with the constraint tables.

To enter design constraints, attributes, and options:

1. Select the design implementation, click the right mouse button, and select Edit Constraints to open the design constraint and optimization-control tables.
2. Constraints and controls are logically separated by function into separate Clocks, Paths, Ports, and Modules tables as shown in the "Ports Constraint Table and Other Table Tabs" figure. Click the tabs to toggle between the tables. Use the online help if you need instructions and information about specific constraints, attributes, and optimization options.

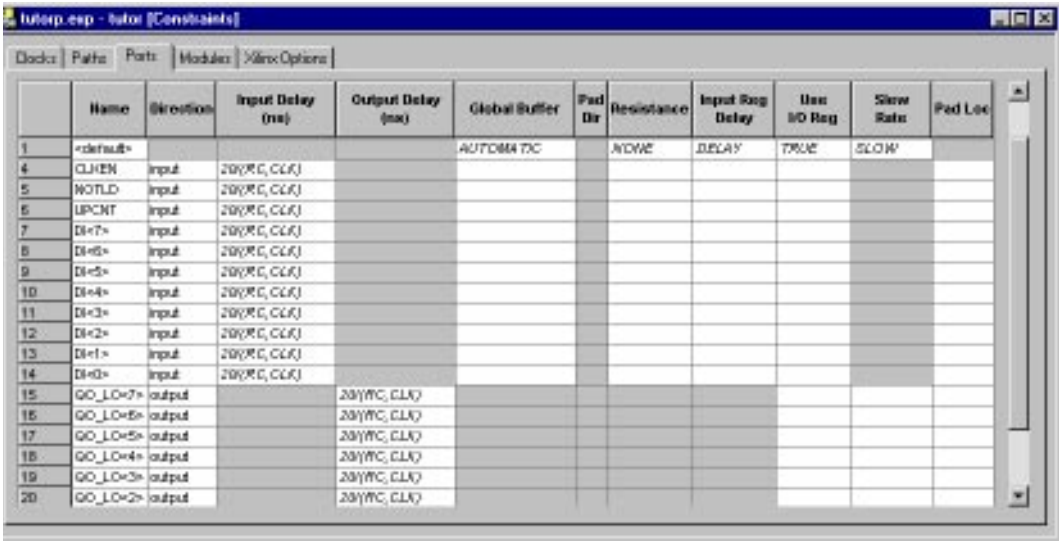

Figure 3-11 Ports Constraint Table and Other Table Tabs

Open and explore the tables for the tutor implementation. The contents of the tables depend on the architecture that you chose. Notice that clock and pad tables are preloaded with the clock frequency (and corresponding period) that you entered for the base clock frequency.

3. After entering constraint, attribute, and option information, close the implementation's constraint window.

Optimizing a Design Implementation

After you finish entering constraint, attribute, and option definitions, you are ready to optimize the design implementation and generate FPGA netlists.

In this step, you optimize a design implementation for performance and area, guided by the constraints and controls you entered in the constraint tables.

To optimize a design implementation:

1. Click the design implementation in the Chips window to select it. Its name is displayed in the top-level design field of the tool bar.

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2. Click the right mouse button and select Optimize Chip or click this icon in the tool bar.

A new optimized implementation icon appears beneath the original implementation.

When you optimize a design implementation, Foundation Express analyzes the actual timing and area of your design to see whether they meet your requirements. After optimization, the design implementation tables display the constraints you have specified with the results of your design so you can compare them.

Analyzing Timing

Determine circuit performance by checking the results of optimization and analyzing timing information shown in the constraint tables.

To view the results of optimization:

1. Open an optimized implementation by clicking the right mouse button and selecting View Results.
2. Check the Clocks constraint table to see the maximum clock frequencies Foundation Express calculated for each of the clocks in the design. Clock frequency violations appear in red. The "Viewing Optimization Results in the Clocks Constraint Table" figure shows the Clocks constraint table after optimization.

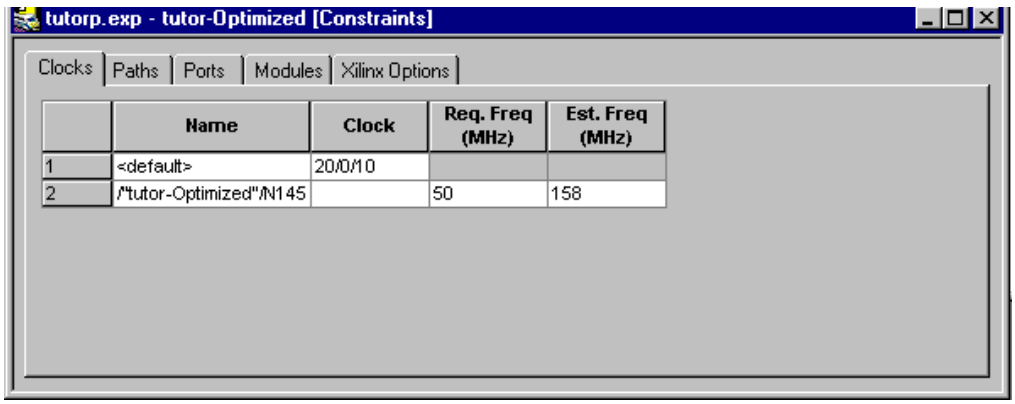

Figure 3-12 Viewing Optimization Results in the Clocks Constraint Table

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3. Check the Paths constraint table for more detail on timing violations. Select a path group to see a list of paths in that group. Select a path from the list to see the details of path composition, cumulative delays, and fanout. The "Viewing Optimization Results in the Paths Constraint Table" figure shows the Paths constraint table after optimization. See the online help for a description of timing analysis in Foundation Express.

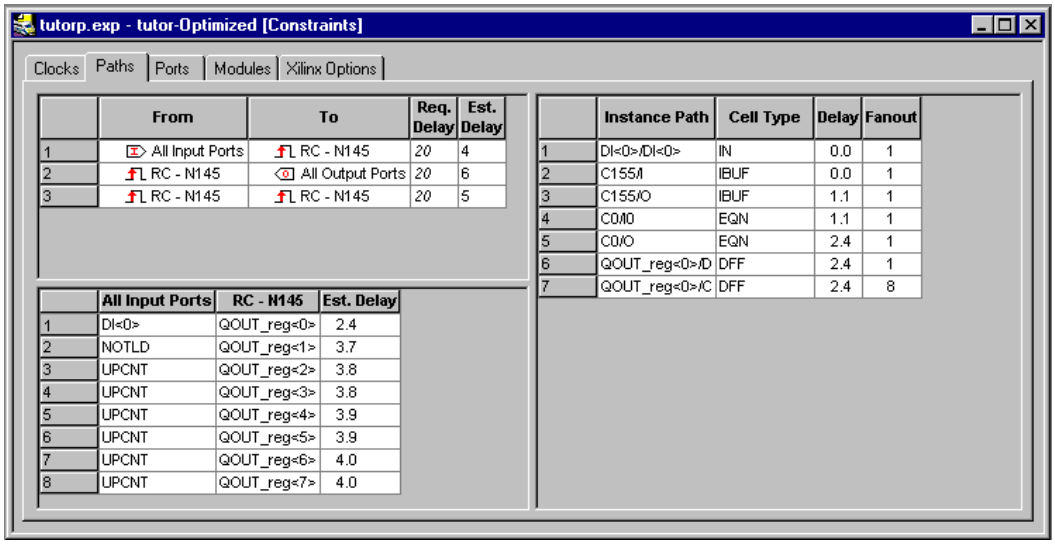

Figure 3-13 Viewing Optimization Results in the Paths Constraint Table

4. Check the Ports constraint table for information about input and output delays. "Viewing Optimization Results in the Ports Constraint Table" figure shows the Ports constraint table where results include the slack for input arrival time and output delay for each port.

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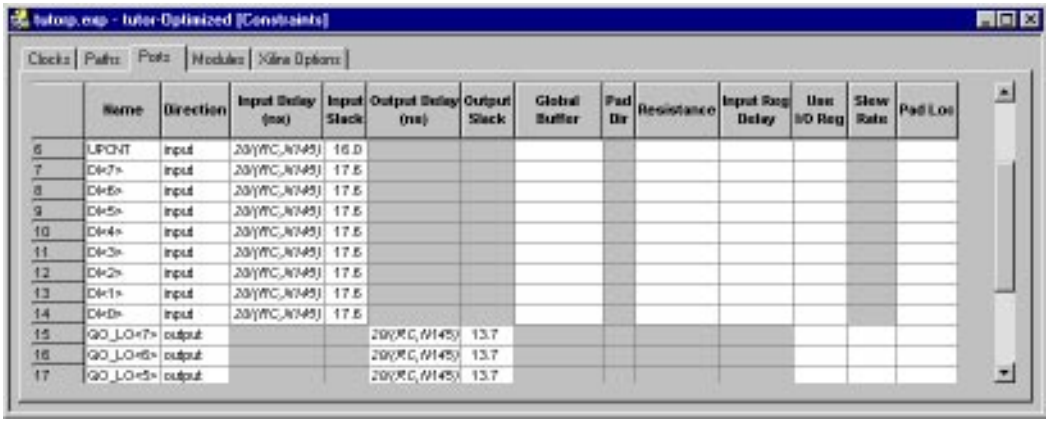

Figure 3-14 Viewing Optimization Results in the Ports Constraint Table

5. Check the Modules constraint table for information about the device resources used. Double-click the rows in the Area column for details about cell count. The "Viewing Optimization Results in the Modules Constraint Table" figure shows the Modules constraint table after optimization.

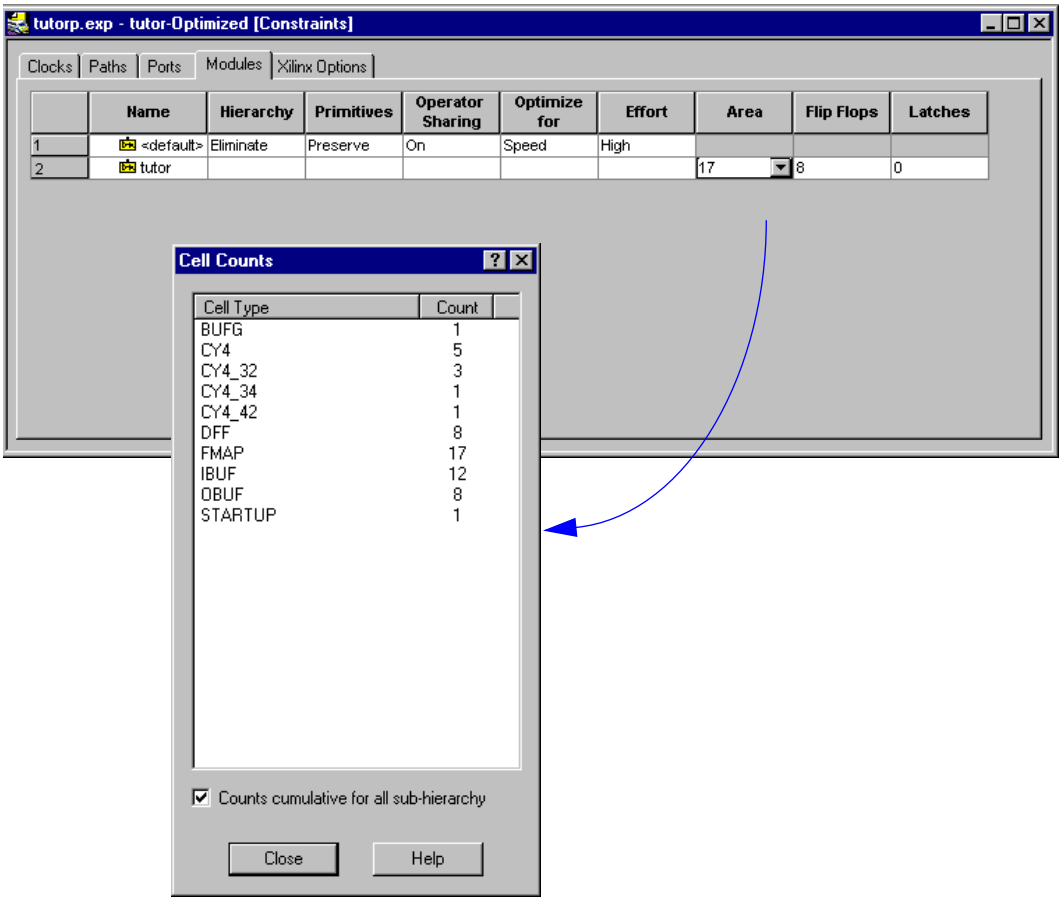

Figure 3-15 Viewing Optimization Results in the Modules Constraint Table

Generating Output

When the design implementation is optimized, you can generate an FPGA netlist file that is formatted for immediate place and route by the Xilinx implementation tools. You can also generate a report file to review and document the project.

These are the steps in generating output for your optimized implementation:

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1. Generating netlist files
2. Generating a report

Generating Netlist Files

Generating an FPGA netlist and project report completes the synthesis design flow. Foundation Express generates netlists that can be directly processed by the place and route systems from technology vendors.

To generate FPGA netlist files:

1. Select the optimized design implementation. Click  in the tool bar or click the right mouse button and select Export Netlist. The Export Netlist dialog box as shown in "Export Netlist Dialog Box" figure appears.
2. In the Export Netlist dialog box, choose the name and location (folder) for the netlist files. You can choose to export timing constraints with the netlist.
3. Click Save. This will create an XNF file.

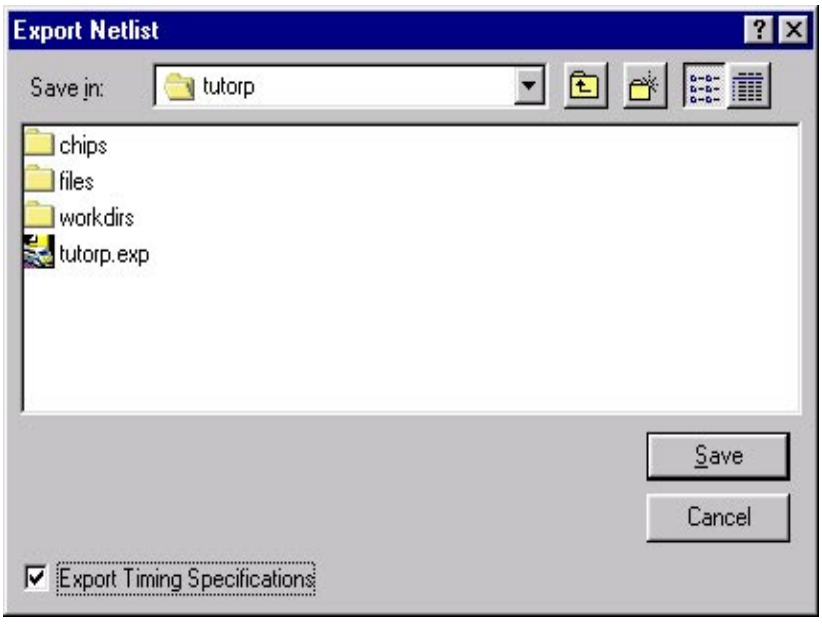

Figure 3-16 Export Netlist Dialog Box

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Generating a Report

You can generate a Foundation Express report on a project, library, file, or chip. A project report documents the design through the synthesis and optimization design flow and includes information such as design source data, constraints, and optimization options.

1. To generate a report:
2. Select the project, library, design, or chip icon in the project window.
3. Click the right mouse button and select the report menu item or click this icon on the tool bar. Specify the name and choose the location for the report.The "Generate Project Report Dialog Box" figure shows the Generate Project Report dialog box.

4. Click Save. Foundation Express creates a text file containing summary information for the whole project, the library, the design, or the chip.
5. Open the report file in a text editor or word processing application.

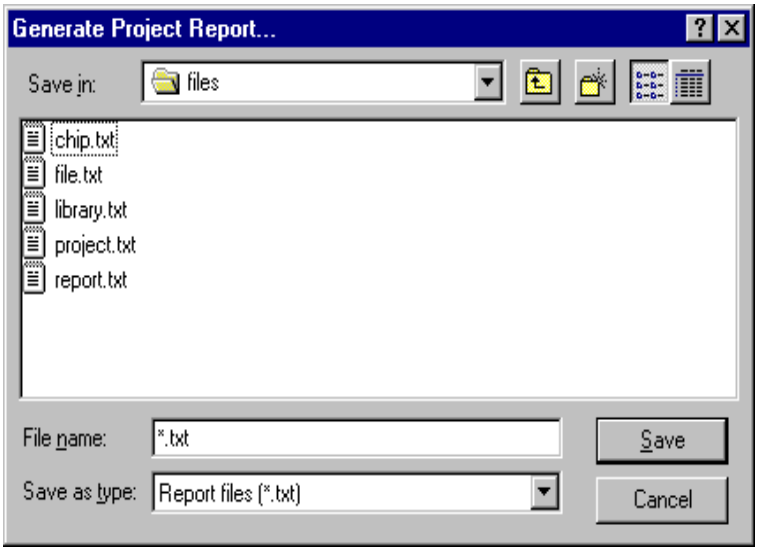

Figure 3-17 Generate Project Report Dialog Box

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Summary

You have completed the Foundation Express design flow tutorial. The design flow is comprised of these steps:

1. Creating design source files.
2. Setting up a Foundation Express project, identifying, analyzing, and debugging source files
3. Creating a design implementation, specifying the top-level design and target device, and synthesizing logic from the design descriptions
4. Entering performance constraints and controls to guide the optimization process
5. Optimizing the logic
6. Analyzing timing
7. Generating netlist and report files

Now you are ready to apply the power of Foundation Express to your own designs.