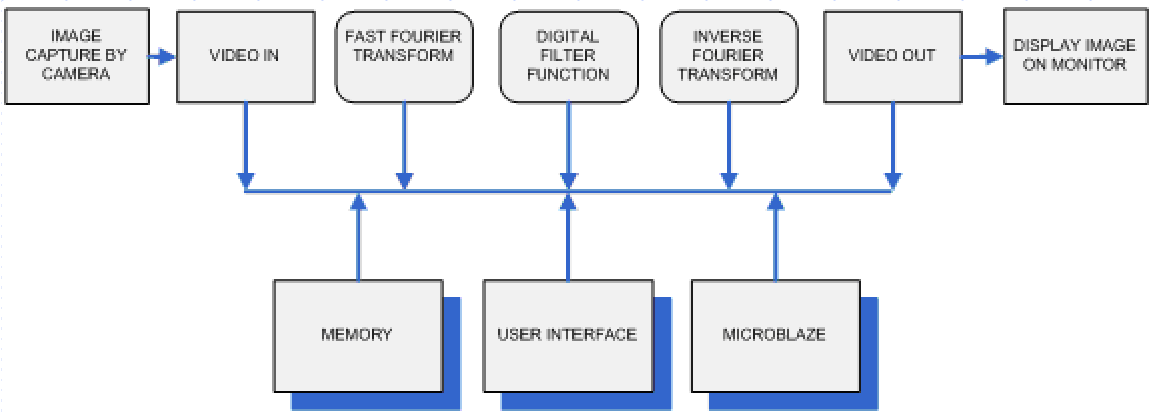
ECE532 Design Project

Photoshop Functionalities on FPGA

Pearl Liu
George Ng

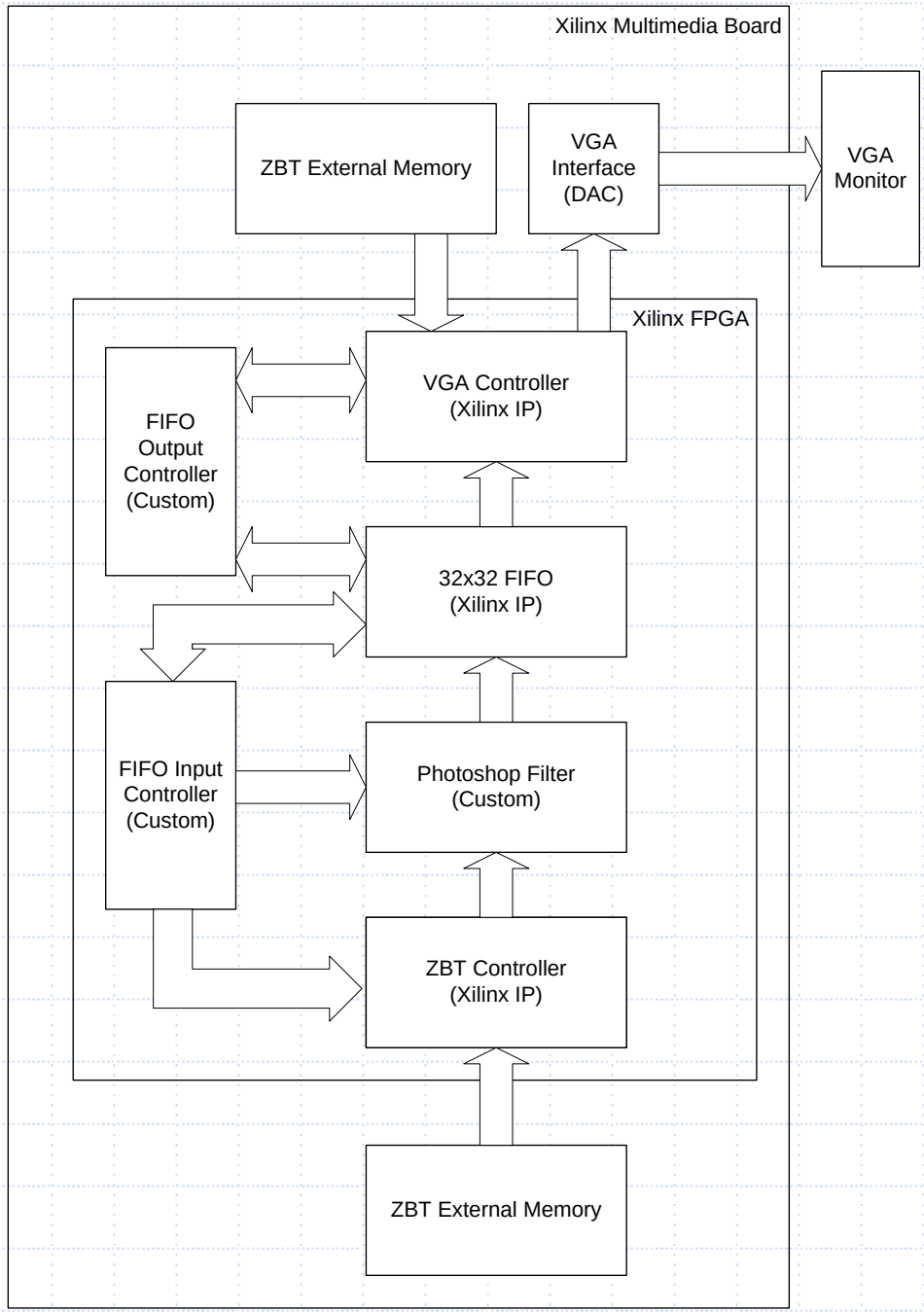
Initial Goals

- Implementation Photoshop filters in real-time on FPGA
- Real time image capture, filtering, and display



Final Design

- Bitmap image stored in ZBT
- Digital Photoshop filter processes data
- Controllers manage data transfer between ZBT and display controller
- Filtered image data displayed on VGA monitor from FIFO



Problems and Changes

- Through research we discovered that digital filtering can be done in time domain eliminating need for FFT and IFFT blocks
- Proving 1D filters work on 2D images in Matlab and simulation testbenches (architectural design)
- Replaced video capture core data with bitmap image to ensure data reliability
- Lack of documentation for example Xilinx cores provided on website

Design Blocks

- Custom: ZBT to FIFO controller, FIFO to display controller, Digital filters
- Xilinx IP: ZBT controller, VGA Display controller, FIFO (CoreGen)

Design Process

- Testbench simulation of individual custom blocks to verify functionality
- Testbenching simulation at every design level
- Simulate Xilinx IP to understand block behavior
- Architectural design phase to prove design concepts at a high level before beginning hardware implementation

What did we learn?

- Importance of simulation for circuit visibility
- Importance of prototyping design at high level to prove functionality
- Filters can be implemented in time domain without FFT and IFFT
- How to use Xilinx example design core and integrated in our system
- Bitmap image file format
- How to design blur and emboss filters

Conclusion

- Successfully implemented 80% of proposed project