SVGA Network Poker

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Project Description

- 2 player Texas Holdem
- Communication over the ethernet between 2 Xilinx multimedia boards (server/client) to run gameplay
- Display table, cards and chips for each player on separate SVGA monitors as game progresses

Main Hardware Blocks

- **Microblaze processor**
  - to run ethernet and poker software
- **EMAC IP Core**
  - to communicate with ethernet hub to other board (adapted from project by Patrick Akl)
- **Graphics controller**
  - custom designed to display game
- **4x BRAM controller IP**
  - cores to control BRAM blocks for instructions, data and character mode SVGA
- **UART**
  - for communication with a PC serial port
- **ZBT EMC**
  - and memory chip to store embedded software
- **Interrupt controller and timer**
  - for incoming frame interrupts, receiving and ack responses
- **GPIO**
  - for manual control of processor and monitor
- **MB Debug Module**
  - for debugging of running software

Software Blocks

- Ethernet drivers from Xilinx to control EMAC
- Ethernet control software to manage frames and fault tolerance (adapted from project by Patrick Akl)
- Ethernet Send/Receive protocol and software to establish common communication between two boards
- Poker gameplay software (custom designed)

Design Process

- Modular design sections divided equally
  - Hardware System
    - MB and ethernet hardware system design
    - Character Mode SVGA controller/bridge
  - Software System
    - Poker gameplay
    - Ethernet control
    - Ethernet protocol
- Testing and debugging of each module separately
- System integration module by module and regression testing

Lessons Learned

- You can fit anything on an FPGA these days
- Having good EDA tools is key to doing full hardware and software system design
- Having knowledge of the underlying hardware can really help with understanding how to better write more complex software