OPB Timer/Counter

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Product Overview

Introduction

This document describes the specifications for a timer/counter core for the On-Chip Peripheral Bus (OPB).

The TC (Timer/Counter) is a 32-bit timer module that attaches to the OPB.

Features

- OPB v2.0 bus interface with byte-enable support
- Supports 32-bit bus interface
- Two programmable interval timers with interrupt, event generation, and event capture capabilities
- Configurable counter width
- One Pulse Width Modulation (PWM) output
- Freeze input for halting counters during software debug

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Virtex-II Pro™, Virtex™-II	
Version of Core	opb_timer	v1.00b
Resources Used		
	Min	Max
Slices	99	200
LUTs	99	275
FFs	105	266
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

Timer/Counter Organization

The TC is organized as two identical timer modules. Each timer module has an associated register (the Load Register) that is used to hold either the initial value for the counter for event generation or a capture value, depending on the mode of the timer. The TC block diagram is shown in the following figure:

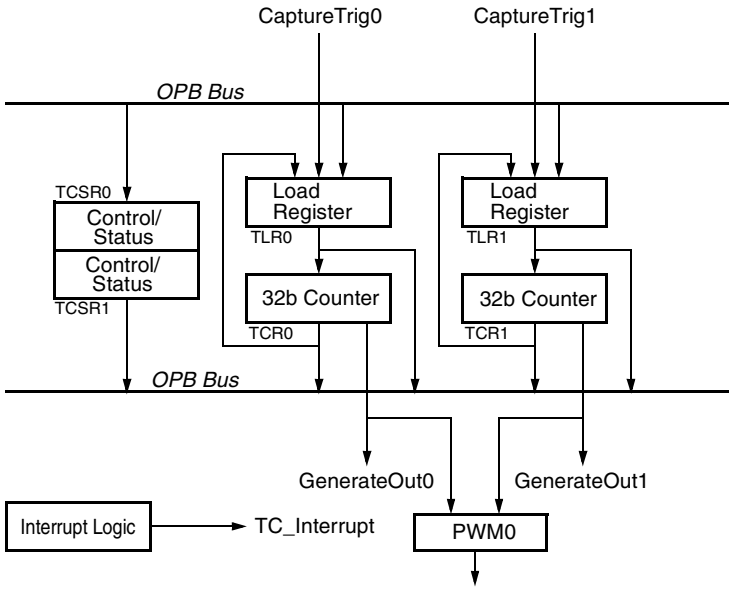

Figure 1: **Timer/Counter Organization**

The *generate value* is used to generate a single interrupt at the expiration of an interval, or a continuous series of interrupts with a programmable interval. The *capture value* is the timer value that has been latched on detection of an external event. The clock rate of the timer modules is OPB_Clk (no prescaling of the clock is performed). All of the TC interrupts are OR'ed together to generate a single external interrupt signal. The interrupt service routine reads the control/status registers to determine the source of the interrupt.

Programming Model

Timer Modes

You can use a Generate Mode, a Capture Mode, or a Pulse Width Modulation (PWM) Mode with the two timer/counter modules.

Generate Mode

In Generate Mode, the value in the Load Register is loaded into the counter and the counter begins to count (up or down, selectable by the UDT bit in TCSR) when it is enabled. On transition of the carry out of the counter, the counter stops or automatically reloads the generate value from the Load Register and continues counting (selectable by the ARHT bit in TCSR). The TINT bit is set in TCSR and, if enabled, the external GenerateOut signal is driven to 1 for one clock cycle. If enabled, the interrupt signal for the timer is driven to 1 for one clock cycle. This mode is useful for generating repetitive interrupts or external signals with a specified interval.

Characteristics

Generate Mode has the following characteristics:

- The value loaded into the Load Register is called the generate value.

- On startup, the generate value in the Load Register must be loaded into the counter by setting the Load bit in the TCSR. This applies whether the counter is set up to Auto Reload or Hold when the interval has expired. Setting the Load bit to '1' loads the counter with the value in the Load Register. The Load bit must be cleared before the counter is enabled for proper operation.
- When the ARHT bit (Auto Reload/Hold) is set to '1' and the counter rolls over from all '1's to all '0's (when counting up), or from all '0's to all '1's (when counting down), the generate value in the Load Register will be automatically reloaded into the counter and the counter will continue to count. If the GenerateOut signal is enabled (bit GENT in the TCSR), an output pulse will be generated (one clock period in width). This is useful for generating a repetitive pulse train with a specified period.
- When the ARHT bit (Auto Reload/Hold) is set to '0' and the counter rolls over from all '1's to all '0's (when counting up), or from all '0's to all '1's (when counting down), the counter will hold at the current value and will not reload the generate value. If the generate out signal is enabled (bit GENT in the TCSR), an output pulse will be generated (one clock period in width). This is useful for a one-shot pulse that is to be generated after a specified period of time.
- The counter can be set up to count either up or down (bit UDT in the TCSR). If the counter is set up as a down counter, the generate value is the number of clocks in the timing interval. The period of the GenerateOut signal is the generate value times the clock period.
- When the counter is set to count down, $\text{TIMING\_INTERVAL} = (\text{TLRx} + 2) \times \text{OPB\_CLOCK\_PERIOD}$.
- When the counter is set to count up, $\text{TIMING\_INTERVAL} = (\text{MAX\_COUNT} - \text{TLRx} + 2) \times \text{OPB\_CLOCK\_PERIOD}$
  where MAX_COUNT is the maximum count value of the counter, such as 0xFFFFFFFF for a 32-bit counter.
- The GenerateOut signals can be configured as high-true or low-true.

Capture Mode

In Capture Mode, the value of the counter is stored in the Load Register when the external capture signal is asserted. The TINT bit is also set in TCSR on detection of the capture event. The counter can be configured as an up or down counter for this mode (selectable by the UDT bit in TCSR). The ARHT bit controls whether the capture value is overwritten with a new capture value before the previous TINT flag is cleared. This mode is useful for time tagging external events while simultaneously generating an interrupt.

Characteristics

Capture Mode has the following characteristics:

- The capture signal can be configured to be low-true or high true.
- The capture signal is sampled within the TC with the OPB_Clk. The capture event is defined as the transition on the sampled signal to the asserted state. For example, if the capture signal is defined to be high-true, then the capture event is when the sampled (synchronized to the OPB_Clk) signal transitions from '0' to '1'.
- When the capture event occurs, the counter value is written to the Load Register. This value is called the capture value.
- When the ARHT bit (Auto Reload/Hold) is set to '0' and the capture event occurs, the capture value is written to the Load Register. The Load Register will hold this capture value until the Load Register is read. If the Load Register is not read, subsequent capture events will not update the Load Register and will be lost.
- When the ARHT bit (Auto Reload/Hold) is set to '1' and the capture event occurs, the capture value is always written to the Load Register. Subsequent capture events will update the Load Register and will overwrite the previous value, whether it has been read or not.
- The counter can be set up to count either up or down (bit UDT in the TCSR).

Pulse Width Modulation (PWM) Mode

In PWM mode, two timer/counters are used as a pair to produce an output signal (PWM0) with a specified frequency and duty factor. Timer0 sets the period and Timer1 sets the high time for the PWM0 output.

Characteristics

PWM Mode has the following characteristics:

- The mode for both Timer0 and TImer1 must be set to Generate Mode (bit MDT in the TCSR set to '0').
- The PWMA0 bit in TCSR0 and PWMB0 bit in TCSR1 must be set to '1' to enable PWM mode.

- The GenerateOut signals must be enabled in the TCSR (bit GENT set to '1'). The PWM0 signal is generated from the GenerateOut signals of Timer0 and Timer1, so these signals must be enabled in both timer/counters.
- The assertion level of the GenerateOut signals for both timers in the pair must be set to '1'. This is done by setting C_GEN0_ASSERT and C_GEN1_ASSERT to '1'.
- The counter can be set to count up or down.

Setting the PWM Period and Duty Factor

The PWM period is determined by the generate value in Timer0's Load Register (TLR0). The PWM high time is determined by the generate value in Timer1's Load Register (TLR1). The period and duty factor are calculated as follows:

When counters are configured to count **up** (UDT = '0'):

$$\text{PWM\_PERIOD} = (\text{MAX\_COUNT} - \text{TLR0} + 2) \times \text{OPB\_CLOCK\_PERIOD}$$

$$\text{PWM\_HIGH\_TIME} = (\text{MAX\_COUNT} - \text{TLR1} + 2) \times \text{OPB\_CLOCK\_PERIOD}$$

When counters are configured to count **down** (UDT = '1'):

$$\text{PWM\_PERIOD} = (\text{TLR0} + 2) \times \text{OPB\_CLOCK\_PERIOD}$$

$$\text{PWM\_HIGH\_TIME} = (\text{TLR1} + 2) \times \text{OPB\_CLOCK\_PERIOD}$$

where MAX_COUNT is the maximum count value for the counter, such as 0xFFFFFFFF for a 32-bit counter.

Interrupts

The TC interrupt signals can be enabled or disabled with the ENIT bit in the TCSR. The interrupt status bit (TINT) in the TCSR cannot be disabled and always reflects the current state of the timer interrupt. In Generate Mode, a timer interrupt is caused by the counter rolling over (the same condition used to reload the counter when ARHT is set to '1'). In Capture Mode, the interrupt event is the capture event. Characteristics of the interrupts are:

- Interrupt events can only occur when the timer is enabled. In Capture Mode, this prevents interrupts from occurring before the timer is enabled.
- The interrupt signal goes high when the interrupt condition is met and the interrupt is enabled in the TCSR. The interrupt is asserted when the interrupt signal is high.
- A single interrupt signal is provided. The interrupt signal is the OR of the interrupts from the two counters. The interrupt service routine must poll the TCSR's to determine the source or sources of the interrupt.
- The interrupt status bit (TINT in the TCSR) can only be cleared by writing a '1' to it. Writing a '0' to it has no effect on the bit. Since the interrupt condition is an edge (the counter rollover or the capture event), it can cleared at any time and will not indicate an interrupt condition until the next interrupt event.

Register Data Types and Organization

TC registers are accessed as one of the following types:

- Byte (8 bits)
- Half word (2 bytes)
- Word (4 bytes)

Configuration

The following table shows TC configurations and access type.

Table 1: **TC Configuration and Access Type**

Configuration	Access Type
32-bit slave OPB peripheral	Word

The addresses of the TC registers are shown in the following table:

Table 2: **TC Register Address Map**

Register	Address (Hex)	Size	Type	Description
TCSR0	0x00	Word	R/W	Control/Status Register 0
TLR0	0x04	Word	R/W	Load Register 0
TCR0	0x08	Word	R	Timer/Counter Register 0
TCSR1	0x10	Word	Read/Write	Control/Status Register 1
TLR1	0x14	Word	Read/Write	Load Register 1
TCR1	0x18	Word	Read	Timer/Counter Register 1

The TC registers are organized as big-endian data. The bit and byte labeling for the big-endian data types is shown in the following figure:

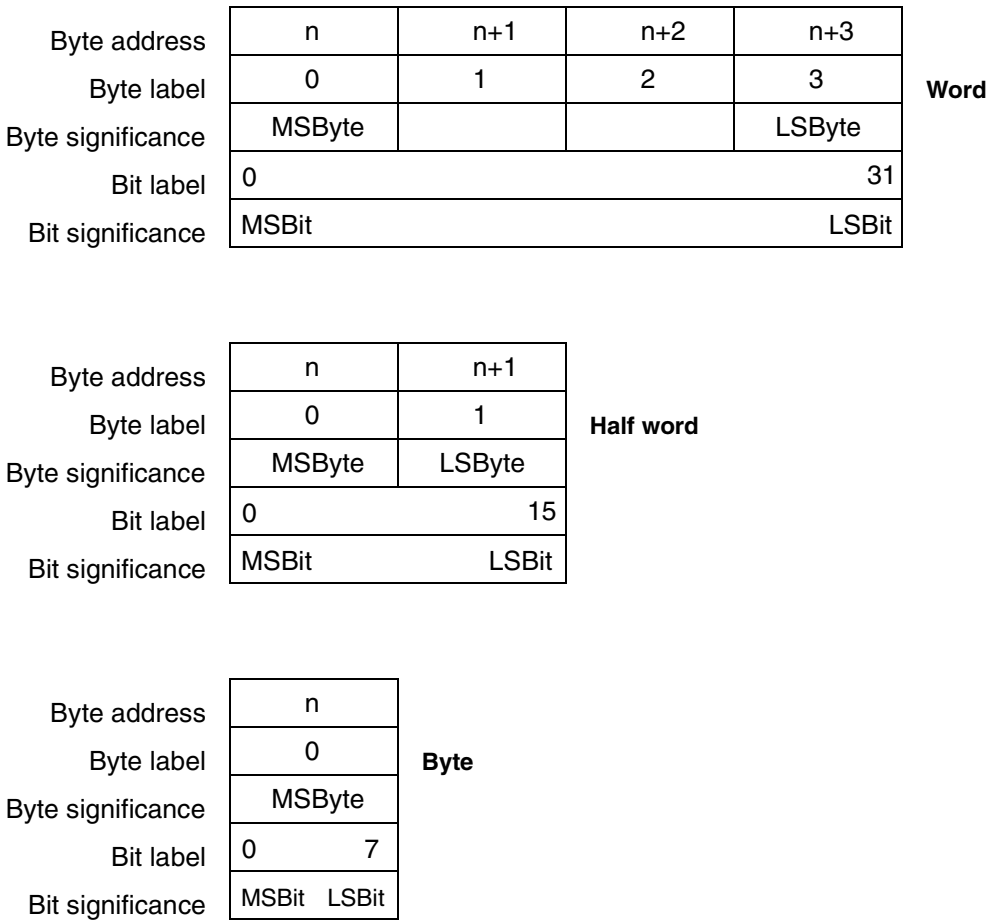

Figure 2: **Big-Endian Data Types**

Register Descriptions

Load Register (TLR0-TLR1)

When the counter width has been configured as less than 32 bits, the Load Register value is right-justified in TLR0 and TLR1. The least-significant counter bit is always mapped to Load Register bit 31.

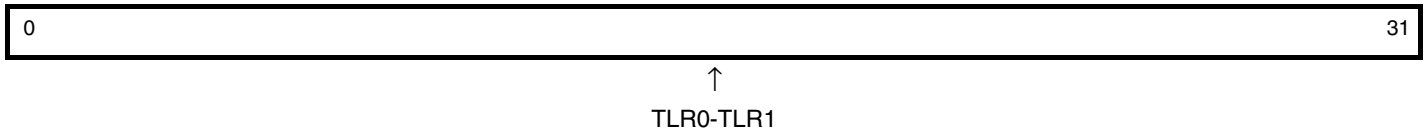

Figure 3: **TLR0-TLR1**

Timer/Counter Register (TCR0-TCR1)

When the counter width has been configured as less than 32 bits, the count value is right-justified in TCR0 and TCR1. The least-significant counter bit is always mapped to Timer/Counter Register bit 31.

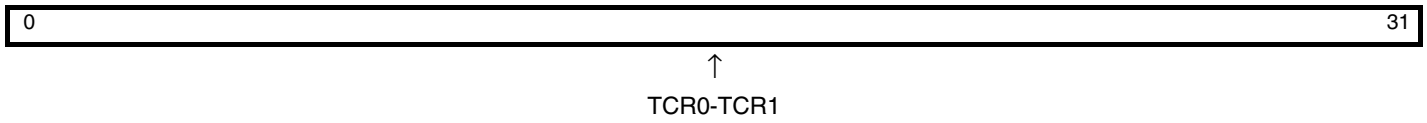

Figure 4: **TCR0-TCR1**

Control/Status Register 0 (TCSR0)

Control/Status Register 0 contains the control and status bits for timer module 0.

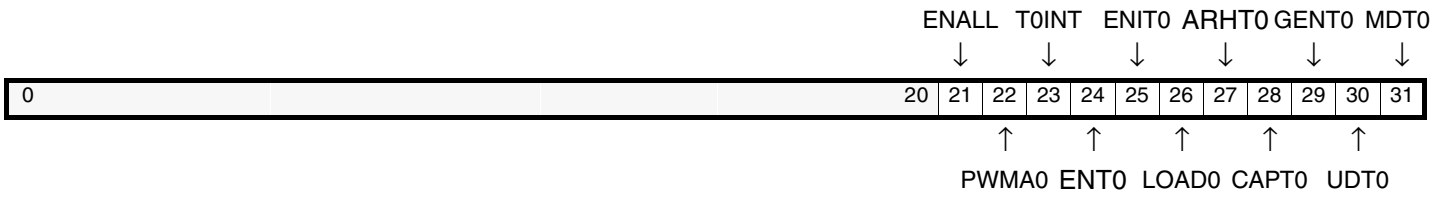

Figure 5: **TCSR0**

Table 3: **Control/Status Register 0 (TCSR0)**

Bits	Name	Description	Reset Value
0:20	Reserved		

Table 3: **Control/Status Register 0 (TCSR0) *(Continued)***

Bits	Name	Description	Reset Value
21	ENALL	**Enable All Timers** 0 No effect on timers 1 Enable all timers (counters run) This bit is mirrored in all control/status registers and is used to enable all counters simultaneously. Writing a '1' to this bit sets ENALL, ENT0, and ENT1. Writing a '0' to this register clears ENALL but has no effect on ENT0 and ENT1.	0
22	PWMA0	**Enable Pulse Width Modulation for Timer0** 0 Disable pulse width modulation 1 Enable pulse width modulation PWM requires using Timer0 and Timer1 together as a pair. Timer0 sets the period of the PWM output, and Timer1 sets the high time for the PWM output. For PWM Mode, MDT0 and MDT1 must be '0' and C_GEN0_ASSERT and C_GEN1_ASSERT must be '1'.	0
23	TINT0	**Timer0 Interrupt** Indicates that the condition for an interrupt on this timer has occurred. If the timer mode is capture and the timer is enabled, this bit indicates a capture has occurred. If the mode is generate, this bit indicates the counter has rolled over. Must be cleared by writing a '1'. *Read:* 0 No interrupt has occurred 1 Interrupt has occurred *Write:* 0 No change in state of T0INT 1 Clear T0INT (clear to '0')	0
24	ENT0	**Enable Timer0** 0 Disable timer (counter halts) 1 Enable timer (counter runs)	0
25	ENIT0	**Enable Interrupt for Timer0** Enables the assertion of the interrupt signal for this timer. Has no effect on the interrupt flag in TCSR0. 0 Disable interrupt signal 1 Enable interrupt signal	0
26	LOAD0	**Load Timer0** 0 No load 1 Loads timer with value in TLR0	0
27	ARHT0	**Auto Reload/Hold Timer0** When the timer is in Generate Mode, this bit determines whether the counter reloads the generate value and continues running or holds at the termination value. In Capture Mode, this bit determines whether a new capture trigger overwrites the previous captured value or if the previous value is held. 0 Hold counter or capture value 1 Reload generate value or overwrite capture value	0

Table 3: **Control/Status Register 0 (TCSR0) *(Continued)***

Bits	Name	Description	Reset Value
28	CAPT0	Enable External Capture Trigger Timer0 0 Disables external capture trigger 1 Enables external capture trigger	0
29	GENT0	Enable External Generate Signal Timer0 0 Disables external generate signal 1 Enables external generate signal	0
30	UDT0	Up/Down Count Timer0 0 Timer functions as up counter 1 Timer functions as down counter	0
31	MDT0	Timer0 Mode See the Timer Modes section. 0 Timer mode is generate 1 Timer mode is capture	0

Control/Status Register 1 (TCSR1)

Control/Status Register 1 contains the control and status bits for timer module 1.

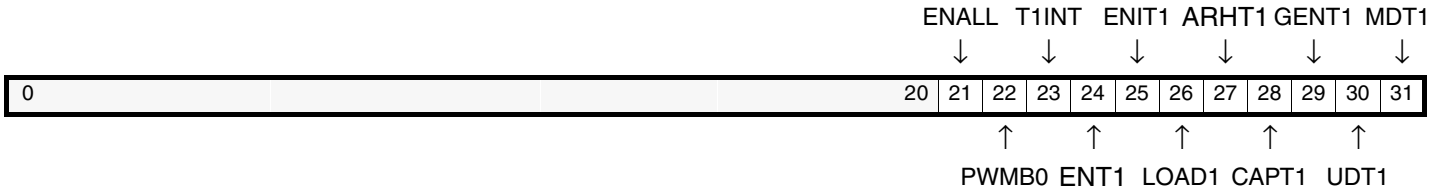

Figure 6: **TCSR1**

Table 4: **Control/Status Register 1 (TCSR1)**

Bits	Name	Description	Reset Value
0:20	Reserved		
21	ENALL	**Enable All Timers** 0 No effect on timers 1 Enable all timers (counters run) This bit is mirrored in all control/status registers and is used to enable all counters simultaneously. Writing a '1' to this bit sets ENALL, ENT0, and ENT1. Writing a '0' to this register clears ENALL but has no effect on ENT0 and ENT1.	0

Table 4: **Control/Status Register 1 (TCSR1) *(Continued)***

Bits	Name	Description	Reset Value
22	PWMB0	**Enable Pulse Width Modulation for Timer1** 0 Disable pulse width modulation 1 Enable pulse width modulation PWM requires using Timer0 and Timer1 together as a pair. Timer0 sets the period of the PWM output, and Timer1 sets the high time for the PWM output. For PWM Mode, MDT0 and MDT1 must be '0' and C_GEN0_ASSERT and C_GEN1_ASSERT must be '1'.	0
23	TINT1	**Timer1 Interrupt** Indicates that the condition for an interrupt on this timer has occurred. If the timer mode is capture and the timer is enabled, this bit indicates a capture has occurred. If the mode is generate, this bit indicates the counter has rolled over. Must be cleared by writing a '1'. *Read:* 0 No interrupt has occurred 1 Interrupt has occurred *Write:* 0 No change in state of T1INT 1 Clear T1INT (clear to '0')	0
24	ENT1	**Enable Timer1** 0 Disable timer (counter halts) 1 Enable timer (counter runs)	0
25	ENIT1	**Enable Interrupt for Timer1** Enables the assertion of the interrupt signal for this timer. Has no effect on the interrupt flag in TCSR1. 0 Disable interrupt signal 1 Enable interrupt signal	0
26	LOAD1	**Load Timer1** 0 No load 1 Loads timer with value in TLR1	0
27	ARHT1	**Auto Reload/Hold Timer1** When the timer is in generate mode, this bit determines whether the counter reloads the generate value and continues running or holds at the termination value. In capture mode, this bit determines whether a new capture trigger overwrites the previous captured value or if the previous value is held until it is read. 0 Hold counter or capture value 1 Reload generate value or overwrite capture value	0
28	CAPT1	Enable External Capture Trigger Timer1 0 Disables external capture trigger 1 Enables external capture trigger	0
29	GENT1	Enable External Generate Signal Timer1 0 Disables external generate signal 1 Enables external generate signal	0

Table 4: **Control/Status Register 1 (TCSR1) *(Continued)***

Bits	Name	Description	Reset Value
30	UDT1	Up/Down Count Timer1 0 Timer functions as up counter 1 Timer functions as down counter	0
31	MDT1	Timer1 Mode See the Timer Modes section. 0 Timer mode is generate 1 Timer mode is capture	0

Implementation

I/O Summary

Table 5: **Summary of Timer Core I/O**

Signal	Interface	I/O	Description
OPB_Clk	OPB	I	OPB Clock
OPB_Rst	OPB	I	OPB Reset
OPB_ABus[0:31]	OPB	I	OPB Address Bus
OPB_BE[0:3]	OPB	I	OPB Byte Enables
OPB_DBus[0:31]	OPB	I	OPB Data Bus
OPB_RNW	OPB	I	OPB Read, Not Write
OPB_select	OPB	I	OPB Select
OPB_seqAddr	OPB	I	OPB Sequential Address
TC_DBus[0:31]	OPB	O	TC Data Bus
TC_errAck	OPB	O	TC Error Acknowledge
TC_retry	OPB	O	TC Retry
TC_toutSup	OPB	O	TC Timeout Suppress
TC_xferAck	OPB	O	TC Transfer Acknowledge
CaptureTrig0	Ext.	I	Capture Trigger 0
CaptureTrig1	Ext.	I	Capture Trigger 1
GenerateOut0	Ext.	O	Generate Output 0
GenerateOut1	Ext.	O	Generate Output 1
PWM0	Ext.	O	Pulse Width Modulation Output 0
Interrupt	Ext.	O	Interrupt
Freeze	Ext.	I	Freeze Count Value

MPD File Parameters

The opb_timer.mpd (Microprocessor Peripheral Definition) file contains a list of the peripheral's parameters that are fixed at FPGA configuration time. The parameters are described in the following table:

Table 6: **MPD Parameters**

Parameter	Description	Type
C_FAMILY	FPGA family, one of virtex, virtexe, virtex2, virtex2p, spartan2, or spartan2e	string
C_COUNT_WIDTH	The width in bits of the counters in the OPB Timer/Counter	integer range 8 to 32
C_ONE_TIMER_ONLY	0: Two timers are present 1: One timer is present (No PWM mode)	integer
C_TRIG0_ASSERT	'0': CaptureTrig0 input is low-true '1': CaptureTrig0 input is high-true	std_logic
C_TRIG1_ASSERT	'0': CaptureTrig1 input is low-true '1': CaptureTrig1 input is high-true	std_logic
C_GEN0_ASSERT	'0': GenerateOut0 output is low-true '1': GenerateOut0 output is high-true	std_logic
C_GEN1_ASSERT	'0': GenerateOut1 output is low-true '1': GenerateOut1 output is high-true	std_logic
C_OPB_AWIDTH	The width in bits of the address bus attached to the peripheral.	integer
C_OPB_DWIDTH	The width in bits of the data bus attached to the peripheral.	integer
C_BASEADDR	Indicates the base address of this peripheral expressed as a std_logic_vector.	std_logic_vector (0 to C_AWIDTH-1)
C_HIGHADDR	Indicates the highest address occupied by this peripheral expressed as a standard logic vector.	std_logic_vector (0 to C_AWIDTH-1)

Device Utilization and Performance Benchmarks

The following table shows approximate resource utilization and performance benchmarks for the OPB Timer/Counter. The estimates shown are not guaranteed and can vary with FPGA family and speed grade, parameters selected for implementation, user timing constraints, and implementation tool version. Only parameters that affect resource utilization are shown in the following table:

Table 7: **OPB Timer/Counter Performance and Resource Utilization Benchmarks (Virtex-II Pro)**

Parameter Values		Device Resources			f_{MAX} (MHz)
C_ONE_TIMER_ONLY	C_COUNT_WIDTH	Slices	Slice Flip-Flops	4-input LUTs	f_{MAX}
1	8	99	105	99	130
1	16	119	131	133	130
1	32	158	197	192	130

Table 7: **OPB Timer/Counter Performance and Resource Utilization Benchmarks (Virtex-II Pro) *(Continued)***

Parameter Values		Device Resources			f_{MAX} (MHz)
C_ONE_TIMER_ONLY	C_COUNT_WIDTH	Slices	Slice Flip-Flops	4-input LUTs	f_{MAX}
0	8	113	126	136	130
0	16	148	168	172	130
0	32	200	266	275	130

Parameterization

The following characteristics of the TC can be parameterized:

- Base address for the TC registers
- Assertion level for CaptureTrig and GenerateOut signals (high-true or low-true)
- Number of timer/counter modules

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/19/01	1.0	Initial Xilinx release.
03/20/01	1.1	Incorporated feedback from initial review
05/08/01	1.2	Modified names
05/14/01	1.3	Added TCSR2
06/03/01	1.4	Moved timebase and WDT to separate core
08/09/01	1.5	Changed description of ENALL bits
03/22/01	1.6	Changed Compare Mode to Generate Mode, added mode descriptions, parameterized counter width
05/27/02	1.7	Update to EDK 1.0
07/23/02	1.8	Add XCO parameters for System Generator
11/11/02	1.9	Updated Device Utilization table
01/08/03	1.10	Update for EDK SP3
07/10/03	1.11	Update to new template
07/29/03	1.11.1	Change DS212 to DS465 because of duplication
09/24/03	1.11.2	Update trademarks
11/25/03	1.11.3	Fixes for CR 180134