System Proposal

Project Title:	**SVGA Network Poker**

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Course:	**ECE532 Digital Hardware**
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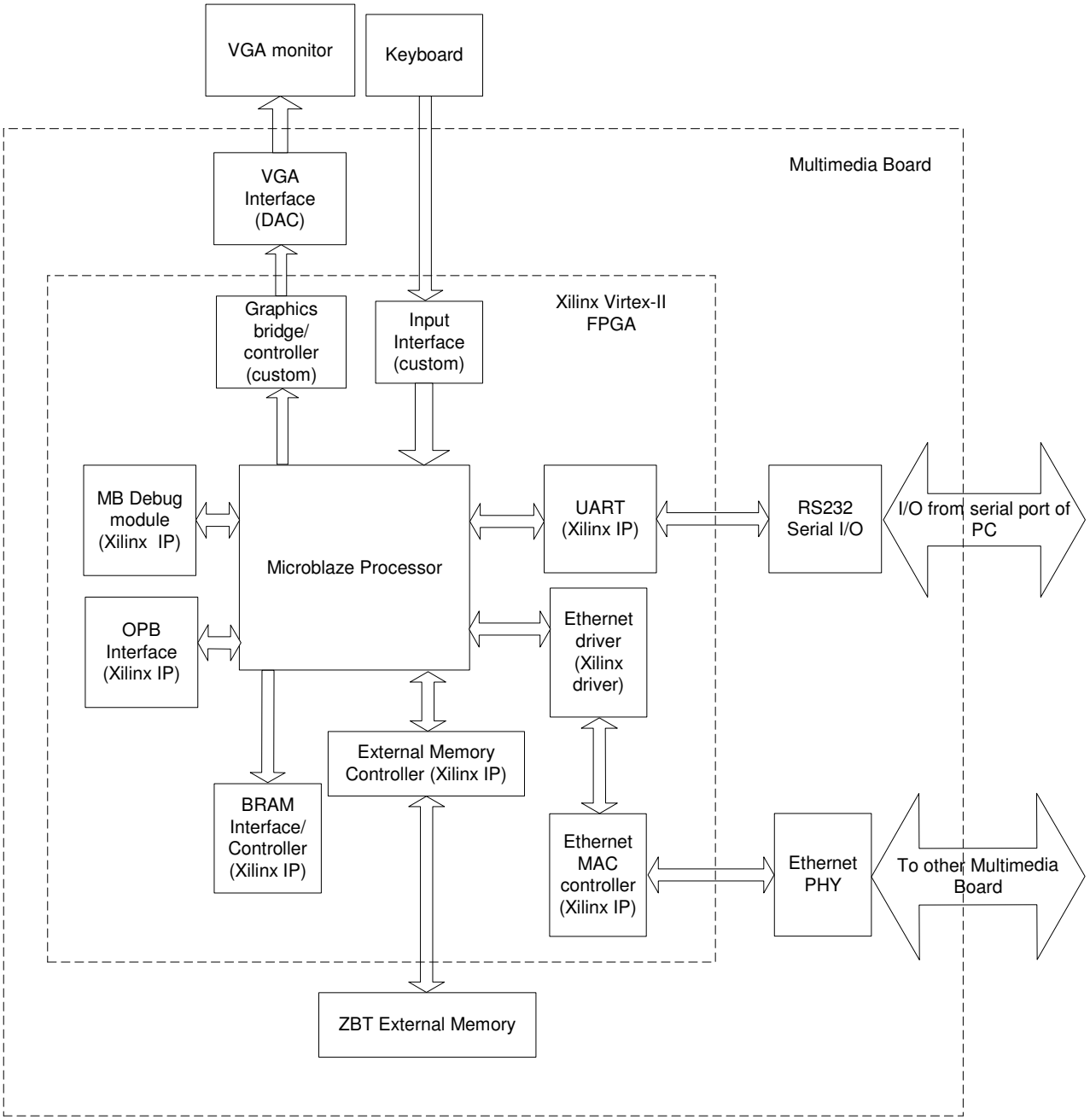
1.1. High Level Description

This system proposal outlines a multiplayer poker card game implemented on the Xilinx Multimedia Board with a Xilinx Virtex-II FPGA. The heart of the system will consist of the Microblaze soft processor core which connects to an Ethernet core on chip. Each running game will communicate over an Ethernet connection to a duplicate system(s) running the same program.

The interaction between different players or systems will proceed on a server/client protocol where one system hosts the game while other systems connect to it over the Ethernet. The Microblaze on the server side will control and keep track of the entire game-play including the cards dealt, the winner of each hand and each player's cash. The other system(s) would function as clients that connect to the server system and run their own copy of the game communicating over the Ethernet.

In addition, each system will display the game status for each player onto a VGA monitor and take input from a keyboard. Both I/O peripherals will be attached directly to the multimedia board. The system block diagram is shown below. Each block is described in subsequent sections.

Figure 1-1 System Block Diagram



1.2. System Description

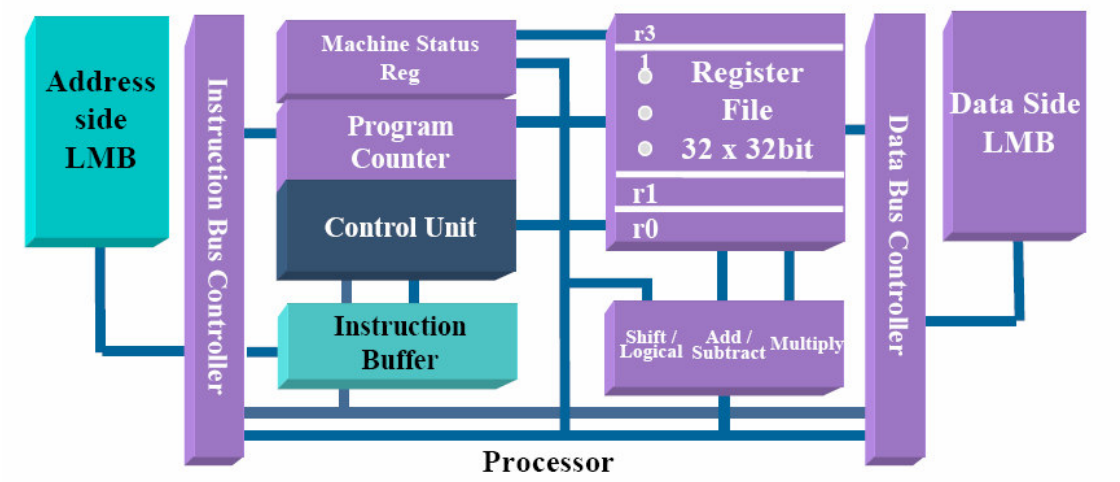
1.2.1. Processor (Microblaze: Xilinx IP)

The Xilinx Microblaze soft processor IP core is central to the SVGA Network Poker system. It is a 32-bit RISC processor that includes the following features:

- Thirty-two 32-bit general purpose RAM based registers with separate instructions for data and memory access
- Separate instruction and data buses (Harvard architecture)
- Built-in interfaces to fast on-chip memory and to IBM's industry-standard On-chip Peripheral Bus (OPB)
- Support for both on-chip Block-RAM and/or external memory.

The Microblaze core is shown in the figure below. It will control the game-play, I/O and communication over the Ethernet with embedded software and Xilinx drivers stored in its 64KB instruction/data memory. This software will control the hardware cores in the system.

Figure 1-2 Microblaze Processor Core



1.2.2. Ethernet (Xilinx IP)

An Ethernet interface will be established using the Ethernet Medium Access Controller (EMAC) provided as a Xilinx IP core. This core can support 32-bit master or slave interfaces on the OPB. The connection speed will be 10/100 Mbps. The EMAC has a media independent interface (MMI) for connection to external 10/100 physical interface (PHY) transceivers. The physical interface is created using a LevelOne LXT972 3.3 Volt PHY. It is an IEEE-compliant Fast Ethernet transceiver that directly supports both 100BASE-TX and 10BASE-T applications. Each board contains a unique 48-bit serial number that can be used as the MAC address for the board. The Ethernet drivers embedded into the processor along with the game communication functions will define and initialize each system as a server or client depending on the connection options.

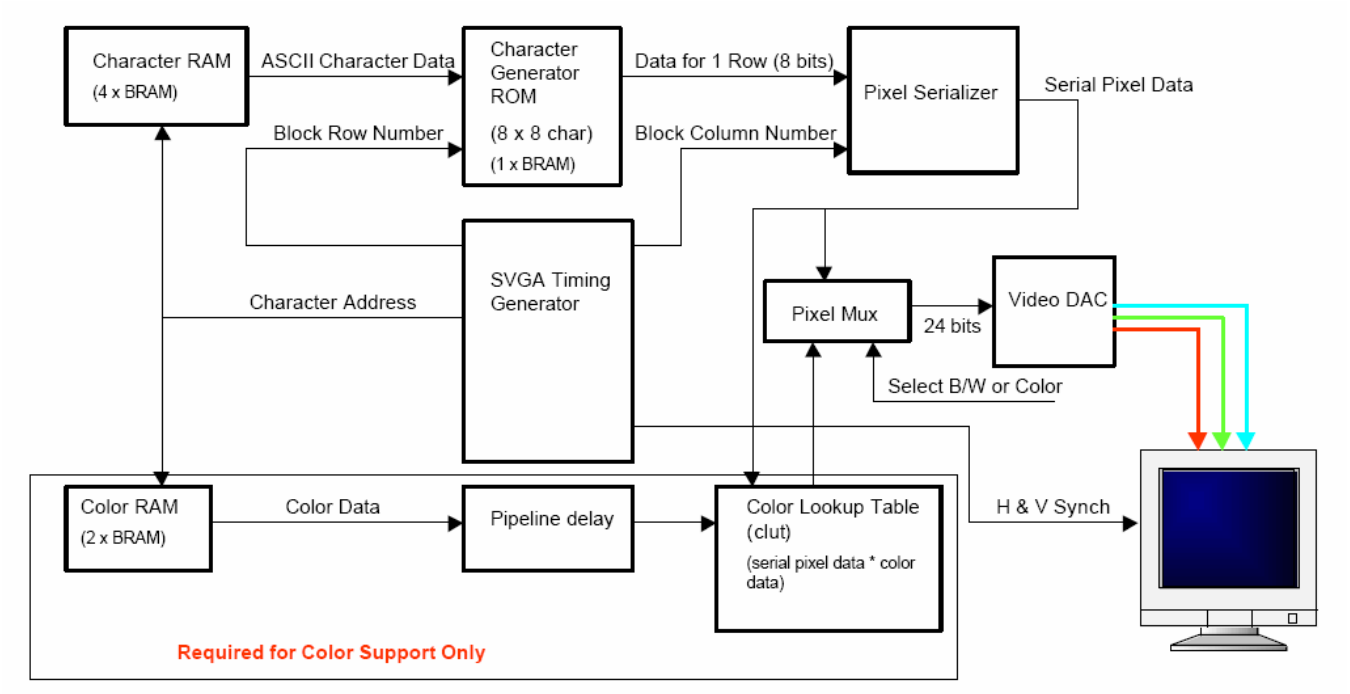
1.2.3. I/O

I/O to the system will be accomplished in two stages. The first stage I/O will consist of serial communication with the processor using a Xilinx IP Universal Asynchronous Receiver/Transmitter (UART) core connected to an off chip RS232 serial port. This port directly connects to the serial interface of a PC. This will be used as the main communication for game play and game display (using ASCII characters) during the design and debug stages of the project. The second stage of I/O will consist of direct connection to and from a keyboard and VGA monitor independent of a PC.

The input will come directly from a keyboard connected to the Multimedia Board through a custom designed input interface to be implemented on the FPGA.

Output will then be transferred directly to a VGA monitor through an SVGA Graphics Bridge/Controller supporting colour character mode SVGA. This graphics controller will be a custom designed core to be implemented on the FPGA. The graphics bridge will be responsible for generating all the timing and control signals to the SVGA interface. The SVGA interface will use an 8-bit DAC for digital to analog conversion and output to the monitor. The block diagram of the character mode SVGA is shown below.

Figure 1-3 Character Mode SVGA Block Diagram



1.2.4. Memory

Two types of memory will be used in the system. On chip block RAM (BRAM will be used to store the character mode SVGA frame data during the second I/O stage and other game-play variables. The BRAM will be controlled through a Xilinx IP core controller.

External ZBT memory will be used when higher capacity storage is required. Such storage might include save game states, store player cash balances or frame buffering for better video quality. This ZBT memory feature may or may not be utilized based on project time constraints but is included for completeness.

1.2.5. Debug

A Microblaze Debug Module (MDM) is included in the system block diagram. This is a Xilinx IP used to access the internal structure of the processor for debugging and troubleshooting during the design and testing phase. This MDM can be interfaced with GNU debugger (GDB) for efficient debugging of software embedded onto the processor.

2. Milestones

Table 2-1 Milestones

2005 Dates	Expected Milestone
February 23	▪ Game-play software complete ▪ Game-play implementation on FPGA without Ethernet using UART for I/O ▪ Ethernet simulations for server and client systems
March 2	▪ Ethernet implementation on FPGA with game-play interface using UART for I/O
March 9	▪ Video drivers and software core complete ▪ Video simulations for character mode SVGA
March 16	▪ SVGA implementation on FPGA with game-play interface using UART for input only
March 23	▪ System integration ▪ Keyboard input implementation on FPGA ▪ Save game implementation on FPGA ▪ Project demo

3. Resources

Resources that will be needed to realize this project are as follows:

- Multimedia boards/cables – 2 or more
- Multiple computers – 1 for each board
- Ethernet cables – 1 or more
- VGA monitors/cables – 1 for each board
- External keyboards – 1 for each board
- Router (optional) – can have more than two players if time permits